ZL30111
POTS Line Card PLL

Data Sheet

January 2007

Features

- Synchronizes to 8 kHz, 2.048 MHz, 8.192 MHz or 19.44 MHz input
- Provides a range of clock outputs: 2.048 MHz, 4.096 MHz and 8.192 MHz
- Provides 2 styles of 8 kHz framing pulses
- Automatic entry and exit from freerun mode on reference fail
- Provides DPLL lock and reference fail indication
- DPLL bandwidth of 922 Hz for all rates of input reference and 58 Hz for an 8 kHz input reference
- Less than 0.6 ns_{pp} intrinsic jitter on all output clocks
- 20 MHz external master clock source: clock oscillator or crystal
- Simple hardware control interface

Ordering Information		
ZL30111QDG	64 Pin TQFP	Trays, Bake & Drypack
ZL30111QDG1	64 Pin TQFP*	Trays, Bake & Drypack
*Pb Free Matte Tin		
-40°C to +85°C		

Applications

- Synchronizer for POTS line cards
- Rate convert NTR 8kHz or GPON physical interface clock to TDM clock

Description

The ZL30111 POTS line card PLL contains a digital phase-locked loop (DPLL), which provides timing and synchronization for SLIC/CODEC devices.

The ZL30111 generates TDM clock and framing signals that are phase locked to the input reference. It helps ensure system reliability by monitoring its reference for stability and by maintaining stable output clocks during short periods when the reference is unavailable.

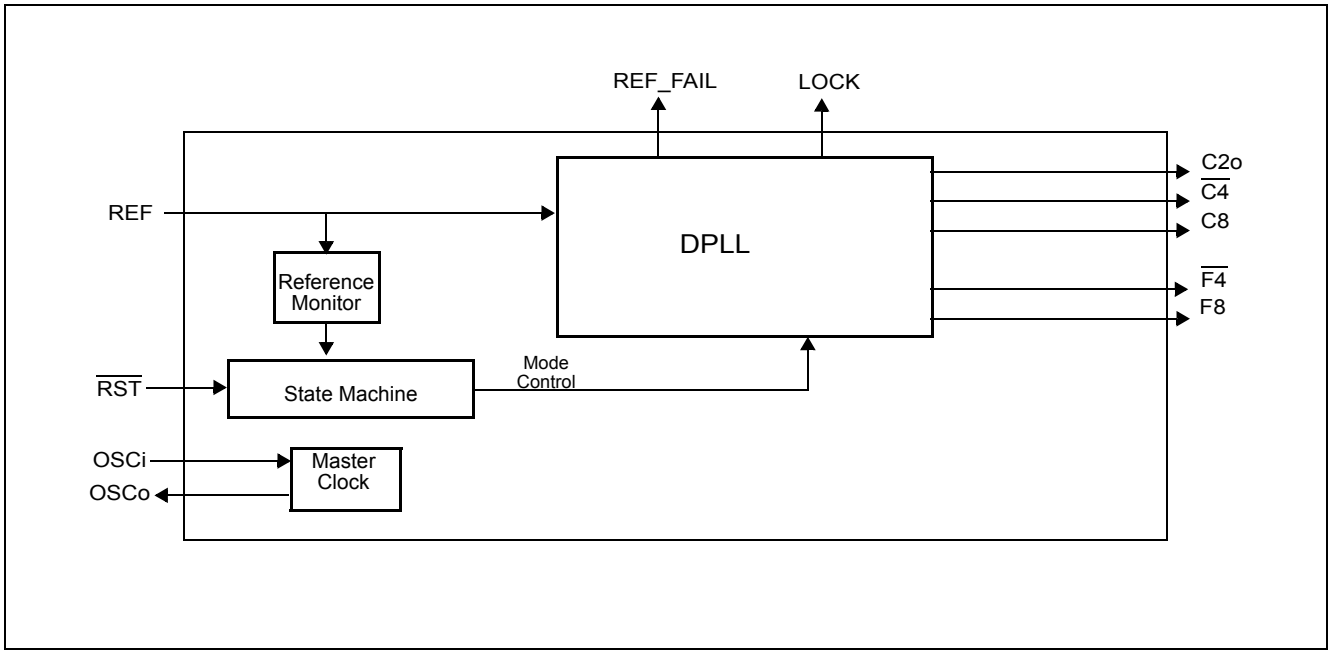

Figure 1 - Functional Block Diagram

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1.0 Physical Description

1.1 Pin Connections

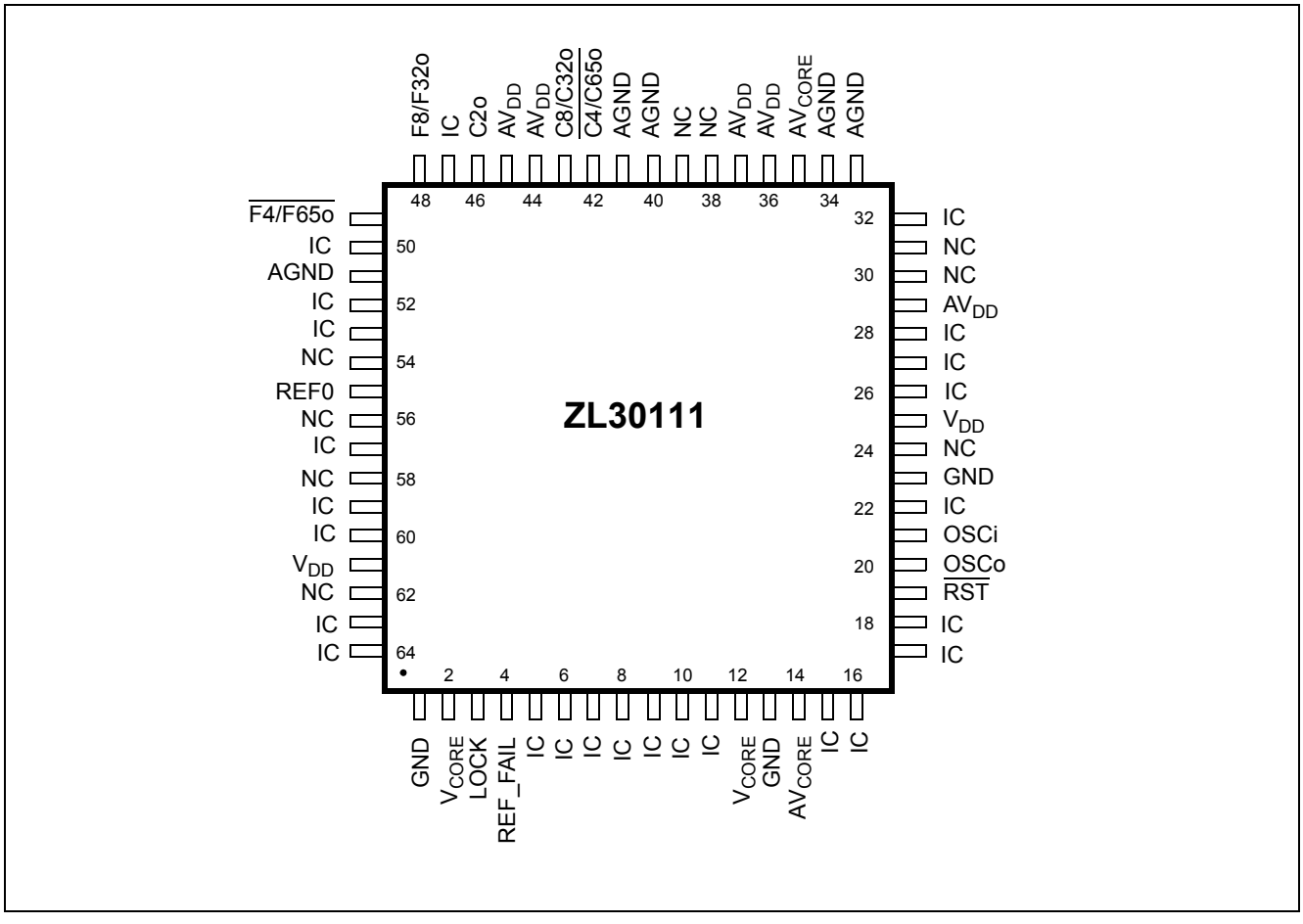


Figure 2 - Pin Connections (64 pin TQFP, please see Note 1)

Note 1: The ZL30111 uses the TQFP shown in the package outline designated with the suffix QD, the ZL30111 does not use the e-Pad TQFP.

1.2 Pin Description

Pin Description

Pin #	Name	Description
1	GND	**Ground.** 0 V.
2	V_{CORE}	**Positive Supply Voltage.** +1.8 V_{DC} nominal.
3	LOCK	**Lock Indicator (Output).** This output goes to a logic high when the PLL is frequency locked to the selected input reference.
4	REF_FAIL	**Reference Failure Indicator (Output).** A logic high at this pin indicates that the REF reference frequency is exhibiting abrupt phase or frequency changes.
5	IC	**Internal Connection.** Leave unconnected.
6	IC	**Internal Connection.** Leave unconnected.
7	IC	**Internal Connection.** Leave unconnected.
8	IC	**Internal Connection.** Leave unconnected.
9	IC	**Internal Connection.** Leave unconnected.
10	IC	**Internal Connection.** Connect to GND.
11	IC	**Internal Connection.** Connect to GND.
12	V_{CORE}	**Positive Supply Voltage.** +1.8 V_{DC} nominal.
13	GND	**Ground.** 0 V.
14	AV_{CORE}	**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal.
15	IC	**Internal Connection.** Leave unconnected.
16	IC	**Internal Connection.** Connect to VDD.
17	IC	**Internal Connection.** Connect to GND.
18	IC	**Internal Connection.** Connect to GND.
19	$\overline{RST}$	**Reset (Input).** A logic low at this input resets the device. On power up, the $\overline{RST}$ pin must be held low for a minimum of 300 ns after the power supply pins have reached the minimum supply voltage. When the RST pin goes high, the device will transition into a Reset state for 3 ms. In the Reset state all clock and frame pulse outputs will be forced into high impedance.
20	OSCo	**Oscillator Master Clock (Output).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCi. This output is not suitable for driving other devices. For clock oscillator operation, this pin must be left unconnected.
21	OSCi	**Oscillator Master Clock (Input).** For crystal operation, a 20 MHz crystal is connected from this pin to OSCo. For clock oscillator operation, this pin must be connected to a clock source.
22	IC	**Internal Connection.** Leave unconnected.
23	GND	**Ground.** 0 V.
24	NC	**No internal bonding Connection.** Leave unconnected.
25	V_{DD}	**Positive Supply Voltage.** +3.3 V_{DC} nominal.
26	IC	**Internal Connection.** Connect this pin to GND.

Pin Description (continued)

Pin #	Name	Description
27	IC	**Internal Connection.** Connect this pin to GND.
28	IC	**Internal Connection.** Connect this pin to GND.
29	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
30	NC	**No internal bonding Connection.** Leave unconnected.
31	NC	**No internal bonding Connection.** Leave unconnected.
32	IC	**Internal Connection.** Leave unconnected.
33	AGND	**Analog Ground.** 0 V
34	AGND	**Analog Ground.** 0 V
35	AV_{CORE}	**Positive Analog Supply Voltage.** +1.8 V_{DC} nominal.
36	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
37	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
38	NC	**No internal bonding Connection.** Leave unconnected.
39	NC	**No internal bonding Connection.** Leave unconnected.
40	AGND	**Analog Ground.** 0 V
41	AGND	**Analog Ground.** 0 V
42	$\overline{C4}$	**Clock 4.096 MHz (Output).** This output is used for ST-BUS operation at 2.048 Mbps or 4.096 Mbps.
43	C8	**Clock 8.192 MHz (Output).** This output is used for ST-BUS and GCI operation at 8.192 Mbps.
44	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
45	AV_{DD}	**Positive Analog Supply Voltage.** +3.3 V_{DC} nominal.
46	C2o	**Clock 2.048 MHz (Output).** This output is used for standard E1 interface timing. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
47	IC	**Internal Connection.** Leave unconnected.
48	F8	**Frame Pulse (Output).** This is an 8 kHz 122 ns active high framing pulse, which marks the beginning of a frame. This clock output pad includes a Schmitt input which serves as a PLL feedback path; proper transmission-line termination should be applied to maintain reflections below Schmitt trigger levels.
49	$\overline{F4}$	**Frame Pulse ST-BUS 2.048 Mbps (Output).** This output is an 8 kHz 244 ns active low framing pulse, which marks the beginning of an ST-BUS frame. This is typically used for ST-BUS operation at 2.048 Mbps and 4.096 Mbps.
50	IC	**Internal Connection.** Leave unconnected.
51	AGND	**Analog Ground.** 0 V

Pin Description (continued)

Pin #	Name	Description
52	IC	**Internal Connection.** Connect this pin to GND.
53	IC	**Internal Connection.** Leave unconnected.
54	NC	**No internal bonding Connection.** Leave unconnected.
55	REF	**Reference (Input).** This is the input reference sources used for synchronization. One of four possible frequencies may be used: 8 kHz, 2.048 MHz, 8.192 MHz or 19.44 MHz. This pin is internally pulled down to GND.
56	NC	**No internal bonding Connection.** Leave unconnected.
57	IC	**Internal Connection.** Leave unconnected.
58	NC	**No internal bonding Connection.** Leave unconnected.
59	IC	**Internal Connection.** Connect this pin to GND.
60	IC	**Internal Connection.** Connect this pin to VDD.
61	V_{DD}	**Positive Supply Voltage.** +3.3 V_{DC} nominal.
62	NC	**No internal bonding Connection.** Leave unconnected.
63	IC	**Internal Connection.** Connect this pin to GND.
64	IC	**Internal Connection.** Connect this pin to VDD.

2.0 Functional Description

The ZL30111 POTS line card PLL contains a digital phase-locked loop (DPLL), which provides timing and synchronization for SLIC/CODEC devices. Figure 1 is a functional block diagram which is described in the following sections.

2.1 Reference Monitor

The input reference is monitored by two reference monitor blocks. The block diagram of reference monitoring is shown in Figure 3. The reference frequency is detected and the clock is continuously monitored for two independent criteria that indicate abnormal behavior of the reference signal, for example; loss of clock or excessive level of frequency error. To ensure proper operation of the reference monitor circuit, the minimum input pulse width restriction of 15 nsec must be observed.

- **Reference Frequency Detector (RFD)**: This detector determines whether the frequency of the reference clock is 8 kHz, 2.048 MHz, 8.192 MHz or 19.44 MHz and provides this information to the various monitor circuits and the phase detector circuit of the DPLL.
- **Coarse Frequency Monitor (CFM)**: This circuit monitors the reference frequency over intervals of approximately 30 μs to quickly detect large frequency changes.
- **Single Cycle Monitor (SCM)**: This detector checks the period of a single clock cycle to detect large phase hits or the complete loss of the clock.

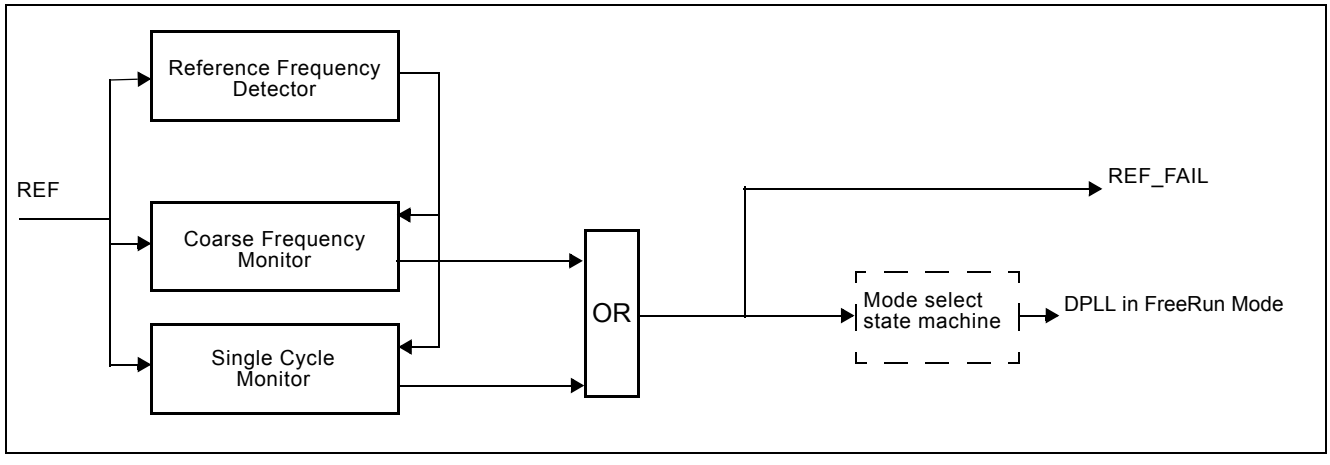


Figure 3 - Reference Monitor Circuit

Exceeding the thresholds of any of the monitors forces the corresponding REF_FAIL pin to go high. The single cycle and coarse frequency failure flags force the DPLL into FreeRun mode.

2.2 Digital Phase Lock Loop (DPLL)

The DPLL of the ZL30111 consists of a phase detector, a loop filter and a digitally controlled oscillator.

Phase Detector - the phase detector compares the input reference signal to the feedback signal and provides an error signal corresponding to the phase difference between the two.

Loop Filter - the loop filter is similar to a first order low pass filter with a bandwidth of 922 Hz. For stability reasons, the loop filter bandwidth for an 8 kHz reference is limited to a maximum of 58 Hz.

Digitally Controlled Oscillator (DCO) - the DCO receives the filtered signal from the Loop Filter, and based on its value, generates a corresponding digital output signal. The synchronization method of the DCO is dependent on the state of the ZL30111.

In Normal Mode, the DCO provides an output signal which is frequency and phase locked to the selected input reference signal.

In Freerun Mode, the DCO is free running with an accuracy equal to the accuracy of the OSCi 20 MHz source.

Lock Indicator - the lock detector monitors if the output value of the phase detector is within the phase-lock-window for a certain time. The selected phase-lock-window guarantees the stable operation of the LOCK pin with maximum network jitter and wander on the reference input. If the DPLL goes into FreeRun mode, the LOCK pin will initially stay high for 0.1 s. If at that point the DPLL is still in FreeRun mode, the LOCK pin will go low. In Freerun mode the LOCK pin will go low immediately.

2.3 Frequency Synthesizers

The output of the DCO is used by the frequency synthesizer to generate the output clock which is synchronized to the inputs (REF). The frequency synthesizer uses digital techniques to generate output clock and advanced noise shaping techniques to minimize the output jitter. The clock and frame pulse outputs have limited driving capability and should be buffered when driving high capacitance loads.

2.4 State Machine

As shown in Figure 1, the state machine controls the DPLL.

2.5 Master Clock

The ZL30111 can use either a clock or crystal as the master timing source. For recommended master timing circuits, see the Applications - Master Clock section.

3.0 DPLL Modes of Operation

The ZL30111 has two possible modes of operation; Normal, and Freerun. The ZL30111 starts up in Freerun mode, it automatically transitions to Normal mode if a valid reference is available and transitions to Freerun mode if the reference fails.

3.1 Freerun Mode

Freerun mode is typically used when an independent clock source is required or immediately following system power-up before synchronization is achieved.

In Freerun mode, the ZL30111 provides timing and synchronization signals which are based on the master clock frequency (supplied to OSCi pin) only and are not synchronized to the reference input signals.

The accuracy of the output clock is equal to the accuracy of the master clock (OSCi). So if a ±32 ppm output clock is required, the master clock must also be ±32 ppm. See Applications - Section 5.2, “Master Clock“.

Freerun Mode is also used for short durations while system synchronization is temporarily disrupted. The accuracy of the output clock during these input reference disruptions is better than the accuracy of the master clock (OSCi), but it is off compared to the reference before disruptions.

3.2 Normal Mode

Normal mode is typically used when a system clock source, synchronized to the network is required. In Normal mode, the ZL30111 provides timing synchronization signals, which are synchronized to the input (REF). The input reference signal may have a nominal frequency of 8 kHz, 2.048 MHz, 8.192 MHz or 19.44 MHz. The frequency of the reference inputs are automatically detected by the reference monitors.

When the ZL30111 comes out of RESET it will initially go into Freerun mode and generate a clock with the accuracy of its freerunning local oscillator (see Figure 4). If the ZL30111 determines that its selected reference is disrupted (see Figure 3), it will remain in Freerun until the selected reference is no longer disrupted. If the ZL30111 determines that the reference is not disrupted (see Figure 3) then the state machine will cause the DPLL to recover from Freerun and transition to Normal mode.

When the ZL30111 is operating in Normal mode, if it determines that the input reference is disrupted (Figure 3) then its state machine will cause it to automatically go to Freerun mode. When the ZL30111 determines that its selected reference is not disrupted then the state machine will cause the DPLL to recover from Freerun and transition to Normal mode.

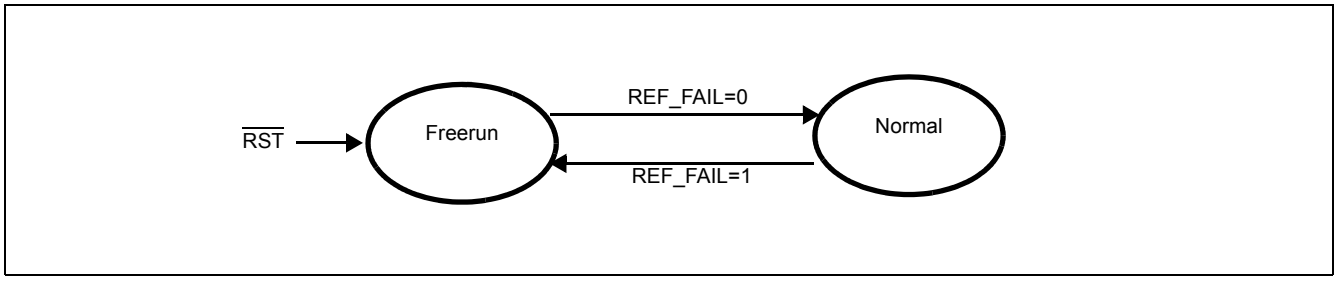


Figure 4 - DPLL Mode Switching

4.0 Measures of Performance

The following are some PLL performance indicators and their corresponding definitions.

4.1 Jitter

Timing jitter is defined as the high frequency variation of the clock edges from their ideal positions in time. Wander is defined as the low-frequency variation of the clock edges from their ideal positions in time. High and low frequency variation imply phase oscillation frequencies relative to some demarcation frequency. (Often 10 Hz or 20 Hz for DS1 or E1, higher for SONET/SDH clocks.) Jitter parameters given in this data sheet are total timing jitter numbers, not cycle-to-cycle jitter.

4.2 Jitter Generation (Intrinsic Jitter)

Jitter generation is the measure of the jitter produced by the PLL and is measured at its output. It is measured by applying a reference signal with no jitter to the input of the device, and measuring its output jitter. Jitter is usually measured with various band limiting filters depending on the applicable standards.

4.3 Jitter Transfer

Jitter transfer or jitter attenuation refers to the magnitude of jitter at the output of a device for a given amount of jitter at the input of the device. Input jitter is applied at various amplitudes and frequencies, and output jitter is measured with various filters depending on the applicable standards.

4.4 Lock Time

This is the time it takes the PLL to frequency lock to the input signal. Phase lock occurs when the input signal and output signal are aligned in phase with respect to each other within a certain phase distance (not including jitter). Lock time is affected by many factors which include:

- initial input to output phase difference
- initial input to output frequency difference
- PLL loop filter bandwidth

The presence of input jitter makes it difficult to define when the PLL is locked as it may not be able to align its output to the input within the required phase distance, dependent on the PLL bandwidth and the input jitter amplitude and frequency.

5.0 Applications

This section contains ZL30111 application specific details for power supply decoupling, reset operation, clock and crystal operation.

5.1 Power Supply Decoupling

Jitter levels on the ZL30111 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the ZL30111 device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Zarlink Application Note ZLAN-178.

5.2 Master Clock

The ZL30111 can use either a clock or crystal as the master timing source.

5.2.1 Clock Oscillator

When selecting a clock oscillator, numerous parameters must be considered. This includes absolute frequency, frequency change over temperature, output rise and fall times, output levels, duty cycle and phase noise.

The output clock should be connected directly (not AC coupled) to the OSCi input of the ZL30111, and the OSCo output should be left open as shown in Figure 5.

1	Frequency	20 MHz
2	Tolerance	as required (better than +/-50ppm)
3	Rise & fall time	< 8 ns
4	Duty cycle	40% to 60%

Table 1 - Clock Oscillator Specification

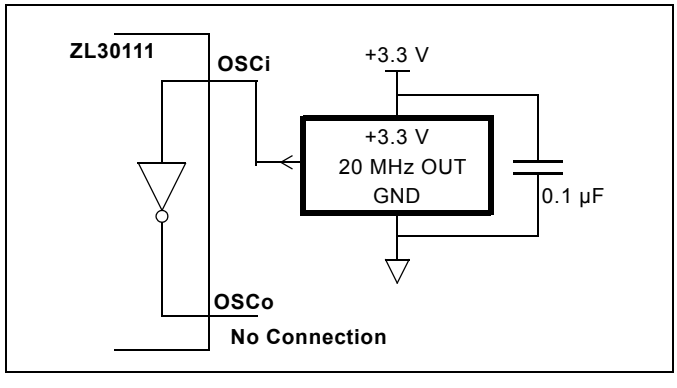


Figure 5 - Clock Oscillator Circuit

5.2.2 Crystal Oscillator

Alternatively, a Crystal Oscillator may be used. The accuracy of a crystal oscillator depends on the crystal tolerance as well as the load capacitance tolerance. Typically, for a 20 MHz crystal specified with a 32 pF load capacitance, each 1 pF change in load capacitance contributes approximately 9 ppm to the frequency deviation. Consequently, capacitor tolerances and stray capacitances have a major effect on the accuracy of the oscillator frequency.

The crystal should be a fundamental mode type - not an overtone. The fundamental mode crystal permits a simpler oscillator circuit with no additional filter components and is less likely to generate spurious responses. A typical crystal oscillator specification is shown in Table 2.

1	Frequency	20 MHz
2	Tolerance	as required (better than +/-50ppm)
3	Oscillation mode	fundamental
4	Resonance mode	parallel
5	Load capacitance	as required
6	Maximum series resistance	50 Ω

Table 2 - Crystal Oscillator Specification

5.3 Power Up Sequence

The ZL30111 requires that the 3.3 V supply is not powered up after the 1.8 V supply. This is to prevent the risk of latch-up due to the presence of protection diodes in the IO pads.

Two options are given:

1. Power-up the 3.3 V supply fully first, then power up the 1.8 V supply

2. Power up the 3.3 V supply and the 1.8 V supply simultaneously, ensuring that the 3.3 V supply is never lower than a few hundred millivolts below the 1.8 V supply (e.g., by using a schottky diode or controlled slew rate)

5.4 Reset Circuit

A simple power up reset circuit with about a 60 μs reset low time is shown in Figure 6. Resistor R_P is for protection only and limits current into the $\overline{RST}$ pin during power down conditions. The reset low time is not critical but should be greater than 300 ns.

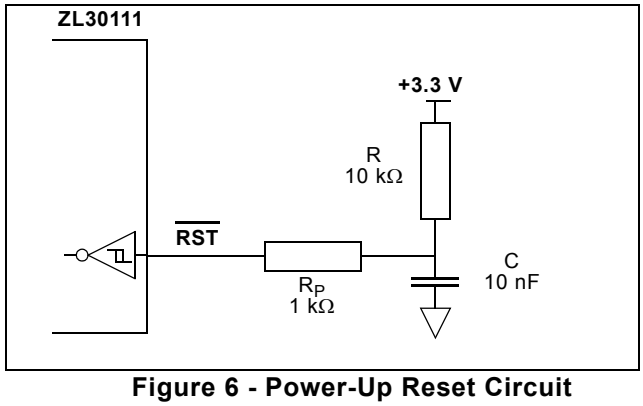


Figure 6 - Power-Up Reset Circuit

6.0 Characteristics

6.1 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Core supply voltage	V_{CORE_R}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on OSCi and OSCo pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Current on any pin	I_{PIN}		30	mA
6	Storage temperature	T_{ST}	-55	125	°C
7	TQFP 64 pin package power dissipation	P_{PD}		500	mW
8	ESD rating	V_{ESD}		2	kV

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated.

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}	3.1	3.30	3.5	V
2	Core supply voltage	V_{CORE}	1.7	1.80	1.9	V
3	Operating temperature	T_A	-40	25	85	°C
4	Input Voltage	V_I	0	3.3	3.5	V

* Voltages are with respect to ground (GND) unless otherwise stated.

DC Electrical Characteristics*

	Characteristics	Sym.	Min.	Max.	Units	Notes
1	Supply current with: OSCi = 0 V	I_{DDS}	3.0	6.5	mA	outputs loaded with 30 pF
2	OSCi = Clock, OUT_SEL=0	I_{DD}	32	47	mA	
4	Core supply current with: OSCi = 0 V	I_{CORES}	0	22	µA	
5	OSCi = Clock	I_{CORE}	14	20	mA	
6	Schmitt trigger Low to High threshold point	V_{t+}	1.43	1.85	V	All device inputs are Schmitt trigger type.
7	Schmitt trigger High to Low threshold point	V_{t-}	0.80	1.10	V	
8	Input leakage current	I_{IL}	-105	105	µA	$V_I = V_{DD}$ or 0 V
9	High-level output voltage	V_{OH}	2.4		V	I_{OH} = 8 mA for clock and frame-pulse outputs, 4 mA for status outputs
10	Low-level output voltage	V_{OL}		0.4	V	I_{OL} = 8 mA for clock and frame-pulse outputs, 4 mA for status outputs

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

AC Electrical Characteristics* - Timing Parameter Measurement Voltage Levels (see Figure 7)

	Characteristics	Sym.	CMOS	Units	Notes
1	Threshold voltage	V_T	$0.5xV_{DD}$	V	
2	Rise and fall threshold voltage high	V_{HM}	$0.7xV_{DD}$	V	
3	Rise and fall threshold voltage low	V_{LM}	$0.3xV_{DD}$	V	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

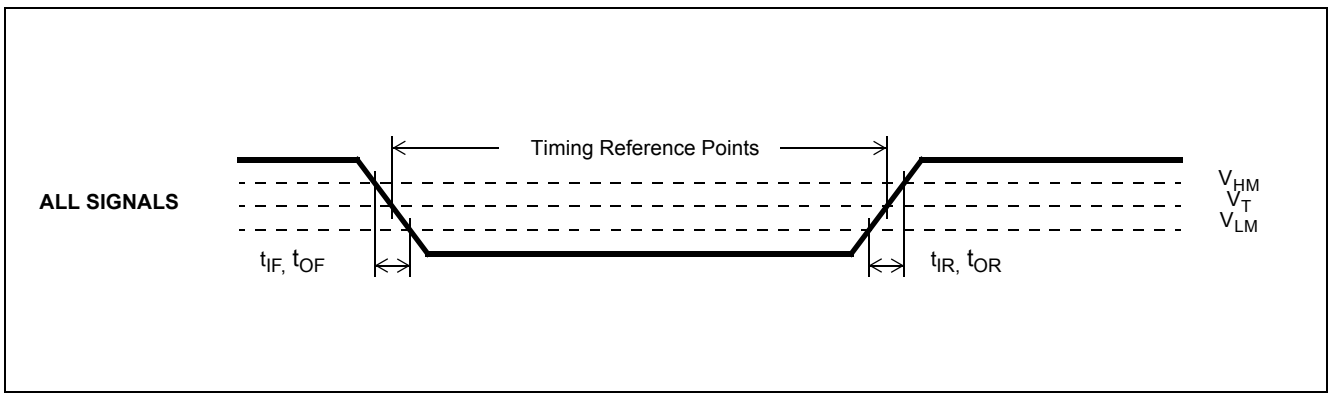


Figure 7 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics* - Input Timing (see Figure 8)

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	8 kHz reference period	t_{REF8KP}	121	125	128	µs
2	2.048 MHz reference period	t_{REF2P}	263	488	712	ns
3	8.192 MHz reference period	t_{REF8P}	63	122	175	ns
4	19.44 MHz reference period	t_{REF16P}	38	51	75	ns
5	reference pulse width high or low	t_{REFW}	15			ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Period Min/Max values are the limits to avoid a single-cycle fault detection. Short-term and long-term average periods must be within Out-of-Range limits.

AC Electrical Characteristics* - Input to Output Timing (see Figure 8)

	Characteristics	Symbol	Min.	Max.	Units
1	8 kHz reference input to F8o delay	t_{REF8KD}	0	8	ns
2	2.048 MHz reference input to C2o delay	t_{REF2D}	2	10	ns
3	2.048 MHz reference input to F8o delay	t_{REF2_F8D}	2	10	ns
4	8.192 MHz reference input to C8o delay	t_{REF8D}	5	13	ns
5	8.192 MHz reference input to F8o delay	t_{REF8_F8D}	5	13	ns
6	19.44 MHz reference input to F8o delay	t_{REF9D_F8D}	0	8	ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

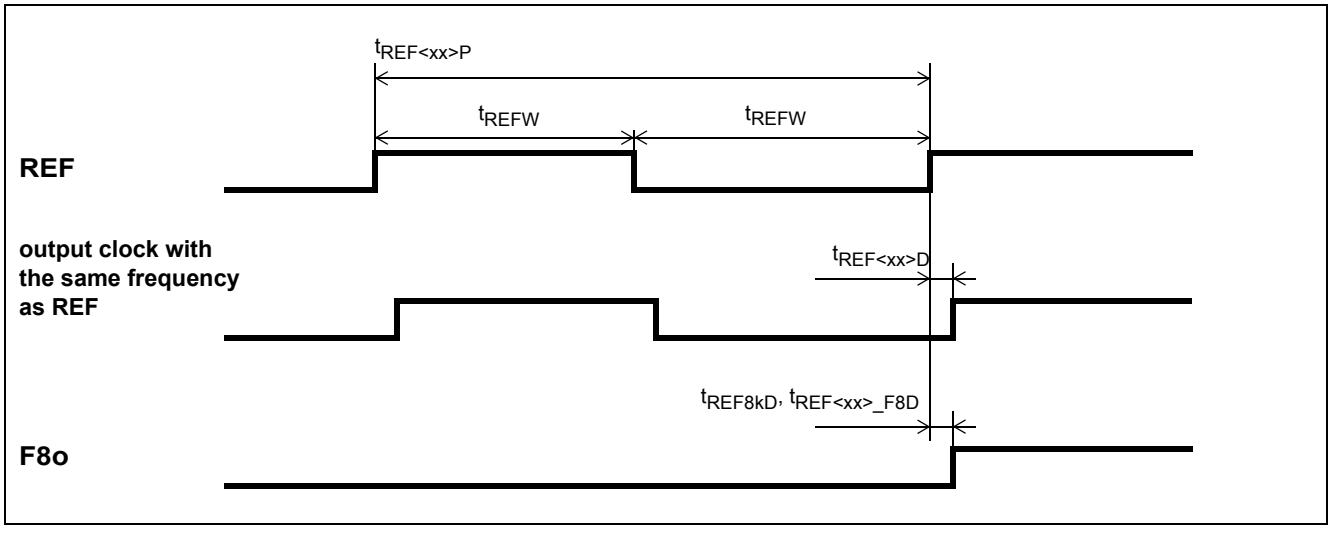


Figure 8 - Input to Output Timing

AC Electrical Characteristics* - Output Timing (see Figure 9)

	Characteristics	Sym.	Min.	Max.	Units	Notes
1	C2o pulse width low	t_{C2L}	243	245	ns	
2	C2o delay	t_{C2D}	-1.0	1.0	ns	
3	$\overline{F4o}$ pulse width low	t_{F4L}	243	245	ns	
4	$\overline{F4o}$ delay	t_{F4D}	121	123	ns	
5	$\overline{C4o}$ pulse width low	t_{C4L}	121	123	ns	
6	$\overline{C4o}$ delay	t_{C4D}	-1.0	1.0	ns	
7	F8o pulse width high	t_{F8H}	121	124	ns	
8	C8o pulse width low	t_{C8L}	60	62	ns	
9	C8o delay	t_{C8D}	-1.0	1.0	ns	
10	Output clock and frame pulse rise time	t_{OR}	1.0	2.0	ns	
11	Output clock and frame pulse fall time	t_{OF}	1.0	2.5	ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions and 30 pF load.

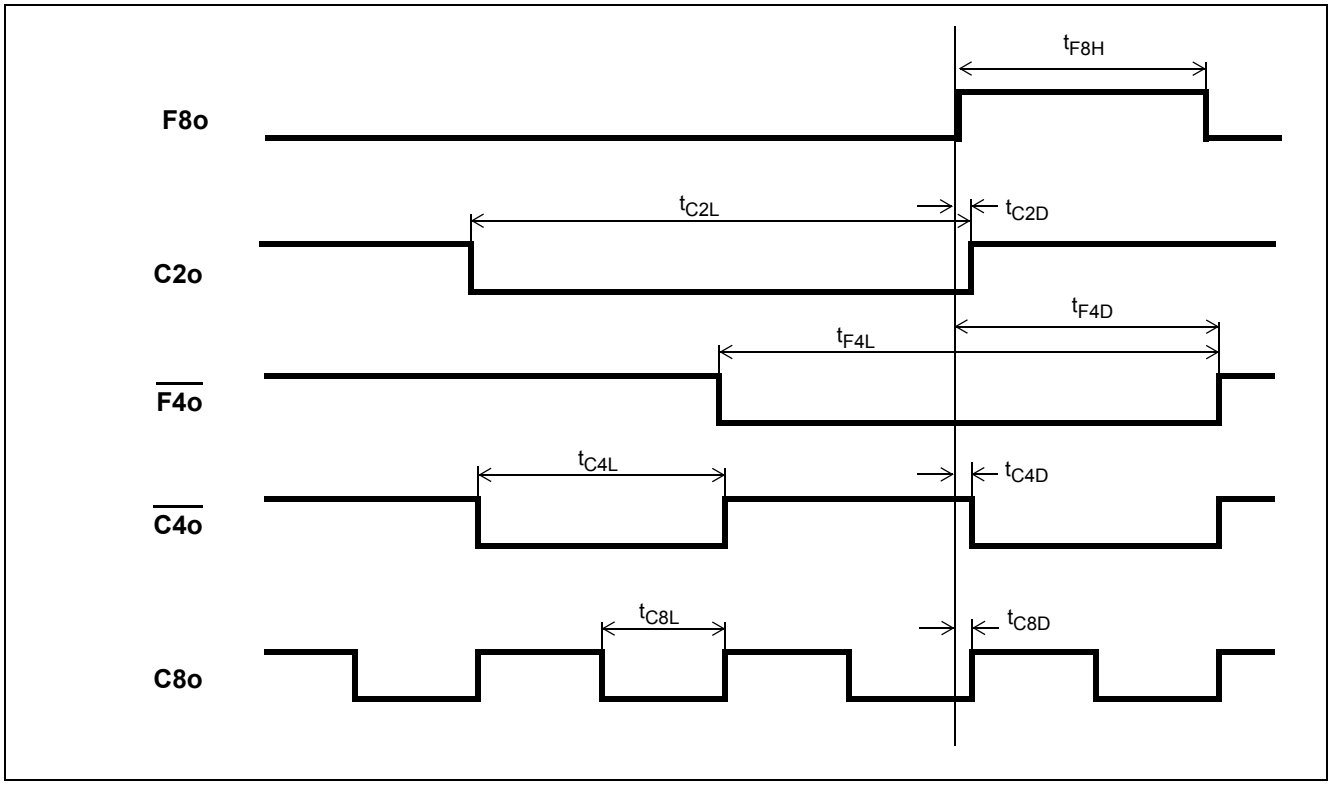


Figure 9 - Output Timing Referenced to F8o

6.2 Performance Characteristics

Performance Characteristics* - Functional

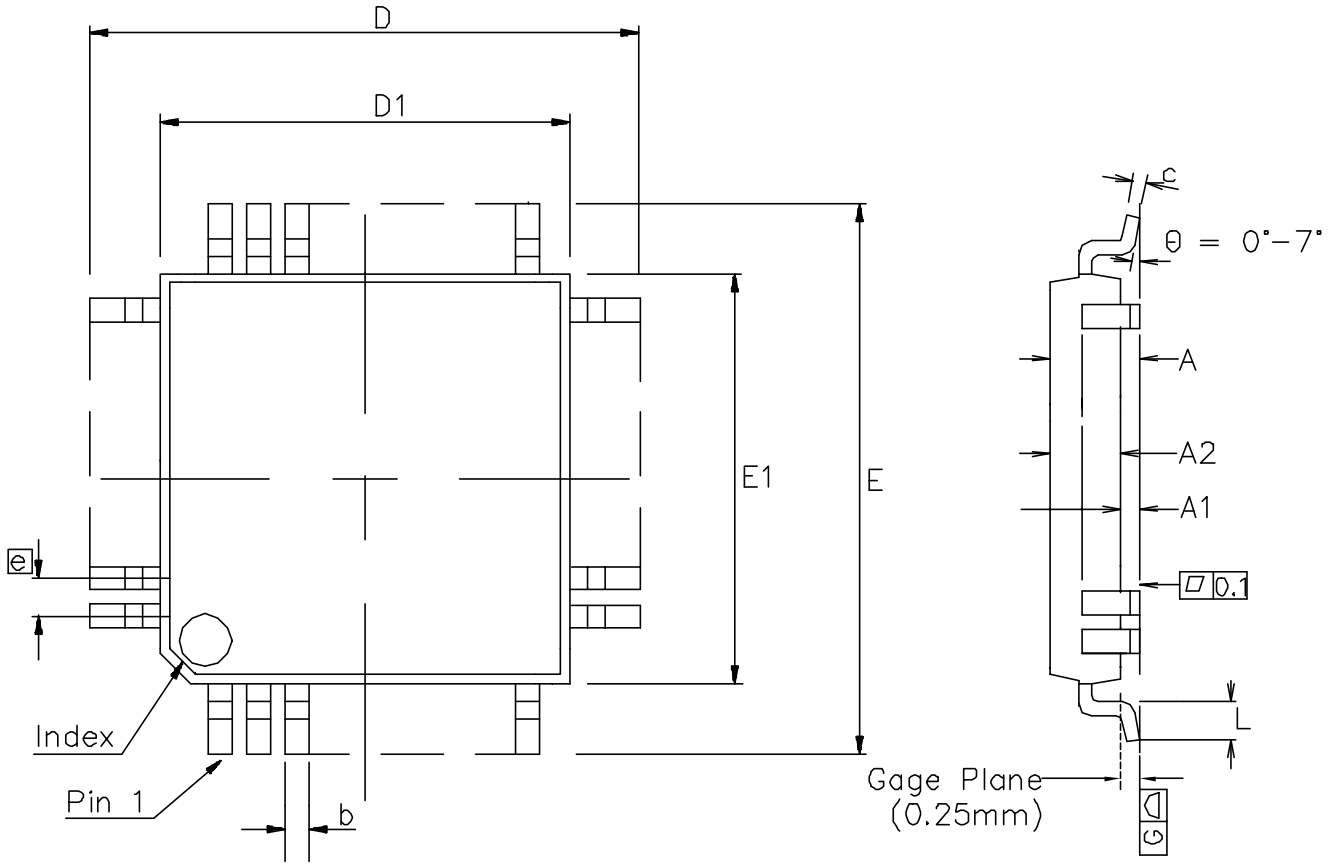
	Characteristics	Min.	Typ.	Max.	Units	Notes
1	DPLL capture range	-130		+130	ppm	The 20 MHz Master Clock oscillator set at 0.ppm
Lock Time						
2	DPLL 58 Hz Filter			1	s	input reference = 8 kHz, ±100 ppm frequency offset
3	DPLL 922 Hz Filter			1	s	input reference ≠ 8 kHz, ±100 ppm frequency offset

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

Performance Characteristics* - Unfiltered Intrinsic Jitter

	Characteristics	Max. [ns_{pp}]	Notes
1	C2o (2.048 MHz)	0.6	
2	$\overline{C4o}$ (4.096 MHz)	0.6	
3	C8o (8.192 MHz)	0.6	
4	$\overline{F4o}$ (8 kHz)	0.6	
5	F8o (8 kHz)	0.6	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.20		---	0.047
A1	0.05	0.15		0.002	0.006
A2	0.95	1.05		0.037	0.041
D	12.00 BSC			0.472 BSC	
D1	10.00 BSC			0.394 BSC	
E	12.00 BSC			0.472 BSC	
E1	10.00 BSC			0.394 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	64				
ND	16				
NE	16				
NOTE	SQUARE				

Conforms to JEDEC MS-026 ACD Iss. C

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protrusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

ISSUE	1	2	3	4
ACN	203170	207075	213856	CDCA
DATE	14Oct97	5Jul99	17Dec02	15Aug05
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

TP/TH

Package Code QD/QG

Package Outline for 64 Lead TQFP 10x10x1.0mm, +2.0mm (footprint)

GPD00450

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