EVALSPEAr310 - evaluation board for the SPEAr310

1 Description

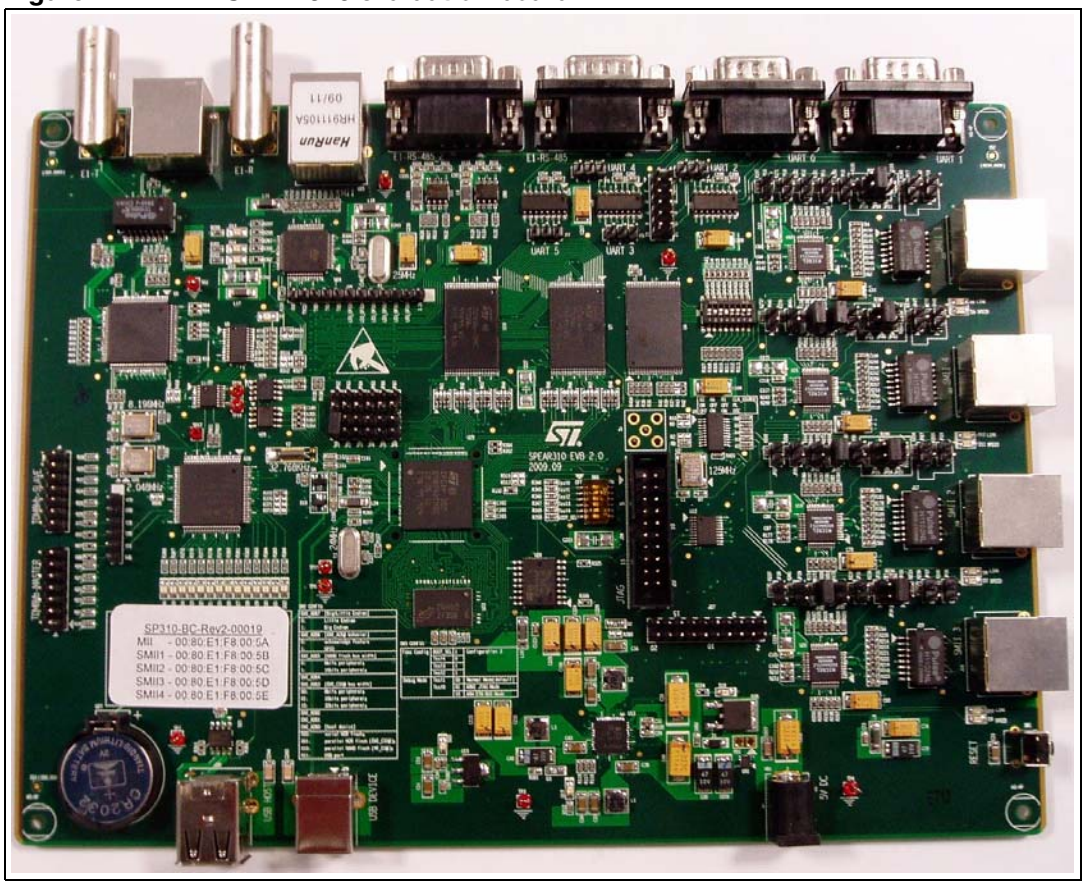
This user manual describes how to use the EVALSPEAr310 evaluation board for SPEAr310.

It is intended to be used for three main purposes:

- To allow you to quickly evaluate and debug software for the SPEAr310
- Act as a learning tool to rapidly get familiar with the SPEAr310 features
- Provide a starting point for the development of the final application board

The EVALSPEAR310 board is equipped with one MII Ethernet port, four SMII Ethernet ports, six RS232 ports, two HDLC based RS485 ports and one E1/TDM port. Memory devices included are NAND Flash, parallel NOR Flash, serial NOR Flash, and I²C EEPROM.

Figure 1. EVALSPEAr310 evaluation board



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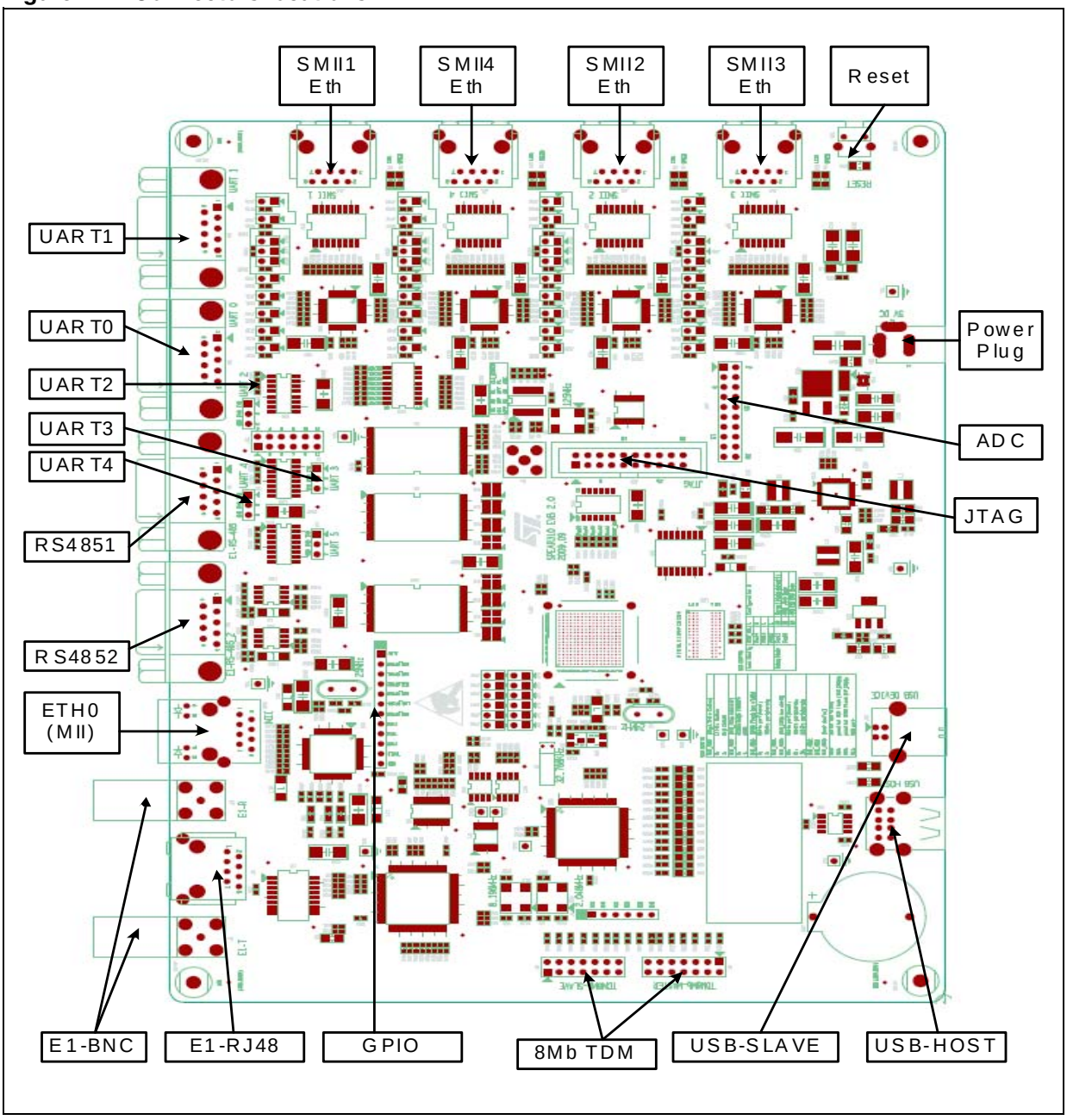
2 Contents of the kit

The EVALSPEAR310 evaluation board kit contains:

- SPEAr310 evaluation board
- AC adapter (output voltage 5 V)
- 2 plug adapters (USA/Europe)
- User manual

3 Connectors locations

Figure 2. Connectors locations



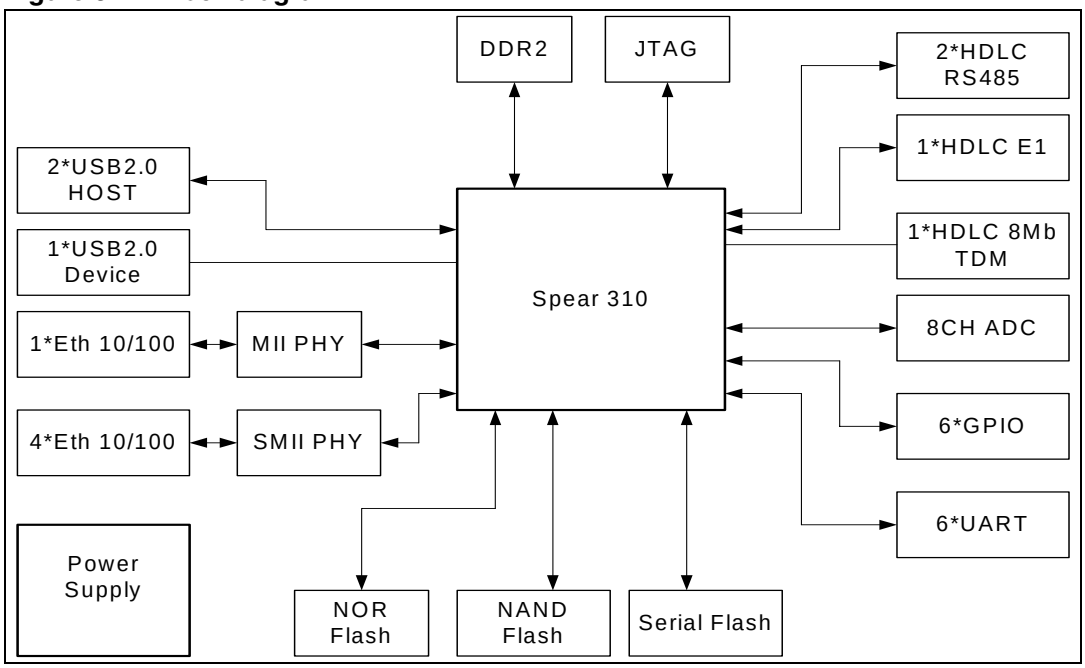
4 Features and block diagram

4.1 Features

- SPEAr310 embedded MPU
- Up to 2 Gbits DDR2 333 MHz (std 128 Mbytes)
- Up to 1.5 Gbytes Parallel NOR Flash (std 16 Mbytes)
- Up to 16 Mbytes Serial NOR Flash memory (std 64 Mbytes)
- Up to 2 Gbits NAND Flash memory (std 64 Mbytes)
- 4 Kb Serial I^2C EEPROM
- 4 Mb SPI Flash memory
- Two USB 2.0 full Host port channels
- One USB 2.0 high speed Device
- One 10/100 Ethernet port based on MII PHY
- Four 10/100 Ethernet port based on SMII PHY
- One E1, 2x BNC/RJ48(2.048 Mbits)
- Two HDLC RS485 DB9 ports (up to 4 MHz)
- One HDLC-TDM port (8 Mb, 128 TS)
- Six Serial ports (up to 115 kbaud)
- 8 ADC channels (10 bit, 1 Msamples)
- 6 GPIOs
- JTAG debug port

4.2 Block diagram

Figure 3. Block diagram



5 Start up

5.1 Unpacking

ELECTROSTATIC WARNING:
The SPEAr310 evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. General practices for working with static sensitive devices should be applied when working with this board.

- **Wear an anti-static wristband** - Wearing a simple anti-static wristband can help to prevent ESD from damaging the SPEAr310 evaluation board.
- **Self-grounding** - Touch a grounded conducting material before handling and periodically while handling the SPEAr310 evaluation board.
- **Use an anti-static pad** - When configuring the SPEAr310 evaluation board, place it on an antic-static pad to reduce the possibility of ESD damage.
- **Only handle the board edges** - When handling the SPEAr310 evaluation board.

5.2 Connection

- Connect a serial cable (RS232 on UART0) to a host PC.
- On a host PC running Windows or Linux, start the Terminal program.
- Connect the AC Adapter to a power outlet.
- Power ON the board (plug the jack of the AC/Adapter on VB1). A sequence of boot messages is displayed, followed by the Linux console prompt.

For more information, refer to the *Getting started with Linux for SPEAr (UM0844)* available on www.st.com.

5.3 Booting procedure

The SPEAr310 board is able to boot a Linux kernel pre-installed in the serial NOR Flash.

At power on, the serial port outputs a brief header message with some uBoot information (uBoot version, SDK version, and some internal hardware information). At this point you can choose to:

1. **Stop the system directly in uBoot**: For this you have to press the spacebar on the host computer keyboard before the boot delay time expires (default is 3 seconds).
2. **Boot Linux**: The system logs you in automatically as super user and the Linux shell prompt is displayed on the screen.

6 Block descriptions

6.1 MII Ethernet

There is one MII Ethernet PHY available on the board at U24, connected through the media independent interface to the Ethernet MAC on the CPU processor.

By default the MII address of the MII Ethernet PHY is selected as shown in *Table 1.*

Table 1. MII address of the MII Ethernet PHY at U24

Component	MII address
U24	0x04

By default the initial configuration of the MII Ethernet PHY is selected as shown in *Table 2.*

Table 2. Default configuration of the Ethernet PHY in U24

Function	Default configuration
Auto negotiation	Enabled
10/100 Mbits	100 Mbits selected for auto negotiation advertisement
Half/Full duplex	Full duplex selected for auto negotiation advertisement
Internal loopback	Disabled
Power down	Disabled (PHY active)
MII/RMII mode	MII selected

There are two LEDs embedded in each RJ45 connector (U25) which are used to indicate the status of the line:

- The green LED in the connector is driven on continuously when the Ethernet link is established with the counterpart.
- The yellow LED in the connector blinks when there is TX or RX activity.

The Serial Management Interface (SMI) is part of the MII interface and is used to transfer management information between MAC and PHY (access to the PHY registers).

For the correct functionality of the MII Ethernet PHY (U24 in MII mode), it is necessary to clock with a by 25 MHz clock. The default option is to use oscillator OSC1.

6.2 SMII Ethernet

There are four SMII Ethernet PHYs available on the board at U18, U19, U20 and U21, connected through serial media independent interfaces to the Ethernet MACs in the SPEAr310 MPU.

By default the SMII addresses of the SMII Ethernet PHYs are selected as shown in *Table 3*.

Table 3. SMII addresses of the SMII Ethernet PHYs

Component	MII address
U18	0x01
U19	0x03
U20	0x05
U21	0x07

By default the external configuration of the SMII-1 Ethernet PHYs is selected as shown in *Table 4*.

Table 4. SMII-1 PHY jumpers

Jumper	Description	Default configuration
JP13, JP14, JP15	**SMII PHY U18 mode configuration**: Default: JP13-open, JP14-fitted, JP15-open: Set U18 to work as SMII function	**JP10** **JP11** **JP12**
JP10, JP11, JP12	**SMII PHY U18 address configurations**: Default: JP10-open, JP11-open, JP12-open: Set SMII-1 PHY address: 0x01	**JP10** **JP11** **JP12**
JP16	**Isolate mode**: Pull-up = Enable Pull-down (default) = Disable	**JP16**
JP17	**Nway auto-negotiation enable**: Pull-up (default) = Enable auto-negotiation Pull-down = Disable auto-negotiation	**JP17**
JP18	**Speed mode**: Pull-up (default) = 100 Mbps Pull-down = 10 Mbps	**JP18**
JP19	**Duplex mode**: Pull-up (default) = Half duplex Pull-down = Full duplex	**JP19**

By default the external configuration of the SMII-2 Ethernet PHYs is selected as shown in *Table 5*.

Table 5. SMII-2 PHY jumpers

Jumper	Description	Default configuration
JP23, JP24, JP25	**SMII PHY U19 mode configuration:** Default: JP23-open, JP24-fitted, JP25-open: Set U19 to work as SMII function	**JP23** **JP24** **JP25**
JP20, JP21, JP22	**SMII PHY U19 addresses configuration:** Default: JP20-open, JP21-open, JP22-open: Set SMII-2 PHY address: 0x03	**JP20** **JP21** **JP22**
JP26	**ISOLATE mode:** Pull-up = Enable Pull-down (default) = Disable	**JP26**
JP27	**Nway auto-negotiation enable:** Pull-up (default) = Enable auto-negotiation Pull-down = Disable auto-negotiation	**JP27**
JP28	**Speed mode:** Pull-up (default) = 100 Mbps Pull-down = 10 Mbps	**JP28**
JP29	**Duplex mode:** Pull-up (default) = Half duplex Pull-down = Full duplex	**JP29**

By default the external configuration of the SMII-3 Ethernet PHYs is selected as shown in *Table 6.*

Table 6. SMII-3 PHY jumper

Jumper	Description	Default configuration
JP33, JP34, JP35	**SMII PHY U20 mode configuration:** Default: JP33-open, JP34-fitted,JP35-open: Set U20 to work as SMII function	**JP33** **JP34** **JP35**
JP30, JP31, JP32	**SMII PHY U20 addresses configuration:** Default: JP30-open, JP31-open, JP32-open: Set SMII-3 PHY address: 0x05	**JP30** **JP31** **JP32**
JP36	**ISOLATE mode:** Pull-up = Enable Pull-down (default) = Disable	**JP36**

Table 6. SMII-3 PHY jumper (continued)

Jumper	Description	Default configuration
JP37	**Nway auto-negotiation enable:** Pull-up (default) = Enable auto-negotiation Pull-down = Disable auto-negotiation	● ● **JP37**
JP38	**Speed mode:** Pull-up (default) = 100 Mbps Pull-down = 10 Mbps	● ● **JP38**
JP39	**Duplex mode:** Pull-up (default) = Half duplex Pull-down = Full duplex	● ● **JP39**

By default the external configuration of the SMII-4 Ethernet PHYs is selected as shown in *Table 7*.

Table 7. SMII-4 PHY jumper default settings

Jumper	Description	Default configuration
JP43, JP44, JP45	**SMII PHY U21 mode configuration:** Default: JP43-open, JP44-fitted, JP45-open: Set U21 to work as SMII function	● ● **JP43** **JP44** ● ● **JP45**
JP40, JP41, JP42	**SMII PHY U21 address configurations:** Default: JP40-open, JP41-open, JP42-open: Set SMII-4 PHY address: 0x07	● ● **JP40** ● ● **JP41** ● ● **JP42**
JP46	**Isolate mode:** Pull-up = Enable Pull-down (default) = Disable	● ● **JP46**
JP47	**Nway auto-negotiation enable:** Pull-up (default) = Enable auto-negotiation Pull-down = Disable auto-negotiation	● ● **JP47**
JP48	**Speed mode:** Pull-up (default) = 100 Mbps Pull-down = 10 Mbps	● ● **JP48**
JP49	**Duplex mode:** Pull-up (default) = Half duplex Pull-down = Full duplex	● ● **JP49**

By default the initial configuration of the MII Ethernet PHYs is selected as shown in *Table 8.*.

Table 8. Default configuration of the Ethernet PHYs U18, U19, U20 and U21

Function	Default configuration
Auto negotiation	Enabled
10/100 Mbits	100 Mbits selected for auto negotiation advertisement
Half/Full duplex	Full duplex selected for auto negotiation advertisement
Internal Loopback	Disabled
Power down	Disabled (PHY active)
MII/SMII mode	SMII selected

There are two LEDs embedded in each RJ45 connector (J15, J18, J19, J21) which are used to indicate the status of the line:

- The red LEDs: D6, D8, D10, D12 in the connector are driven on continuously when the Ethernet link is established with the counterpart.
- The red LEDs: D5, D7, D9, D11 in the connector blinks when there is TX or RX activity.

The Serial Management Interface (SMI) is part of the SMII interface and is used to transfer management information between MAC and PHY (access to the PHY registers). All these four SMII PHYs use same SMI to configure them.

For the SMII Ethernet PHYs (U18,U19,U20,U21 in SMII mode) to function correctly, it is necessary to clock them with a 125 MHz clock. There are two ways to provide a 125 MHz clock to the devices. The default option is to use oscillator U2, the other option is to incorporate the CPU board signal PL_CLK2 (from PLL2) which must be configured in the software. In order to switch from the U2 to PLL1, it is necessary to solder a resistor in R2 (33 Ω) resistor and to remove resistor R8.

6.3 USB

The evaluation board supports two USB Host ports (J30) and one USB slave port (J29) compliant with the USB2.0 Spec. ECHI and OCHI modes are available and supported.

6.4 RS232

There are six UARTs on the board. UART0 and UART1 use DB9 connectors P2 and P3., UART2, UART3, UART4 and UART5 use 3-pin connectors (P4,P5,P6,P7).

UART0 features two modes: using either the full modem control signals or only RX/TX signals

In full modem mode, it uses the U33, U34 RS232 transceivers fully. In this case, use six jumpers to connect the J31 connector: 1<->2, 3<->4,5<->6,7<->8,9<->10,11<->12, so then the UART3, UART4 and UART5 functions are disabled. When it uses only RX/TX signals, it uses only the U34 RS232 transceiver.

UART1 features only RX/TX functionality. It uses the RS232 transceiver at U32.

UART2 features only RX/TX functionality. It uses the RS232 transceiver at U32 and its RS232_2 signals are available on the P4 connector.

UART3 features only RX/TX functionality. It uses the RS232 transceiver at U33 and its RS232_2 signals are available on the P5 connector.

UART4 features only RX/TX functionality. It uses the RS232 transceiver at U33 and its RS232_2 signals are available on the P6 connector.

UART5 features only RX/TX functionality. It uses the RS232 transceiver at U34 and its RS232_2 signals are available on the P7 connector.

Do not install jumpers in J31 when UART3, UART4 and UART5 are enabled and used.

6.5 HDLC-RS485

There are two HDLC-RS485s on the board, they are connected to RS485 transceiver (U16 and U60) and use DB9 connectors (P1 and P8).

HDLC-RS485 features the half-duplex communication, RXD and TXD single-end signals are connected to one RS485 transceiver, by enabling CTS function, it can detect and avoid all the possible bus conflict.

For the correct functionality of the HDLC-RS485, it is necessary to clock them by external clock (TCLK, RCLK), the maxim clock frequency is 3.88MHz, There are two ways to deliver the clocks to CPU. The default option is to use on-board clocks (819.2KHz) that are generated by U38 CPLD.

By default the on-board clock configuration of HDLC-RS485-1 is selected as shown in *Table 9*.

Table 9. HDLC-RS485-1 on-board clock jumpers

Jumper	Description	Configuration
JP65	Supply on-board clocks or external clocks to CPU for HDLC-RS485-1 TCLK. (Default - fitted) to use on board clocks (PIN-1)	
JP66	Supply on-board clocks or external clocks to CPU for HDLC-RS485-1 RCLK. (Default - fitted) to use on board clocks (PIN-1)	

By default the on-board clock configuration of HDLC-RS485-2 is selected as shown in *Table 10*.

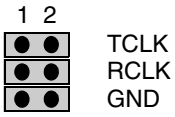
Table 10. HDLC-RS485-2 on-board clock jumpers

Jumper	Description	Configuration
JP62	Supply on-board clocks or external clocks to CPU for HDLC-RS485-2 TCLK. (Default - fitted) to use on board clocks (PIN-1)	
JP63	Supply on-board clocks or external clocks to CPU for HDLC-RS485-2 RCLK. (Default - fitted) to use on board clocks (PIN-1)	

The other option is to use the external clock signals, it is necessary to remove jumpers on J65,J66,J62,J63, and then plug the related clock signals cables to connectors: JP65,JP66, JP67, JP62,JP63,JP64.

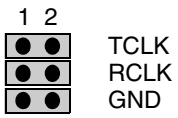
By default the external clock configuration of HDLC-RS485-1 is selected as shown in *Table 11*.

Table 11. HDLC-RS485-1 external clock jumper settings

Jumper	Description	Configuration
JP65	Supply on-board clocks or external clocks to CPU for HDLC-RS485-1 TCLK. Setting: to use external clocks (PIN-2)	
JP66	Supply on-board clocks or external clocks to CPU for HDLC-RS485-1 RCLK. Setting: to use external clocks (PIN-2)	
JP67	Signal Ground	

By default the external clock configuration of HDLC-RS485-2 is selected as shown in *Table 12*.

Table 12. HDLC-RS485-2 external clock jumper settings

Jumper	Description	Configuration
JP62	Supply on-board clocks or external clocks to CPU for HDLC-RS485-2 TCLK. Setting: to use external clocks (PIN-2)	
JP63	Supply on-board clocks or external clocks to CPU for HDLC-RS485-2 RCLK. Setting: to use external clocks (PIN-2)	
JP64	Signal Ground	

6.6 HDLC-E1/TDM

There is one HDLC-E1/TDM on the board, it features two modes: HDLC-E1 and HDLC-TDM.

For HDLC-E1 mode, it uses E1 PHY(U6, DS21354) to communicate with other boards or systems, the connectors are J4 (E1-Receiver), J2 (E1-Transmit) and J3 (RJ48 includes TXD/RXD). The software has to read and write to the E1 PHY registers via the EMI bus to initialize, configure and control the E1 PHY.

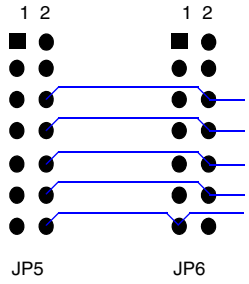
For HDLC-E1 mode to function properly, it is has to be driven by the external clocks (TCLK, RCLK) and external sync (RSYNC,TSYNC). The clock frequency is 2.048 MHz, the sync frequency is 8 kHz. The default setting is to use the on-board clocks and syncs that are generated by the E1 PHY (U36).

For HDLC-TDM mode, no PHY is required and the 128 time slot TDM signals are transmitted to and received from other boards or systems via the J5 connector. For HDLC-TDM mode to function properly, it is has to be driven by the external clocks (TCLK, RCLK) and external sync (RSYNC,TSYNC). The clock frequency is 8.192 MHz, the sync frequency is 8 kHz.

There are two ways to deliver the clocks and syncs to the SPEAr. The default option is to use the on-board clocks (8.192 MHz) and syncs (8 kHz) that are generated by the U38 CPLD, in this case, it act as TDM master. At the same time, it can also provide these source clocks and syncs to other TDM slave boards or systems.

By default the on-board clocks and sync configuration of HDLC-TDM is selected as shown in *Table 13*

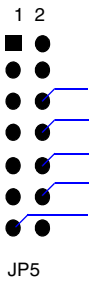
Table 13. HDLC-TDM master on-board clock settings

Jumper	Description	Configuration
JP6	Supply on-board clocks and syncs Default: output TDM_RSYNC(JP6-6), TDM_RCLK(JP6-8), TDM_TSYNC(JP6-10) and TDM_TCLK(JP6-12) TDM_RCLK,TDM_TCLK: 8.192MHz TDM_RSYNC, TDM_TSYNC: 8 kHz JP5-13 and JP6-13 are ground.	
JP5	Receive clocks and syncs to SPEAr for HDLC-TDM. Default: input TDM_RSYNC(JP5-6), TDM_RCLK(JP5-8), TDM_TSYNC(JP5-10) and TDM_TCLK(JP5-12,) Red wire: connect JP6 to JP5 Blue wire: output clocks and syncs to others slave boards	
JP5-2	Input HDLC-TDM RXD to SPEAr, it needs to be connected to the TXD signal of other HDLC-TDM slave boards.	
JP5-4	Output HDLC-TDM TXD from SPEAr to RXD signal of other HDLC-TDM slave boards.	

The other option is to use the external clock and sync signals, in this case, it act as TDM slave, it is necessary to remove connection between JP5 with JP6, and then plug the related external clock and sync signals cables to connectors: JP5.

By default the external clocks and syncs jumpers configuration of HDLC-TDM slave is selected as shown in *Table 14*

Table 14. HDLC-TDM slave external clock and sync settings

Jumper	Description	Configuration
JP5	Receive clocks and syncs to CPU for HDLC-TDM from external boards. Default: input TDM_RSYNC(JP6-6), TDM_RCLK(JP6-8), TDM_TSYNC(JP6-10) and TDM_TCLK(JP6-12) TDM_RCLK,TDM_TCLK: 8.192MHz TDM_RSYNC, TDM_TSYNC: 8KHz JP5-13 is ground. Red wire: input clocks and syncs from other HDLC_TDM slave boards	
JP5-2	Input HDLC-TDM RXD to CPU, it needs to be connected to TXD signal of other HDLC-TDM slave boards.	
JP5-4	Output HDLC-TDM TXD from CPU to RXD signal of other HDLC-TDM slave boards.	

6.7 General purpose ADC connector

Eight analog input lines are available on J27 connector. Inside the connector it is also possible to determine the range of the conversion by setting the conversion limits on the pin J27-19 (lower limit) and J27-1 (upper limit) via jumpers.

By default the on-board VREFP and VREFN jumper configuration of ADC is selected as shown in *Table 15*.

Table 15. General ADC reference voltage settings

Jumper	Description	Configuration
J27-1 J27-2	Connects the +2V5_ADC on-board ADC supply voltage to the ADC_VREFP pin of the CPU board (Default)	
	Connects the external ADC application supply voltage to the ADC_VREFP pin J27-1 of the CPU board	
J27-19 J27-20	Connects the application board GND of the ADC supply voltage domain to the ADC_VREFN pin of the CPU board (Default)	
	Connects the external ADC application GND (lower limit) supply voltage to the ADC_VREFN pin J27-19 of the CPU board	

The following relationship between the pins should be guaranteed in the application:

0V ≤ J27-19 ≤ J27-3 - J27-17 ≤ J27-1 ≤ +2.5V

GND ≤ ADC_VREFN ≤ AIN0 -AIN7 ≤ ADC_VREFP ≤ +2V5ADC

6.8 NOR Flash

The NOR Flash is connected to the EMI interface of CPU, two NOR Flash (U7,U10) are available on the board, the bit-width is 32-bit, the current memory size is 128Mbit. The 32bit NOR Flash is mapped to memory space of CPU, use Jumpers (JP1,JP2,JP3,JP4,JP5,JP6) to select one of six memory space.

By default the memory space mapping of NOR Flash is selected as shown in *Table 16*

Table 16. Memory space map jumpers of NOR Flash

Jumper	Description	Configuration
JP1	NOR Flash is mapped to EMI CSn0 memory space: 0x50000000	
JP2	Nor Flash is mapped to EMI CSn1 memory space: 0x60000000	

Table 16. Memory space map jumpers of NOR Flash (continued)

Jumper	Description	Configuration
JP3	NOR Flash is mapped to EMI CSn2 memory space: 0x70000000	
JP4	NOR Flash is mapped to EMI CSn3 memory space: 0x80000000	
JP5	NOR Flash is mapped to EMI CSn4 memory space: 0x90000000	
JP6	NOR Flash is mapped to EMI CSn5 memory space:	

6.9 NAND Flash

The NAND Flash is connected to the EMI interface of CPU, one NAND Flash (U4) is available on the board, the bit-width is 8-bit, and the current memory size is 8GMbit.

6.10 Serial NOR Flash

There are two serial NOR Flash, one Serial NOR Flash (U26) is connected to the SMI interface of CPU, the bit-width is 8-bit, and the current memory size is 64Mbit; the another serial NOR FLASH (U29) is connected to the SPI interface of CPU, the bit-width is 8-bit, and the current memory size is 4Mbit.

6.11 Parallel NOR Flash

There are two Parallel NOR FLASH (U7, U10) connected to the EMI interface of CPU, the bit-width is 32-bit, and the current memory size is 128Mbit.

6.12 EEPROM

The EEPROM is connected to the I2C interface of CPU, one EEPROM (U28) is available on the board, the bit-width is 8-bit, and the current memory size is 4Kbit.

6.13 DDR2 SDRAM

The DDR2 SDRAM is connected to the DDR2 interface of CPU, one DDR2 SDRAM (U23) is available on the board, the bit-width is 16-bit, and the current memory size is 1Gbit.

6.14 CPLD

The board includes a XILINX CPLD (U38) that implement E1 PHY initial configuration, HDLC-RS485 on-board clocks generation, HDLC-TDM on-board clocks/syncs generation and timing matching for CPU EMI bus to access E1 PHY internal registers.

J8 is the connector for CPLD JTAG emulator to download programming file.

6.15 LEDs

There are 2 general purpose LEDs (D33,D34) available on the left side of the board. All LEDs are driven on when the related CPLD IO pin is driven high.

GPIO59 (D33), GPIO58 (D34)

6.16 Reset button

A manual reset button (SW1) is available on the board's right side.

6.17 Debug Interface

A debug interface is provided:

The JTAG interface provides "static" debug capability. This means that it is possible to set a breakpoint and, when the system stops, to verify the contents of the memory and/or registers and modify them if needed.

6.18 Power supply

This block, receiving 5V from an external AC/DC regulator will provide all the

Voltage needed that are:

- 1.2V (Switching regulator PM6641) to supply the internal logic of SPEAr310
- 1.8V (Switching regulator PM6641) for the DDR2memory
- 2.5V (LDO 1117A regulator) for the analog portion of SPEAr310
- 3.3V (Switching regulator PM6641) to supply the other interfaces

The board is protected against over voltage by U61 (STBP120DVDK6F).

A power monitor is also present to provide the general reset for the board.

6.19 Jumper settings

Table 17. SW3 (SoC functional configuration)

Bit	Description
1	Test0 - refer to the table below for the configuration settings
2	Test1 - refer to the table below for the configuration settings
3	Test2 - refer to the table below for the configuration settings
4	Test3 - refer to the table below for the configuration settings
5	Test4 - refer to the table below for the configuration settings
6	BootSel - refer to the table below for the configuration settings

Table 18. SW3 (debug configuration)

Test bit		Description
1	2	
0	0	Normal Mode (No debug enabled)
0	1	ARM1 JTAG connected to J26
1	0	The ARM ETM bus available, but not linked out on this board.

Table 19. SW3 (functional configuration)

Test bit				Description
6	5	4	3	
1	0	1	1	Configuration 3

Bits 3, 4, and 5 allow you to set the Functional configuration. The default configuration is Configuration 3.

Table 20. SW2 strapping options

SW2-x	Description	Settings	
SW2_1	Little/Big endian	0	Little endian (default)
		1	Big endian
SW2_2	EMI_ACK#	0	ACK enabled
		1	GPIO
SW2_3	NAND bus width	0	8-bit NAND Flash
		1	16-bit NAND Flash

Table 20. SW2 strapping options (continued)

SW2-x	Description	Settings			
SW2_4 SW2_5	NOR Flash bus width	**SW2_4**	**SW2_5**		
		0	0		8-bit NOR Flash
		0	1		16-bit NOR Flash
		1	0		32-bit NOR Flash
SW2_6 SW2_7 SW2_8	Boot device	**SW2_6**	**SW2_7**	**SW2_8**	
		0	0	0	Serial Flash
		0	0	1	NOR Flash
		0	1	0	NAND Flash
		0	1	1	USB

Note: When DIP switch SW2-X is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.

7 Connectors

7.1 MPU JTAG connector

Figure 4. MPU JTAG connector

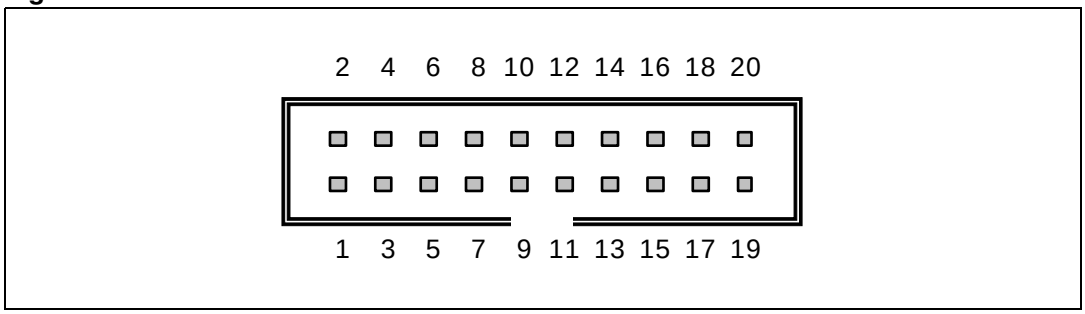


Table 21. MPU JTAG connector pin assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+3V3	6	GND	11	NC	16	GND
2	+3V3	7	TMS	12	GND	17	NC
3	nTRST	8	GND	13	TDO	18	GND
4	GND	9	TCK	14	GND	19	NC
5	TDI	10	GND	15	NC	20	NC

7.2 CPLD JTAG connector

Figure 5. CPLD JTAG connector

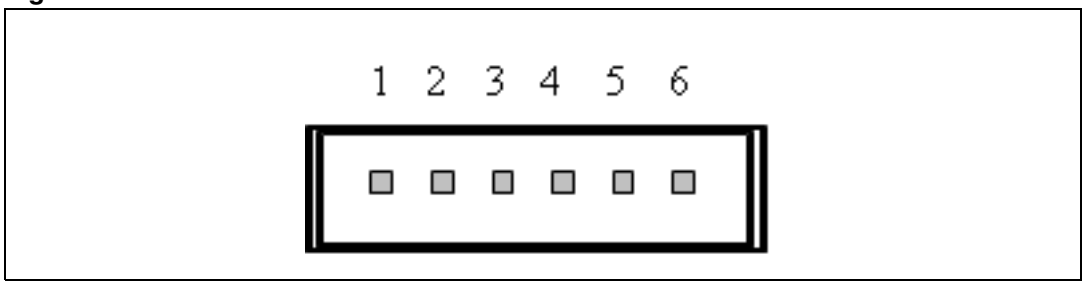


Table 22. CPLD connector pin assignment

Pin	Signal	Pin	Signal	Pin	Signal
1	+3V3	3	TCK	5	TDI
2	+GND	4	TDO	6	TMS

7.3 TDM master connector J5

This connector is the TDM interface for SPEAr310 TDM HDLC controller.

Figure 6. TDM master connector J5

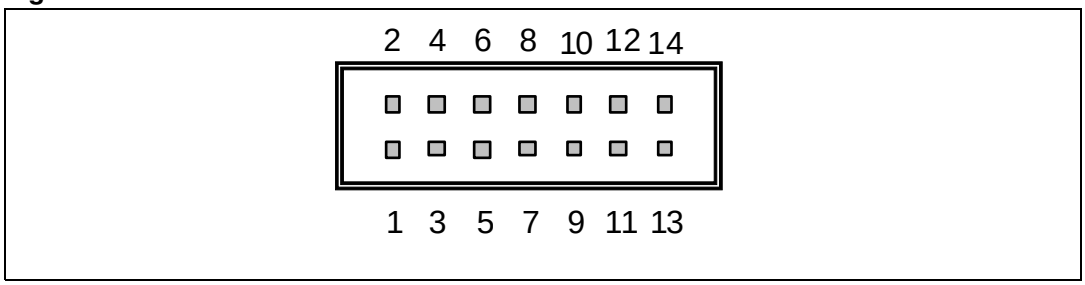


Table 23. TDM master connector J5 pin assignments

Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	TDM_RSYNC	11	GND
2	TDM_RXD	7	GND	12	TDM_TCLK
3	GND	8	TDM_RCLK	13	GND
4	TDM_TXD	9	GND	14	N.C
5	GND	10	TDM_TSYNC		

7.4 TDM slave connector J6

This connector provides TDM clock and sync signals to master interface.

Figure 7. TDM slave connector J6

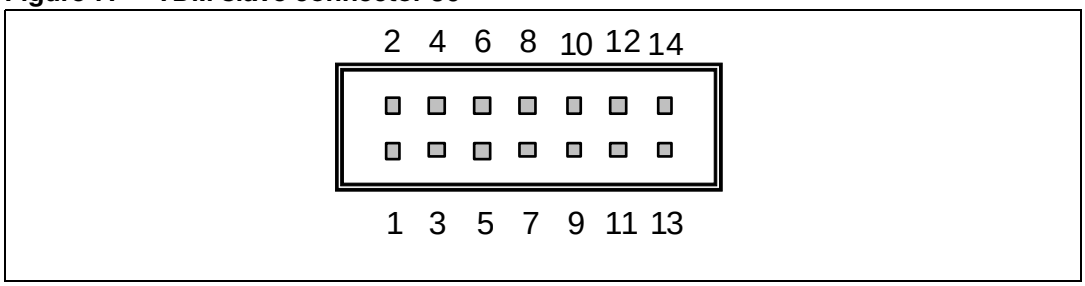


Table 24. TDM slave connector J6 pin assignments

Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	TDM_RSYNC	11	GND
2	N.C	7	GND	12	TDM_TCLK
3	GND	8	TDM_RCLK	13	GND
4	N.C	9	GND	14	N.C
5	GND	10	TDM_TSYNC		

7.5 Ethernet RJ45 connectors J15, J18, J19, J21, U25

J15, J18, J19, J21 is for SMII Ethernet.

U25 is for MII Ethernet.

Figure 8. Ethernet RJ45 connectors J15, J18, J19, J21, U25 - front view

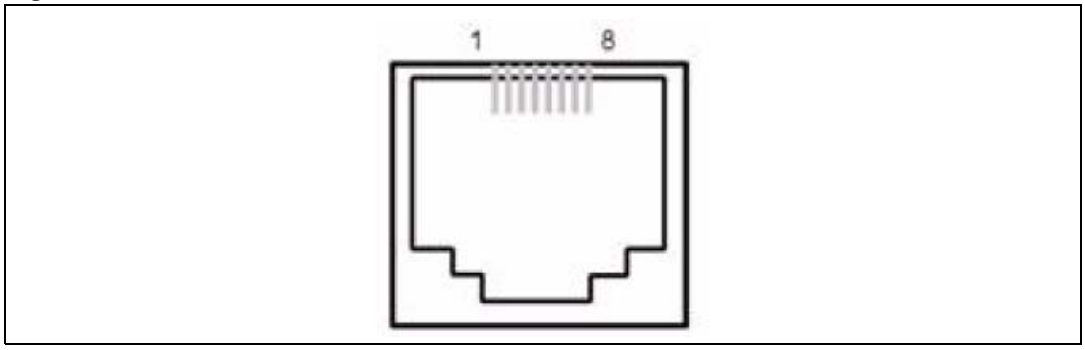


Table 25. RJ45 connectors J15, J18, J19, J21, U25

Pin number	Description	Pin number	Description
1	TxData+	2	TxData-
3	RxData+	4	NC
5	NC	6	RxData-
7	NC	8	NC

7.6 General purpose ADC connector J27

Figure 9. General purpose ADC connector J27

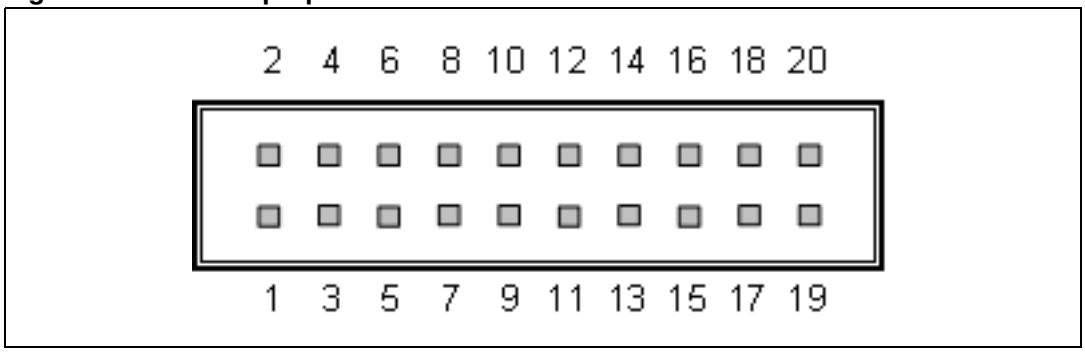


Table 26. General purpose ADC connector J27

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	ADC VREF POSITIVE	6	GND	11	AIN4	16	GND
2	+2V5	7	AIN2	12	GND	17	AIN7
3	AIN0	8	GND	13	AIN5	18	GND

Table 26. General purpose ADC connector J27 (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
4	GND	9	AIN3	14	GND	19	ADC VREF NEGTIVE
5	AIN1	10	GND	15	AIN6	20	GND

7.7 General purpose GPIO connector J25

Figure 10. General purpose GPIO J25

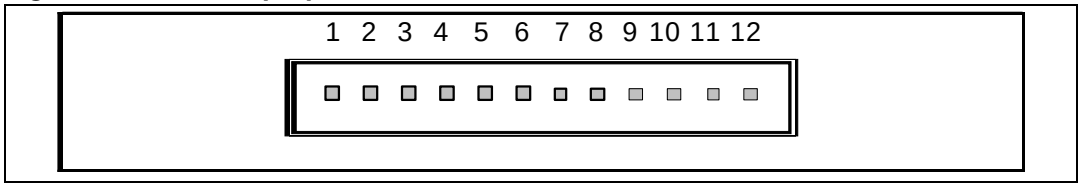


Table 27. General purpose GPIO J25

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+3V3	4	basGPIO2	7	basGPIO5	10	TXD0
2	basGPIO0	5	basGPIO3	8	TXD2	11	TX_CLK
3	basGPIO1	6	basGPIO4	9	TXD1	12	GND

7.8 RS485 DB9 socket P1, P8

Figure 11. RS485 DB9 socket connector P1, P8

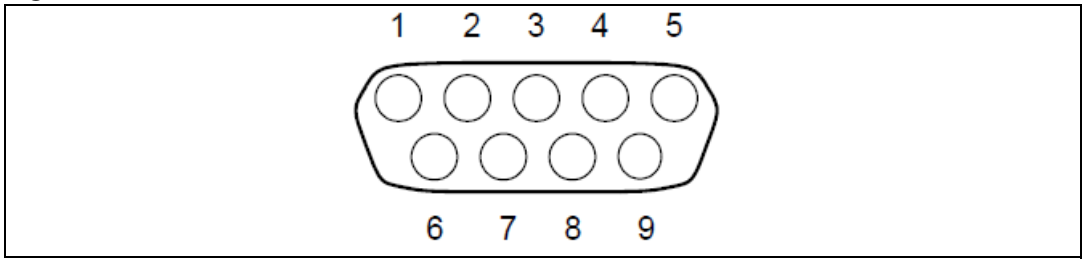


Table 28. RS485 DB9 socket connector P1, P8

Pin number	Description	Pin number	Description
1	NC	6	NC
2	NC	7	A
3	NC	8	B
4	NC	9	NC
5	GND		

7.9 RS232/UART0 DB9 plug connector P2

Figure 12. RS232/UART0 DB9 plug connector P2

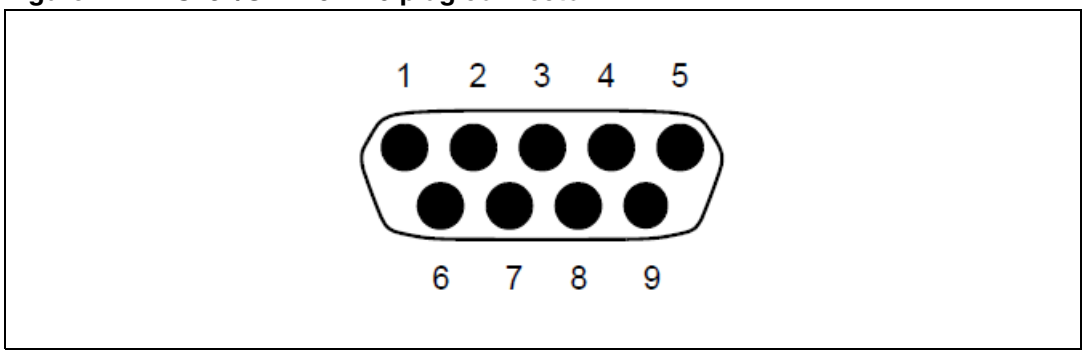


Table 29. RS232/UART0 DB9 plug connector P2

Pin number	Description	Pin number	Description
1	UART0_DCD	6	UART0_DSR
2	UART0_RX	7	UART0_RTS
3	UART0_TX	8	UART0_CTS
4	UART0_DTR	9	UART0_RI
5	GND		

7.10 RS232/UART1 DB9 plug connector P3

Figure 13. RS232/UART1 DB9 plug connector P3

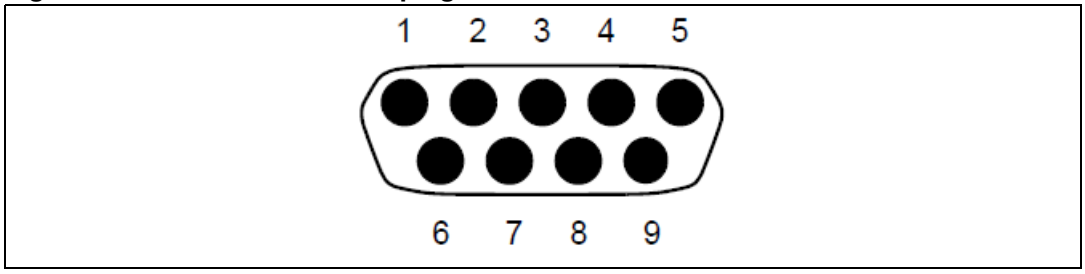


Table 30. RS232/UART1 DB9 plug connector P3

Pin number	Description	Pin number	Description
1	NC	6	NC
2	UART1_RX	7	NC
3	UART1_TX	8	NC
4	NC	9	NC
5	GND		

7.11 RS232/UART2,3,4,5 connector P4,P5,P6,P7

Figure 14. RS232/UART2,3,4,5 connector P4,P5,P6,P7

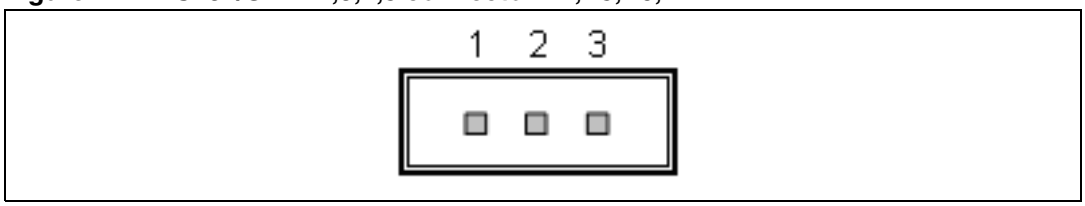


Table 31. RS232/UART2, 3, 4, 5 connector P4, P5, P6, P7

Pin number	Description	Pin number	Description
1	TXD	3	GND
2	RXD		

7.12 BNC plug connector J2

This connector is the output stream for E1.

7.13 BNC plug connector J4

This connector is the input stream for E1.

8 Evaluation board bill of materials (BOM)

Table 32. SPEAr310 bill of materials (BOM)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
1	Capacitor/100 nF/16 V/ 10%/SC0603/X7R			119	C1, C2, C3, C4, C6, C7, C8, C9, C10, C14, C15, C16, C17, C18, C19, C20, C21, C24, C25, C26, C29, C32, C40, C52, C54, C55, C56, C61, C62, C64, C65, C66, C68, C69, C70, C73, C79, C80, C82, C83, C84, C86, C87, C88, C94, C95, C97, C98, C99, C101, C102, C103, C109, C110, C112, C113, C114, C116, C117, C118, C120, C123, C124, C125, C126, C127, C128, C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C139, C140, C143, C146, C147, C148, C149, C150, C154, C155, C156, C158, C160, C161, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C209, C210, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C655	0.1uF-0603
2	Capacitor/1 uF/16 V/10 %/SC1206/X7R			1	C5	1uF-1206
3	Capacitor/10 uF/16 V/1 0%/SC1206/X7R	CL31F106ZPA E	SNMSUNG	12	C23, C31, C33, C34, C35, C36, C39, C43, C44, C51, C53, C657	10uF-1206
4	Capacitor/33 nF/16 V/1 0%/SC0603/X7R			1	C27	33nF-0603
5	Capacitor/100 uF/25 V/ 100%/0.9 ohm/NO/STC 7343/Tan/RoHS	TAJD107K025 RNJ	AVX	1	C28	100u-TAJ-R

Table 32. SPEAr310 bill of materials (BOM) (continued)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
6	Capacitor/22 uF/25 V/20%/1.4 ohm/NO/STC6032/Tan/RoHS	TAJC226M025RNJ	AVX	13	C30, C58, C67, C71, C76, C85, C89, C91, C115, C119, C229, C235, C237	22uF-TAJ-R NO POP
7	Capacitor/470 pF/SC0603/X7R(X5R, Y5V, C0G)	CL10B471KBNC	SNMSUNG	1	C37	470pF-0603
8	Capacitor/22 nF/10 V/10%			3	C38, C41, C42	22nF-0603
9	Capacitor/2.2 nF/NO/NO/SC0603	CL 10B222KBNC	SNMSUNG	1	C45	2.2nF-0603
10	Capacitor/47 uF/10 V/20%/1.2 ohm/NO/STC6032/Tan/	TCSCS1A476MCAR	SNMSUNG	4	C46, C50, C72, C656	47uF-TAJ-R
11	Capacitor/220 uF/16 V/20%/0.5 ohm/NO/STC7343/Tan/	TAJE227M016RNJ	AVX	2	C48, C658	220uF-TAJ-R
12	Capacitor/10 uF/25 V/20%/NO/NO/STC6032/Tan/			25	C57, C75, C90, C100, C104, C105, C106, C206, C207, C208, C222, C224, C225, C226, C228, C230, C231, C232, C233, C234, C236, C238, C239, C240, C241	10uF-TAJ-R
13	Capacitor/1 nF/2 kV/NO/SC1206/NO			10	C59, C60, C77, C78, C92, C93, C107, C108, C244, C245	1000pF-1206
14	Capacitor/100 pF/NO/NO/SC0603/NO	CL10C101JBNC	SNMSUNG	4	C63, C81, C96, C111	100pF-0603
15	Capacitor/22 uF/25 V/20%/1.4 ohm/NO/STC6032/Tan/	TAJC226M025RNJ	AVX	1	C74	22uF-TAJ-R
16	Capacitor/15 pF/50 V/5%/SC0603/COG			4	C141, C142, C151, C152	15PF-0603
17	Capacitor/10 pF/NO/NO/SC0603/	CL10C100JBNC	SNMSUNG	2	C144, C145	10PF-0603
18	Capacitor/33 pF/NO/NO/SC0603/	CL10C330JBNC	SNMSUNG	2	C153, C157	33PF-0603
19	Capacitor/10 nF/NO/NO/SC0603/X7R(X5R, Y5V, C0G)	CL10B103KB8NNNC	SNMSUNG	2	C159, C191	0.01uF-0603

Table 32. SPEAr310 bill of materials (BOM) (continued)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
20	Capacitor/100 nF/10 V/ 10%/SC0402/X5R			24	C162, C163, C164, C165, C166, C167, C168, C169, C170, C171, C172, C173, C174, C175, C176, C177, C178, C179, C180, C181, C182, C183, C184, C185	0.1uF-0603
21	Capacitor/10 uF/25 V/2 0%/NO/NO/STC6032/T an			4	C223, C227, C242, C243	10uF-TAJ-R NO POP
22	LED/GREEN/SLED080 5			15	D1, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34	GREEN
23	LED/RED/SLED0805			14	D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D17, D19, D20	RED
24	Diode/70V/200 mA/ 250 mW/SOT23/RoHS	BAV70		1	D16	BAV70
25	Diode/600/4 A/ 200 mW/DPAK/RoHS	TS420-600B	ST	1	D35	SCR TS420-B_1
26	Header/single row/short/vertical/2.54 mm pin pitch header	1x2		52	JP1, JP2, JP3, JP4, JP5, JP6, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP20, JP21, JP22, JP23, JP24, JP25, JP26, JP27, JP28, JP29, JP30, JP31, JP32, JP33, JP34, JP35, JP36, JP37, JP38, JP39, JP40, JP41, JP42, JP43, JP44, JP45, JP46, JP47, JP48, JP49, JP62, JP63, JP64, JP65, JP66, JP67	J-JMPR-2PIN
27	Connector/SMA/Vertica l/TH			1	J1	SMA NO POP
28	Connector/BNC 75 ohm/5-pin/1.29 mm pitch/RA/TH	5413558-1	Tyco	2	J2, J4	BNC-5PIN
29	RJ45/no LED/1.27 mm pitch/8-pin/RA/TH	5621-1x1	Hesheng	1	J3	CONN_RJ48

Table 32. SPEAr310 bill of materials (BOM) (continued)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
30	Header/dual row/short/vertical/2.54 mm pin pitch	2x7		2	J5, J6	HEADER2X7
31	Header/single row/short/vertical/2.54 mm	1x6		1	J8	CON6
32	RJ45/no LED/1.27 mm pitch/8-pin/RA/TH	5621-1x1	Hesheng	4	J15, J18, J19, J21	RJ45x4_8
33	transformer/1:1/10/100 base-T/sop16-50-370	H1102	Pulse	4	J16, J17, J20, J22	H1102
34	Header/single row/short/vertical/2.54 mm pin pitch header	1x12		1	J25	CON12_0
35	IDC 10x2/100 mil-pitch/shrouded/vertical/ TH	HL0705F	Foxconn	1	J26	IDC10X2
36	Header/dual row/short/vertical/2.54 mm pin pitch	2x10		1	J27	CON20A
37	TYPE B USB CONNECTOR	amp-787924	AMP	1	J29	USB_DEV
38	TYPE A DUAL USB CONNECTOR/RA/TH	tyco-5787617	Tyco	1	J30	USB_HOST_CON
39	Header/dual row/short/vertical/2.54 mm pin pitch	2x6		1	J31	JUMP2X6
40	Inductor/1 uH/2.76 A/20 %/3.9x3.9/	GSCD43-1R0	genericsz	1	L1	LPS4012-102NL
41	Inductor/2.2 uH/1.75 A/ 20%/3.9x3.9	GSCD43-2R2	genericsz	2	L2, L3	LPS4012-222ML
42	Bead/3000 mA/75 ohm/ 0.025 ohm/SL1806	BLM41PG750 SN1L	Murata	21	L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L20, L21, L22, L23, L24, L25, L606	BLM41PG750SN1L
43				1	PD1	PADX2-80H60
44	Connector/D-sub9/male/RA/TH			4	P1, P2, P3, P8	CONNECTOR DB9 Male
45	Header/single row/short/vertical/2.54 mm pin pitch header	1x3		4	P4, P5, P6, P7	CON3

Table 32. SPEAr310 bill of materials (BOM) (continued)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
46	NPN Transistor/30 V/30 V/6 V/ 0.1 A/0.33 W/SOT23	BC848A	Infineon	1	Q4	BC848
47	Resistor Array/33Rohm/63 mW/ 5%/SR0603X4			8	RN1, RN2, RN3, RN4, RN5, RN6, RN7, RN8	33, 1%
48	Resistor/33Rohm/NO/1 %/SR0603/			101	R1, R3, R4, R5, R6, R8, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R36, R37, R38, R39, R40, R41, R69, R70, R71, R74, R75, R76, R127, R128, R130, R134, R135, R136, R154, R157, R158, R159, R189, R192, R193, R194, R224, R227, R228, R229, R259, R262, R263, R264, R367, R368, R369, R372, R374, R389, R401, R500, R501, R502, R503, R504, R505, R506, R507, R508, R509, R510, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R529, R531, R532, R533, R534, R535, R600, R601, R627, R628, R630, R635, R636, R637	33-0603
49	Resistor/33Rohm/NO/1 %/SR0603			8	R2, R9, R370, R371, R373, R393, R402, R403	33-0603-NO POP

Table 32. SPEAr310 bill of materials (BOM) (continued)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
50	Resistor/4K7ohm/NO/1 %/SR0603			47	R7, R77, R78, R79, R80, R82, R83, R84, R137, R141, R155, R161, R162, R163, R164, R165, R167, R172, R177, R190, R196, R197, R198, R199, R201, R202, R207, R210, R225, R231, R232, R233, R234, R236, R237, R242, R245, R260, R266, R267, R268, R269, R271, R272, R359, R404, R901	4.7K-0603
51	Resistor/75Rohm/NO/5 %/SR0603			17	R10, R140, R143, R146, R147, R175, R176, R180, R181, R212, R213, R216, R217, R247, R248, R250, R251	75-0603
52	Resistor/0Rohm/NO/5 %/SR0603			37	R11, R12, R13, R14, R110, R118, R138, R139, R142, R144, R145, R148, R149, R173, R174, R178, R179, R182, R183, R184, R208, R209, R211, R214, R215, R218, R219, R243, R244, R246, R249, R252, R253, R254, R332, R341, R405	0-0603
53	Resistor/61R9ohm/NO/ 1%/SR0603			2	R15, R16	61.9-0603
54	Resistor/51R1ohm/NO/ 1%/SR0603			1	R17	51.1-0603

Table 32. SPEAr310 bill of materials (BOM) (continued)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
55	Resistor/1Kohm/NO/1 %/SR0603			75	R42, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R72, R124, R160, R169, R170, R171, R195, R204, R205, R206, R230, R239, R240, R241, R265, R274, R275, R276, R286, R287, R297, R298, R300, R302, R314, R315, R316, R317, R318, R319, R320, R325, R328, R331, R333, R334, R335, R338, R340, R343, R352, R353, R354, R355, R363, R364, R394, R399, R541	1K-0603
56	Resistor/1Kohm/NO/1 %/SR0603			1	R43	1K-0603-NO POP
57	Resistor/330Rohm/NO/ 1%/SR0603			20	R73, R112, R124, R375, R376, R377, R378, R379, R380, R381, R382, R383, R384, R385, R386, R387, R388, R390, R391, R392	330-0603
58	Resistor/4K7ohm/NO/1 %/SR0603			2	R81, R87	4.7K-0603-NO POP
59	Resistor/4R3ohm/NO/1 %/SR0603			2	R103, R105	4.3-0603
60	Resistor/6 Kohm/NO/1 %/SR0603			7	R106, R107, R108, R109, R116, R117, R119	68k-0603
61	Resistor/150Kohm/NO/ 5%/SR0603			2	R111, R122	150k-0603
62	Resistor/27Kohm/0.063 W/1%			1	R113	27K-0603
63	Resistor/47Kohm/0.063 W/5%			1	R114	47K-0603
64	Resistor/15Kohm/NO/5 %/SR0603			1	R115	15K-0603

Table 32. SPEAr310 bill of materials (BOM) (continued)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
65	Resistor/10Kohm/NO/5 %/SR0603			29	R120, R132, R133, R304, R306, R307, R308, R309, R310, R311, R312, R313, R321, R322, R323, R324, R326, R344, R345, R346, R347, R349, R350, R356, R357, R358, R540, R632, R633	10K-0603
66	Resistor/75Kohm/NO/1 %/SR0603			1	R121	75k-0603
67	Resistor/120Rohm/NO/ 5%/SR0603			6	R126, R129, R131, R626, R629, R631	120-0603
68	Resistor/49R9ohm/NO/ 1%/SR0603			16	R150, R151, R152, R153, R185, R186, R187, R188, R220, R221, R222, R223, R255, R256, R257, R258	49.9-0603
69	Resistor/6K49ohm/NO/ 1%/SR0603			4	R156, R191, R226, R261	6.49K-0603
70	Resistor/220Rohm/NO/ 1%/SR0603			8	R166, R168, R200, R203, R235, R238, R270, R273	220-0603
71	Resistor/121Kohm/NO/ 1%/SR0603			3	R277, R342, R400	121K-0603
72	Resistor/470Rohm/0.06 3W/5%			2	R280, R281	470-0603
73	Resistor/100Rohm/NO/ 1%/SR0603			11	R282, R283, R284, R285, R289, R290, R291, R292, R294, R295, R296	100-0603
74	Resistor/150Rohm/NO/ 5%/SR0603			5	R288, R299, R301, R303, R305	150-0603
75	Resistor/1Mohm/NO/1 %/SR0603			1	R293	1M-0603
76	Resistor/0Rohm/NO/5 %/SR0603			7	R327, R329, R330, R407, R408, R606, R900	0-0603-NO POP
77	Resistor/10Rohm/NO/5 %/SR0603			3	R336, R337, R339	10-0603
78	Resistor/100Kohm/NO/ 5%/SR0603			1	R348	100K-0603

Table 32. SPEAr310 bill of materials (BOM) (continued)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
79	Resistor/390Kohm/NO/ 1%/SR0603			1	R351	390K-0603
80	Resistor/43R2ohm/NO/ 1%/SR0603			1	R360	43.2-0603
81	Resistor/120Kohm/NO/ 1%/SR0603			1	R406	120k
82	Push button/4-pin/6x6 mm/RA/TH	TS6601V	Kingtek	1	SW1	PUSHBUTTOM
83	Slide switch/8 ways/1.27 mm pitch/SMT	CHS-08TB1	COPAL	1	SW2	SW DIP-8
84	Slide switch/6 ways/1.27 mm pitch/SMT	CHS-06TB1	COPAL	1	SW3	SW DIP-6
85	Test terminal/1.02 mm hole/1-pin/TH	20-2137	VERO	11	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP16, TP17, TP19, TP20	TEST_POINT
86	Transformer/Dual ports/1CT:1:0.8/T1/sop 16-50-370	TX1099	PULSE	1	T1	TRANS TX1099
87	Clock driver/3.3V CMOS/1 input 10 output/QSOP20	PI49FCT3807 BQE	Pericom	1	U1	PI49FCT3807BQE+ AMX
88	Oscillator 125 MHz			1	U2	OSC-125MHz
89	CMOS switch/4 ways/QSOP16	QS3125QG	IDT	3	U3, U36, U37	IDTQS3125QG
90	NAND Flash/8 Gbit/8 bit/3.3 V/TSOP48/	NAND08GW3 B2CN6	numonyx/S T	1	U4	NAND08GW3B2CN 6
91	CMOS switch/10 ways/QSOP24	QS3861QG	IDT	1	U5	IDTQS3861QG
92	Transceiver/E1/CEPT/L QFP100	DS21354L	MAXIM	1	U6	DS21354
93	Flash/64 Mbit/16 bit/3.3 V/boot block/TSOP48/	M28W640HC T70N6E	numonyx	2	U7, U10	M28W640HCT
94	D-type latch/16 bit/TSSOP48	74LCX16373T TR	ST	2	U8, U9	74LCX16373TTR
95	Reset IC/3V/SOT143-4/RoHs	STM811SW16 F	ST	1	U11	STM811
96	Buffer/8 bit/TSSOP20	74LCX244TT R	ST	1	U12	74LCX244TTR
97	Switching Power/2.7 V-5.5 V/1.5 V-1.8 V/3.9 A-6.1 A/ QFPN48 7x7	PM6641	ST	1	U13	PM6641

Table 32. SPEAr310 bill of materials (BOM) (continued)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
98	LDO/15 Vmax/2.5 V/1 A/2%/SOT223	LD1117AS25 TR	ST	1	U15	LD1117A
99	Transceiver/RS-485/SO8	ST485CDR	ST	2	U16, U60	ST485C
100	Oscillator 8.192 MHz			1	U17	OSC 8.192MHz
101	Transceiver/100Base-TX PHY/TQFP48	KSZ8041TL	Micrel	4	U18, U19, U20, U21	KSZ8041TL/KSZ8041FTL
102	SPEAr310 LFBGA289	SPEAr310	ST	1	U22	SPEAr310
103	DDR2/1 Gbit/BGA84	MT47H64M16 HR3	Micron	1	U23	MT47H64M16HR
104	Transceiver/100Base-TX PHY/TQFP64	STE100P	ST	1	U24	STE100P_0
105	Connector/RJ45	HR911105A	Hanrun	1	U25	HR911105A
106	Flash/64 Mbit/8 bit/SPI/ 3.3 V/	M25P64-VMF6PT	ST	1	U26	M25P64
107	Battery holder/3 V/220 mAh/ battery-holder-cr2032	CR2032-2-1	Keyu	1	U27	BATT BR2032
108	EEPROM/4 Kbit/8 bit/ I2C	M24C04-WMN6TP	ST	1	U28	M24C04
109	Flash/4 Mbit/8 bit/SPI/ 3.3 V	M25P40-VMN6T	ST	1	U29	M25P40
110	Power MOSFET	ST2052BDR	ST	1	U31	ST2052
	Transceiver/RS-232/SO16	ST3232CDR	ST	3	U32, U33, U34	ST3232CDC
112	Oscillator 2.048 MHz/			1	U35	OSC 2.048MHz
113	CPLD/10 ns/72 user IOs/TQFP100/	XC9572XL-10TQ100C	Xilinx	1	U38	XC9572XL
114	Inverter/1.65 5.5 V	74LVC1G14GW	NXP	2	U40, U41	74LVC1G14
115	Overvoltage protection	STBP120BVDK6F	ST	1	U61	ST STBP120C
116	3-pin power jack diameter 2.1 mm			1	VB1	PWS-JACK
117	Crystal/25 MHz /NO/1HC49			1	Y1	25MHZ
118	Crystal/32.768 kHz/			1	Y2	32.768KHZ
119	Crystal/24MHz/NO/HC 49			1	Y3	24MHZ

Table 32. SPEAr310 bill of materials (BOM) (continued)

Item	Description	Part number	Manu-facturer	Qty	Reference	Part
120	Zener Diode/5.6 V/0.5 A/0.5 W	MMSZ5232BT1	Onsemi	1	Z1	MMSZ5232BT1
121	Bat/3V/220 mAh/CR2032	CR2032	TMMQ	1		
122	LED/RED/SLED0805			2	D2, D3	RED-NO POP
123	Resistor/680Rohm/NO/1%/	SZDZ6201CR0603F680R	ROYALOHM	16	R73, R112, R375, R376, R377, R378, R379, R380, R381, R382, R383, R384, R385, R386, R387, R388	680-0603
124	Resistor/330Rohm/NO/1%/			2	R390, R391	330-0603-NO POP

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Revision history

Table 33. Document revision history

Date	Revision	Changes
27-Oct-2009	1	Initial release.
25-Feb-2010	2	Changed the title of the document. Minor text changes.

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