

# ISL6445 Evaluation Board User Guide

## Hardware Description

The ISL6445EVAL3Z evaluation board is designed to demonstrate the performance of the ISL6445.

The ISL6445 is a high-performance, dual-output PWM controller optimized for converting wall adapter, battery or network intermediate bus DC input supplies into the system supply voltages required for a wide variety of applications. Each output is adjustable down to 0.8V. The two PWMs are synchronized 180° out-of-phase reducing the RMS input current and ripple voltage.

## ISL6445 Reference Design

The ISL6445 evaluation board illustrates the operation of the IC. The design criteria is listed in Table 1.

TABLE 1. DESIGN CRITERIA

PARAMETERS	PACKAGE
Output voltage ( $V_{OUT1}$ )	3.3V
Output current ( $I_{OUT1}$ )	3A
Output voltage ( $V_{OUT2}$ )	2.5V
Output current ( $I_{OUT2}$ )	3A

### Power and Load Connections

If using an input supply ranging from 5.6V to 24V, connect the supply to  $V_{IN}$  (P1) and GND (P2) posts as shown in Figure 1. ISL6445 has an internal +5V linear regulator which can be used to bias the IC.

When using a  $5V \pm 10\%$  input supply, connect the negative polarity to GND (P2) post and connect the positive polarity of the power supply to both  $V_{IN}$  (P1) post and the VCC5 (TP1) post. This will disable the internal LDO and the chip will be powered by the input power supply (see Figure 2).

**CAUTION: Ensure that the +5V terminal is not connected to when applying voltages >7V. This can damage the IC.**

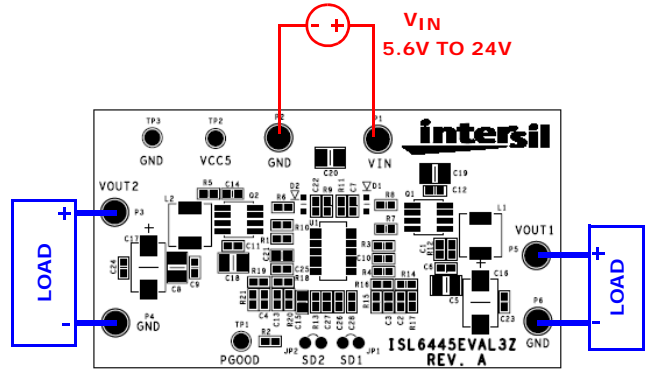


FIGURE 1. POWER AND LOAD CONNECTIONS FOR 5.6V TO 24V INPUT VOLTAGE

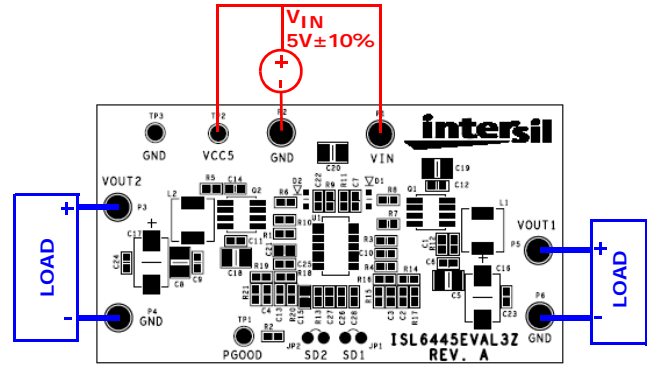


FIGURE 2. POWER AND LOAD CONNECTIONS FOR  $5V \pm 10\%$  INPUT VOLTAGE

### Test-point and Terminals Descriptions

TABLE 2. ISL6445EVAL3Z TEST POINT DESCRIPTION

TEST POINTS AND TERMINALS	SIGNALS
TP1	PGOOD
TP2	VCC5
TP3	GND
P1	VIN
P2	GND
P3	VOUT2
P4	GND
P5	VOUT1
P6	GND

## Typical Performance Curves

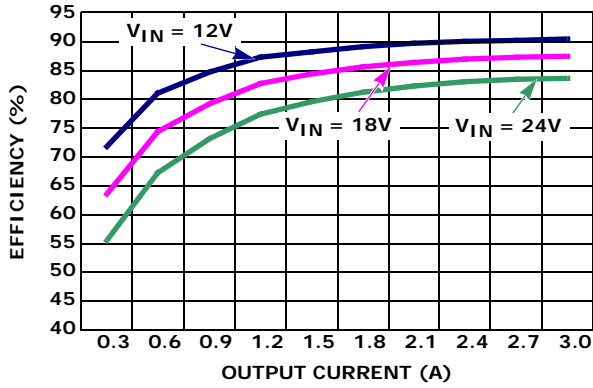


FIGURE 3. EFFICIENCY FOR  $V_{OUT1}$  ( $V_{OUT2}$  IS DISABLED)

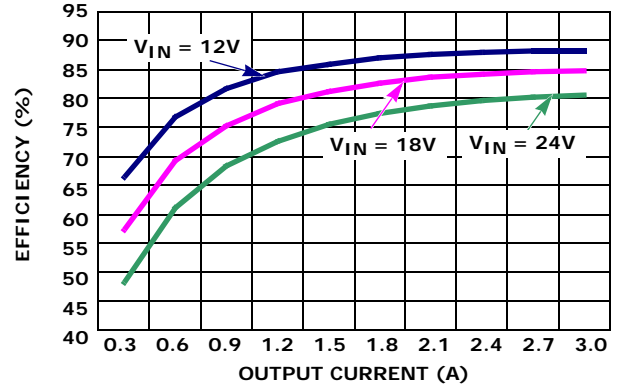


FIGURE 4. EFFICIENCY FOR  $V_{OUT2}$  ( $V_{OUT1}$  IS DISABLED)

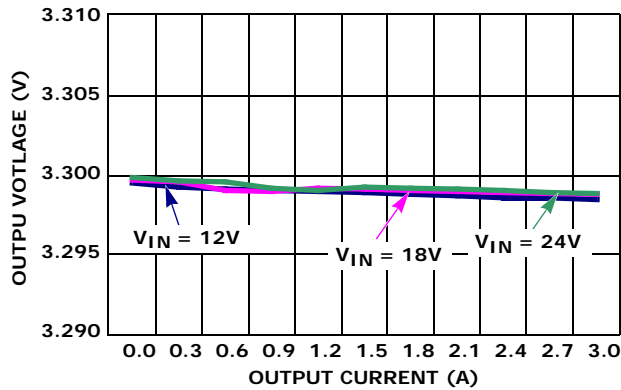


FIGURE 5.  $V_{OUT1}$  (3.3V) REGULATION

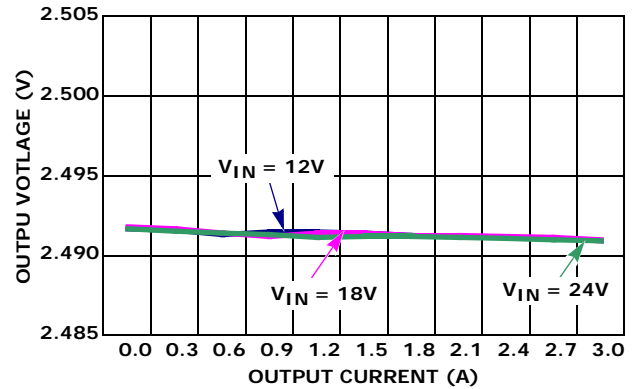


FIGURE 6.  $V_{OUT2}$  (2.5V) REGULATION

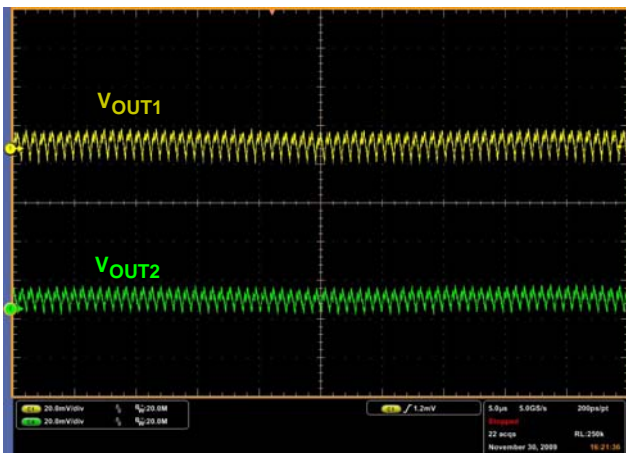


FIGURE 7. OUTPUT RIPPLES AT FULL LOAD (20BW); INPUT VOLTAGE = 12V

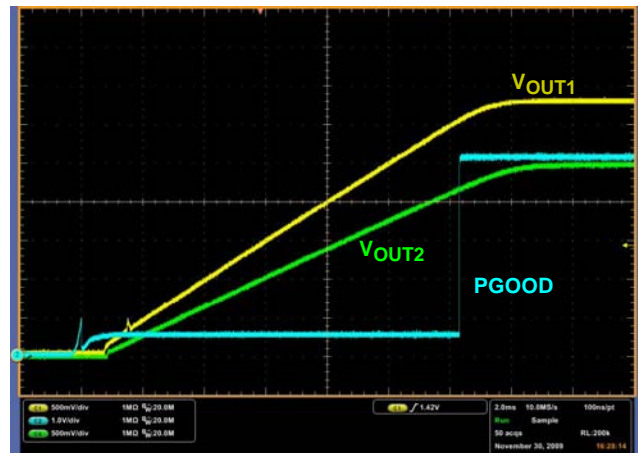


FIGURE 8. SOFT-START WAVEFORMS

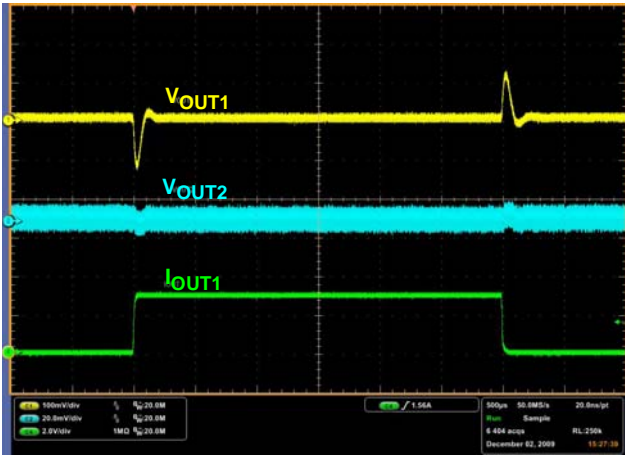


FIGURE 9. LOAD TRANSIENT:  
INPUT VOLTAGE = 12V,  
 $I_{OUT1} = 0A \leftrightarrow 3A$ ,  $I_{OUT2} = 3A$

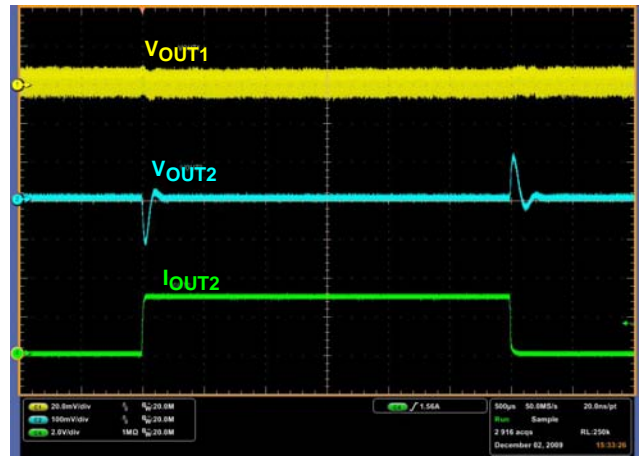


FIGURE 10. LOAD TRANSIENT:  
INPUT VOLTAGE = 12V,  
 $I_{OUT1} = 3A$ ,  $I_{OUT2} = 0A \leftrightarrow 3A$

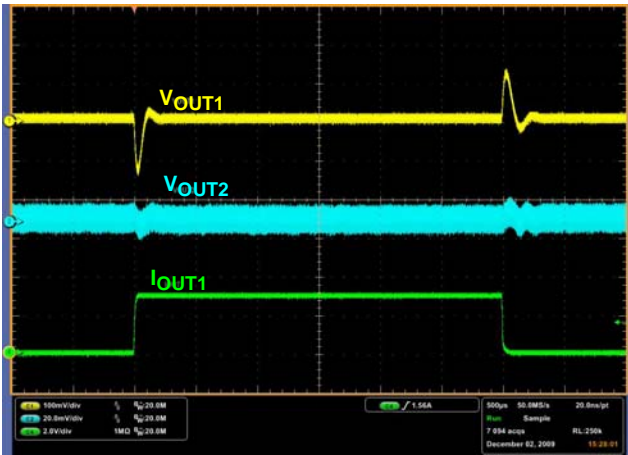


FIGURE 11. LOAD TRANSIENT:  
INPUT VOLTAGE = 18V,  
 $I_{OUT1} = 0A \leftrightarrow 3A$ ,  $I_{OUT2} = 3A$

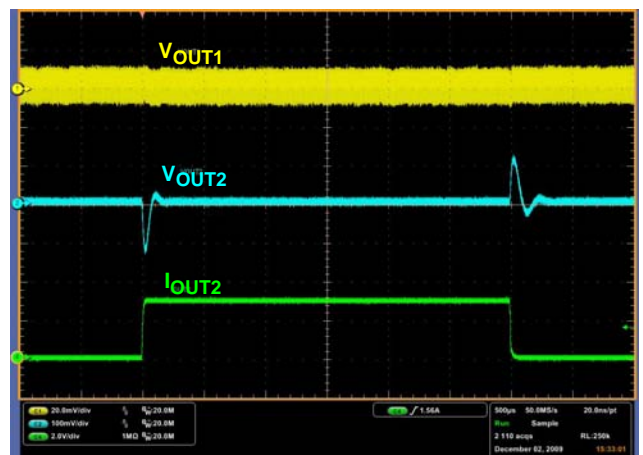


FIGURE 12. LOAD TRANSIENT:  
INPUT VOLTAGE = 18V,  $I_{OUT1} = 3A$ ,  
 $I_{OUT2} = 0A \leftrightarrow 3A$

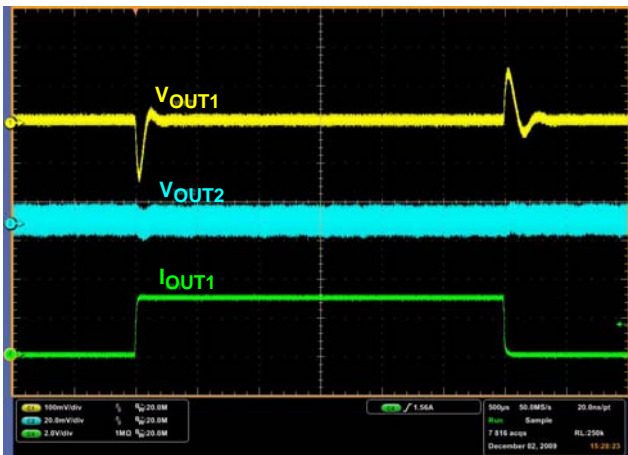


FIGURE 13. LOAD TRANSIENT:  
INPUT VOLTAGE = 24V,  
 $I_{OUT1} = 0A \leftrightarrow 3A$ ,  $I_{OUT2} = 3A$

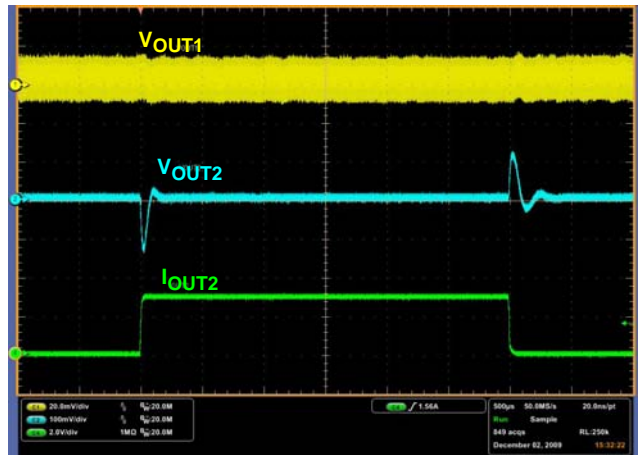
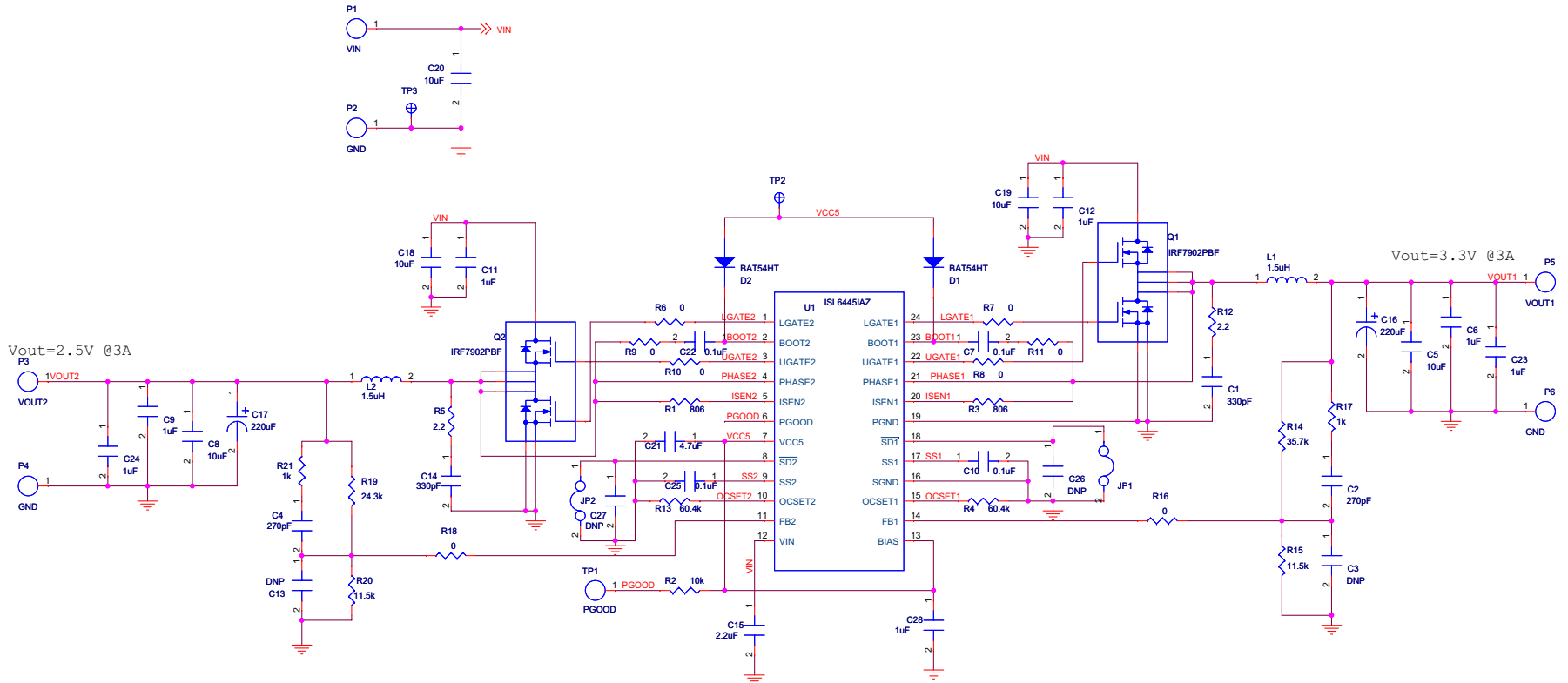


FIGURE 14. LOAD TRANSIENT:  
INPUT VOLTAGE = 24V,  
 $I_{OUT1} = 3A$ ,  $I_{OUT2} = 0A \leftrightarrow 3A$

# ISL6445EVAL3Z Schematic



## ISL6445EVAL3Z Rev. A Bill of Materials

ID	REFERENCE	QTY	PART NUMBER	PART TYPE	DESCRIPTION	PACKAGE	VENDOR
1	U1	1	ISL6445IAZ	Dual PWM Controller	IC, Dual PWM Controller	24 Ld QSOP	Intersil
2	Q1, Q2	2	IRF7902PBF	MOSFET, Dual	Dual 30V N-channel MOSFET	SO-8	International Rectifier
3	D1, D2	2	BAT54HT1G-T	Diode, Schottky	30V, 200mA	SOD-323	On Semi
4	L1, L2	2	FP3-1R5-R	Inductor	1.5 $\mu$ H, 20%, 6.2A	SMD	Coiltronics
<b>CAPACITORS</b>							
5	C1, C14	2		Capacitor, Ceramic, X7R	330pF, 10%, 50V	SM_0603	Various
6	C2, C4	2		Capacitor, Ceramic, X7R	270pF, 10%, 50V	SM_0603	Various
7	C5, C8	2		Capacitor, Ceramic, X5R	10 $\mu$ F, 10%, 16V	SM_1206	Various
8	C6, C9, C11, C12, C23, C24, C28	7		Capacitor, Ceramic, X5R	1 $\mu$ F, 10%, 25V	SM_0603	Various
9	C7, C10, C22, C25	4		Capacitor, Ceramic, X7R	0.1 $\mu$ F, 10%, 50V	SM_0603	Various
10	C15	1		Capacitor, Ceramic, X5R	2.2 $\mu$ F, 20%, 25V	SM_805	Various
11	C16, C17	2	6TPE220MI	Capacitor, POSCAP	220 $\mu$ F, 20%, 6.3V, 0.018 $\Omega$	Case D2E	SANYO
12	C18, C19, C20	3		Capacitor, Ceramic, X7R	10 $\mu$ F, 10%, 25V	SM_1210	Various
13	C21	1		Capacitor, Ceramic, X5R	4.7 $\mu$ F, 10%, 16V	SM_0805	Various
14	C3, C13, C26, C27			Do not populate			
<b>RESISTORS</b>							
15	R1,R3	2		Resistor, Film	806 $\Omega$ , 1%, 1/10W	SM_0603	Panasonic/Generic
16	R2	1		Resistor, Film	10k $\Omega$ , 1%, 1/10W	SM_0603	Panasonic/Generic
17	R4, R13	2		Resistor, Film	60.4k $\Omega$ , 1%, 1/16W	SM_0603	Panasonic/Generic
18	R5, R12	2		Resistor, Film	2.2 $\Omega$ , 1%, 1/10W	SM_0603	Panasonic/Generic
19	R6, R7, R8, R9, R10, R11, R16, R18	8		Resistor, Film	0 $\Omega$ , 1/10W	SM_0603	Panasonic/Generic
20	R14	1		Resistor, Film	35.7k $\Omega$ , 1%, 1/10W	SM_0603	Panasonic/Generic
21	R15, R20	2		Resistor, Film	11.5k $\Omega$ , 1%, 1/10W	SM_0603	Panasonic/Generic
22	R17, R21	2		Resistor, Film	1k $\Omega$ , 1%, 1/10W	SM_0603	Panasonic/Generic
23	R19	1		Resistor, Film	24.3k $\Omega$ , 1%, 1/10W	SM_0603	Panasonic/Generic
<b>OTHERS</b>							
23	P1 - P6	6	1514-2	Turrett Post	Terminal post, through hole, 1/4 inch	PTH	Keystone
24	TP1, TP2, TP3	3	5002	TEST POINT vertical, white	PC test jack	PTH	Keystone
25	JP1, JP2	2	68000-236-1X2	Header	1X2 Break Strip GOLD		

# ISL6445EVAL3Z Printed Circuit Board Layers

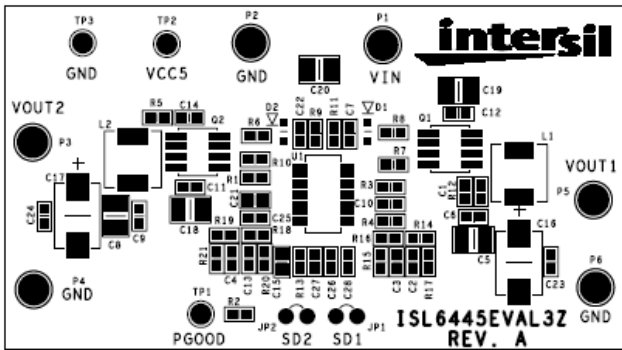


FIGURE 15. ISL6445EVAL3Z - TOP LAYER (SILKSCREEN)

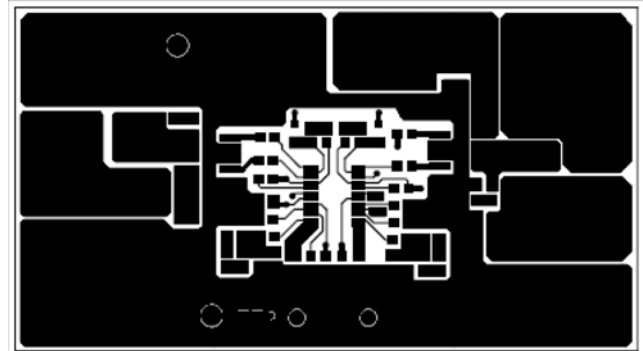


FIGURE 16. ISL6445EVAL3Z - TOP LAYER (COMPONENT SIDE)

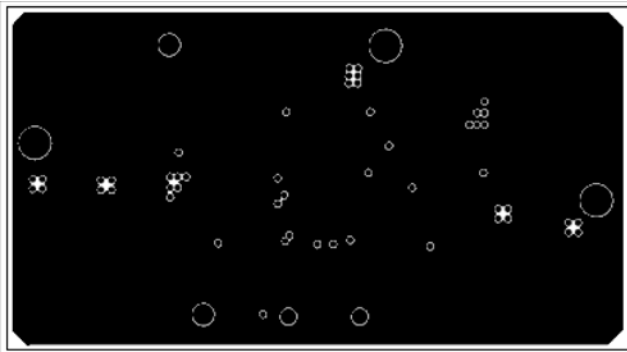


FIGURE 17. ISL6445EVAL3Z - LAYER 2

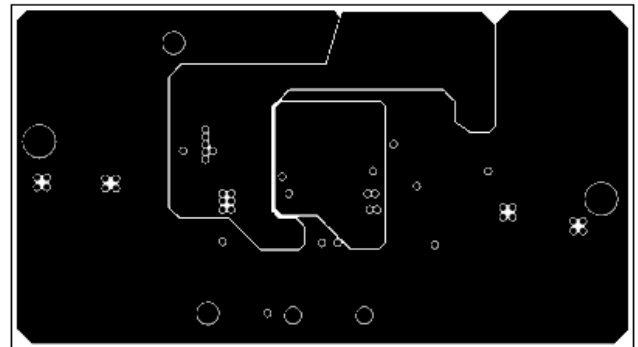


FIGURE 18. ISL6445EVAL3Z - LAYER 3

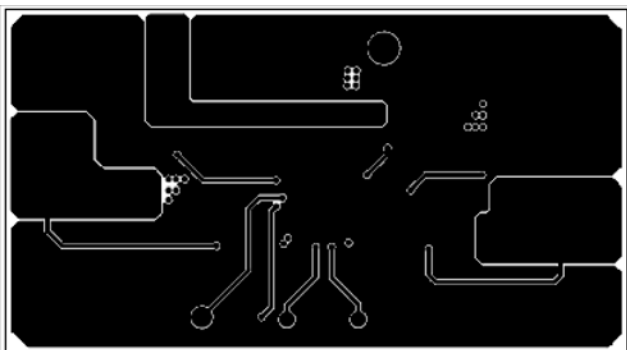


FIGURE 19. ISL6445EVAL3Z - BOTTOM LAYER (SOLDER SIDE)



FIGURE 20. ISL6445EVAL3Z - BOTTOM LAYER (SILKSCREEN)

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