PIC18F2458/2553/4458/4553 Rev. B5 Silicon Errata

The PIC18F2458/2553/4458/4553 Rev. B5 parts you have received conform functionally to the Device Data Sheet (DS39887**B**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2458/2553/4458/4553 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

Note:	The *"PIC18F2458/2553/4458/4553 Data Sheet"* is supplemented by the *"PIC18F2455/2550/4455/4550 Data Sheet"* (DS39632). PIC18F2458/2553/4458/4553 features and specifications that are shared with the PIC18F2455/2550/4455/4550 devices are documented in the *"PIC18F2455/2550/4455/4550 Data Sheet"*.

The following silicon errata apply only to PIC18F2458/2553/4458/4553 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2458	10 1010 011	0 0101
PIC18F2553	10 1010 010	0 0101
PIC18F4458	10 1010 001	0 0101
PIC18F4553	10 1010 000	0 0101

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F2458/2553/4458/4553 silicon.

1. Module: MSSP

In SPI Slave mode with slave select enabled (SSPM<3:0> = 0100), the minimum time between the falling edge of the $\overline{SS}$ pin and first SCK edge is greater than specified in parameter 70 in Table 28-17 and Table 28-18 of the "*PIC18F2455/2550/4455/4550 Data Sheet*" (DS39632). The updated specification is shown in bold in Table 1.

The minimum time between $\overline{SS}$ pin low and an SSPBUF write is also 3 TCY. If the falling edge of the $\overline{SS}$ pin occurs greater than 3 TCY, before the first SCK edge or loading SSPBUF, the peripheral will function correctly. Also, if SSPBUF is written prior to the $\overline{SS}$ pin going low, the peripheral will function correctly.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$ ↓ to SCK ↓ or SCK ↑ Input	**3 TCY**	—	ns	

2. Module: MSSP

With MSSP in SPI Master mode, FOSC/64 or Timer2/2 clock rate and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur as indicated by the WCOL bit being set.

Work around

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: ECCP (PWM Mode)

When configured for half-bridge operation with dead band (CCPxCON<7:6> = 10), the PWM output may be corrupted for certain values of the PWM duty cycle. This can occur when these additional criteria are also met:

- A non-zero dead-band delay is specified (PDC6:PDC0 > 0)
- The duty cycle has a value of 0 through 3, or 4n + 3 (n ≥ 1)

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: EUSART

In Synchronous Master mode, while transmitting the Most Significant data bit, the data line (DT) may change state before the bit finishes transmitting. If the receiver samples the data line later than 0.5 bit times + 1.5 TCY (of the master) after the starting edge of the MSb, the bit may be read incorrectly.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: ADC

When the A/D clock source is selected as 2 TOSC or RC (ADCS2:ADCS0 = 000 or x11), the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 2047, 2048 and 2049 only.

Work around

Select a different A/D clock source (4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC, 64 TOSC) and avoid selecting the 2 TOSC or RC modes.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Electrical Characteristics (BOR)

Certain operating conditions can move the effective Brown-out Reset (BOR) threshold outside of the range specified in the electrical characteristics of the device data sheet (parameter D005).

The BOR threshold has been observed to increase with high device operating frequencies, some table read operations and heavy loading on the USB voltage regulator. When all of these conditions are present, BOR has been observed with VDD 20 percent higher than the VBOR value specified for a given <BORV1:BORV0> setting.

The BOR threshold may decrease under other conditions, such as during Sleep, where it may not occur until VDD is 120 mV below the specified minimums.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: MSSP (SPI Slave)

If configured in SPI Slave mode, the MSSP may not successfully recognize data packets generated by an external master processor. This applies to all SPI Slave modes (CKE/CKP = 1 or 0), whether or not slave select is enabled (SSPM3:SSPM0 = 010x).

Work around

Insert a series resistor between the SPI master Serial Data Out (SDO) and the corresponding SPI slave Serial Data In (SDI) input line of the microcontroller. The required value for the resistor varies with the application system's characteristics and the process variations between the microcontrollers.

Experimentation and thorough testing are encouraged.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: MSSP

When operated in I^2C™ Master mode, the I^2C baud rate may be somewhat slower than predicted by the following formula:

$$I^2C \text{ Master mode, clock} = \frac{F_{OSC}}{4 \bullet (SSPADD + 1)}$$

Work around

If the target application is sensitive to the baud rate and requires more precision, the SSPADD value can be adjusted to compensate.

If this work around is going to be used, it is recommended that the firmware first check the Revision ID by reading the DEVID1 value at address 3FFFFEh. Silicon revisions B6 and B7 will match the I^2C baud rate predicted by the given formula.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (5/2007)
Initial release of this document. Silicon issues 1-2 (MSSP), 3 (ECCP – PWM Mode), 4 (EUSART) and 5 (ADC).

Rev B Document (3/2008)
Added silicon issue 6 Electrical Characteristics (BOR).

Rev C Document (4/2008)
Added silicon issue 7 (MSSP – SPI Slave).

Rev D Document (9/2008)
Added silicon issue 8 (MSSP).

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