

MT9V127IA3XTCH-GEVB

MT9V127 Evaluation Board User's Manual



ON Semiconductor®

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EVAL BOARD USER'S MANUAL

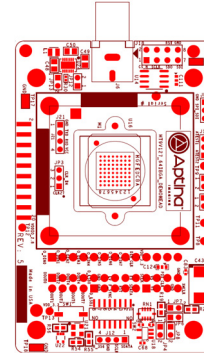


Figure 1. MT9V127 Evaluation Board

Evaluation Board Overview

The evaluation boards are designed to demonstrate the features of ON Semiconductor's image sensors products. This headboard is intended to plug directly into the Demo 2X system. Test points and jumpers on the board provide access to clock, I/Os and other miscellaneous signals.

Features

- Clock Input
 - ◆ Default – 27 MHz crystal oscillator
 - ◆ Optional Demo 2X controlled MCik
- Two Wire Serial Interface
 - ◆ Selectable base address
- Parallel Interface
- ROHS Compliant

Block Diagram

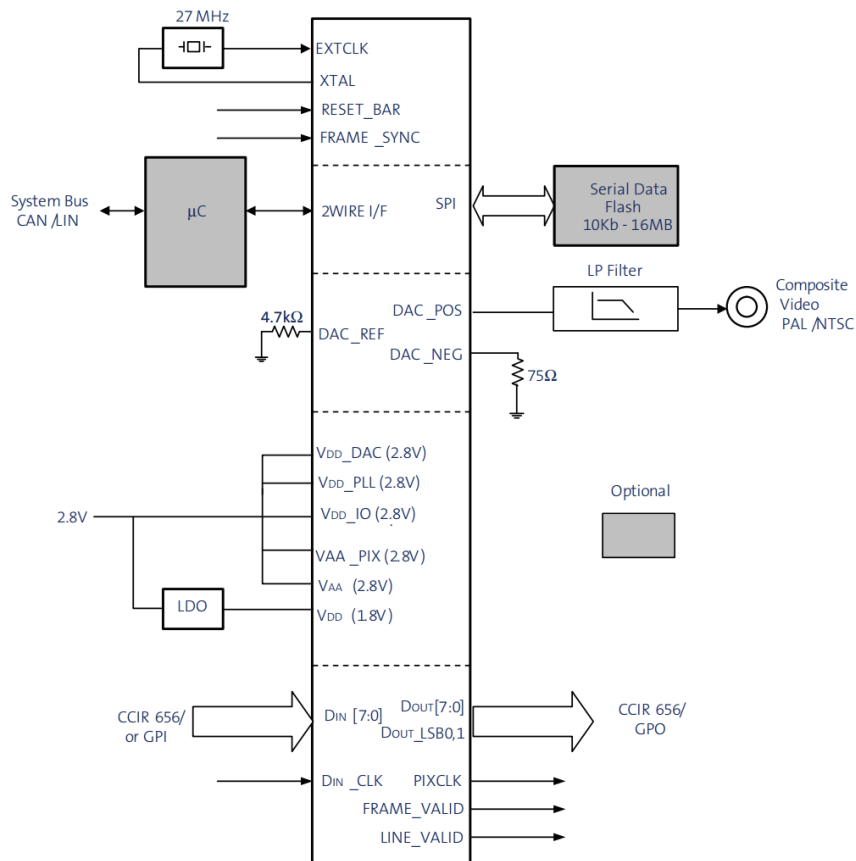


Figure 2. Block Diagram of MT9V127IA3XTCH-GEVB

MT9V127IA3XTCH-GEVB

Top View

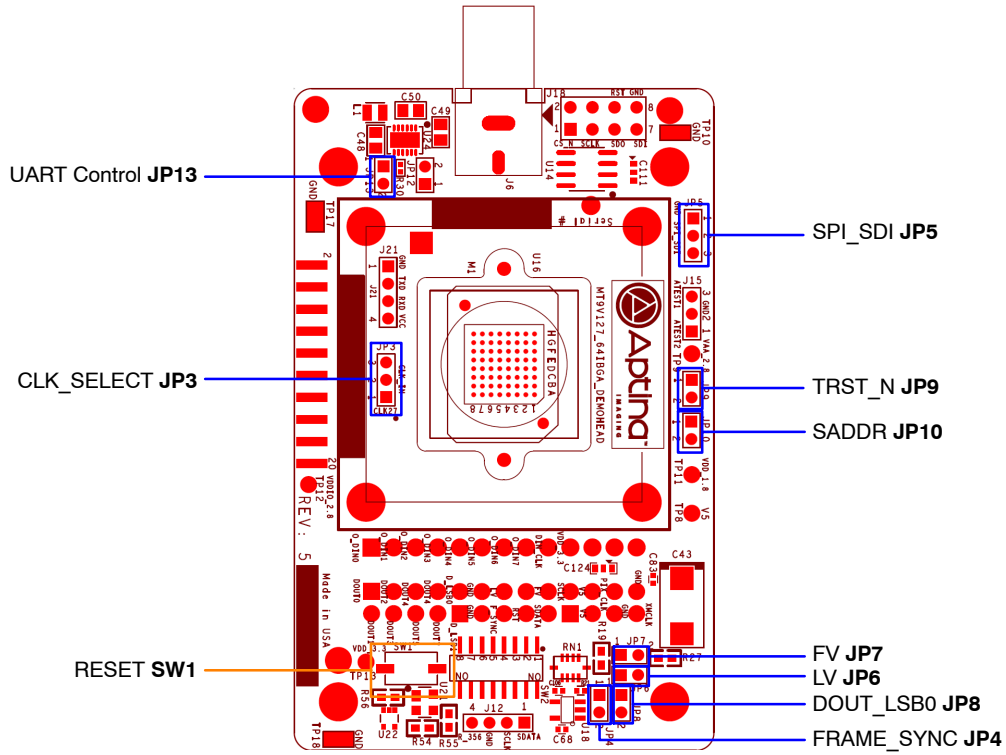


Figure 3. Top View of Evaluation Board – Jumpers

Bottom View

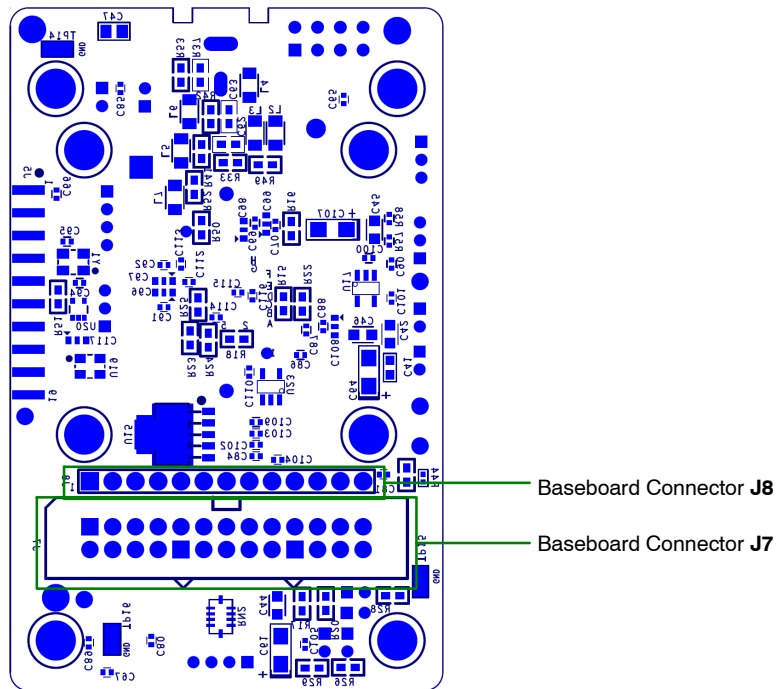


Figure 4. Bottom View of the Evaluation Board – Connector

MT9V127IA3XTCH-GEVB

Jumper Pin Locations

The jumpers on headboards start with Pin 1 on the leftmost side of the pin. Grouped jumpers increase in pin size with each jumper added.

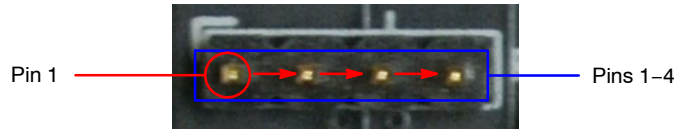


Figure 5. Pin Locations for a Single Jumper.
Pin 1 is Located at the Leftmost Side and Increases as it Moves to the Right

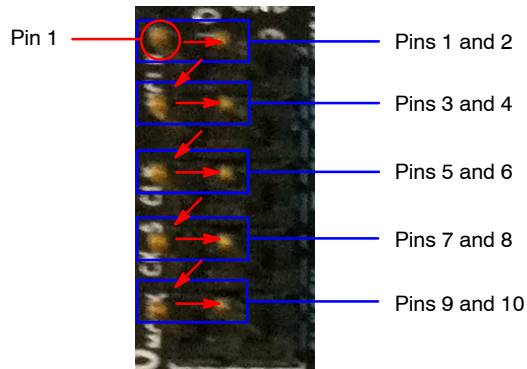


Figure 6. Pin Locations and Assignments of Grouped Jumpers.
Pin 1 is Located at the Top-Left Corner and Increases in a Zigzag Fashion Shown in the Picture

Jumper/Header Functions & Default Positions

Table 1. JUMPERS AND HEADERS

| Jumper/Header No. | Jumper/Header Name | Pins | Description |
|-------------------|--------------------|---------------|---|
| JP3 | CLK_SELECT | 1-2 (Default) | Connect to on-board oscillator |
| | | 2-3 | Connect to crystal oscillator |
| JP4 | FRAME_SYNC | 1-2 (Default) | Normal operation |
| | | Open | Connection to external trigger |
| JP5 | SPI_SDI | 2-3 (Default) | Flash Mode |
| | | 1-2 | Host Mode |
| | | Open | Auto-Configured Mode |
| JP6 | LV | 1-2 (Default) | Video output does not have pedestal |
| | | Open | Video output has pedestal |
| JP7 | FV | 1-2 (Default) | Video output is not horizontally flipped |
| | | Open | Video output is horizontally flipped |
| JP8 | DOUT_LSB0 | 1-2 (Default) | NTSC composite video output mode |
| | | Open | PAL composite video output mode |
| JP9 | TRST_N | 1-2 (Default) | Normal Mode |
| | | Open | External connection for Test Mode |
| JP10 | SADDR | 1-2 (Default) | GND |
| | | Open | External connection to I ² C address control |

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Table 1. JUMPERS AND HEADERS (continued)

| Jumper/Header No. | Jumper/Header Name | Pins | Description |
|-------------------|--------------------|----------------|--|
| JP13 | UART Control | Open (Default) | UART Shutdown |
| | | 1-2 | UART Active |
| SW1 | RESET | N/A | When pushed, 240 ms reset signal will be sent to MT9V127 |

Interfacing to ON Semiconductor Demo 2X Baseboard

The ON Semiconductor Demo 2X baseboard has a similar 26-pin connector and 13 pin connector which mate

with J7 and J8 of the headboard. The four mounting holes secure the baseboard and the headboard with spacers and screws.

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