

***TMS320DM6467***  
***Evaluation Module***

*Technical  
Reference*



# TMS320DM6467 Evaluation Module Technical Reference

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## About This Manual

This document describes the board level operations of the TMS320DM6467 Evaluation Module (EVM). The EVM is based on the Texas Instruments TMS320DM6467 Processor.

The TMS320DM6467 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the TMS320DM6467 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

## Notational Conventions

This document uses the following conventions.

The TMS320DM6467 Evaluation Module will sometimes be referred to as the DM6467 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

```
equations  
!rd = !strobe&rw;
```

## Information About Cautions

This book may contain cautions.

***This is an example of a caution statement.***

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

## Related Documents, Application Notes and User Guides

Information regarding this device can be found at the following Texas Instruments website:

<http://www.ti.com>

**Table 1: Manual History**

Revision	History
A	Alpha Release

**Table 2: Board History**

PWB Revision	History
A	Alpha Release



# Chapter 1

## Introduction to the TMS320DM6467 EVM

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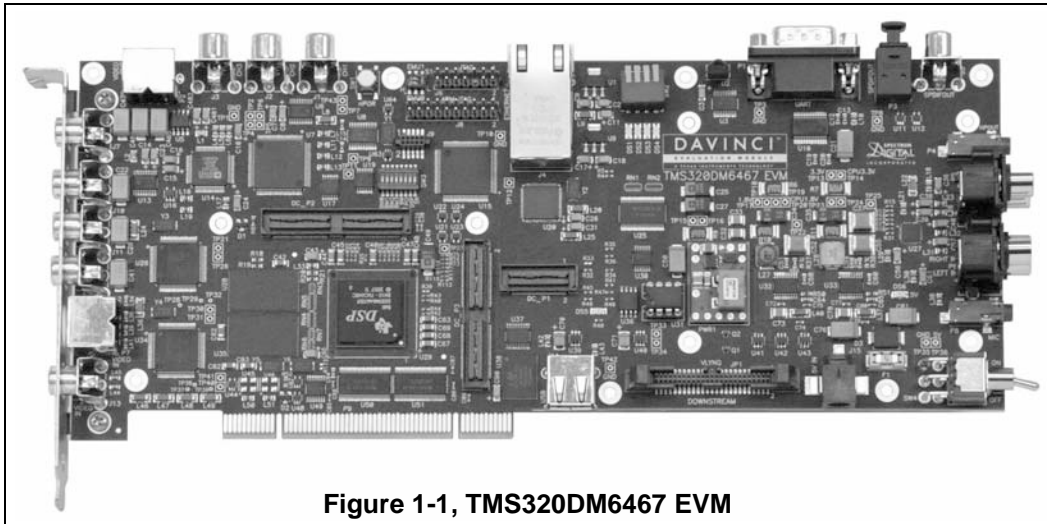
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Chapter One provides a description of the TMS320DM6467 EVM along with the key features and a block diagram of the circuit board.

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## 1.1 Key Features

The TMS320DM6467 EVM is a PCI based or standalone development platform that enables users to evaluate and develop applications for the TI DaVinci™ processor family. Schematics, list of materials, and application notes are available to ease hardware development and reduce time to market.



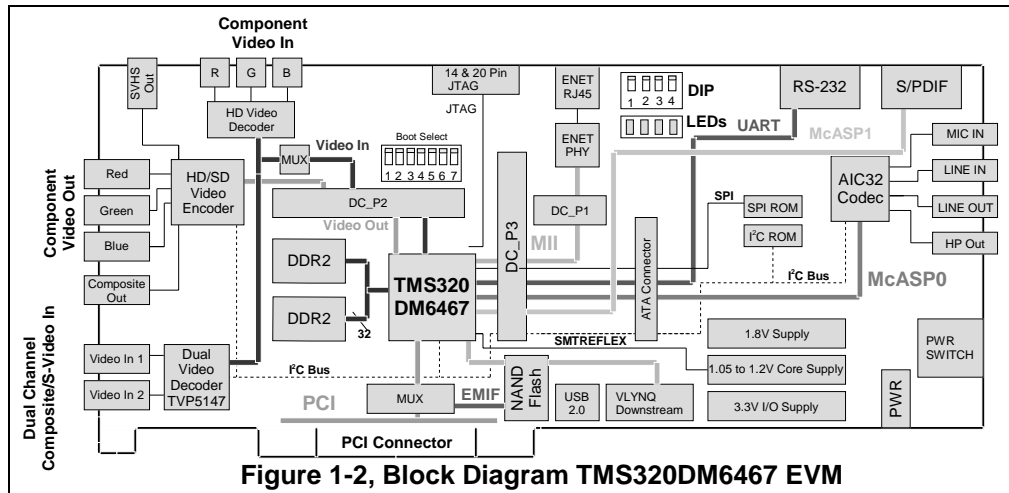
**Figure 1-1, TMS320DM6467 EVM**

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320DM6467 multi-CPU processor, ARM926EJ-S, C64x+
- 256 Mbytes of DDR2 DRAM
- 128 Mbytes of NAND Flash memory, I<sup>2</sup>C EEPROM, SPI EEPROM
- Component HD video output (resolutions up to 720p, 1080i)
- Composite, or S-video output
- Dual TVP5147 video decoders, supports composite and S-video
- TVP7002 provides component HD video input
- AIC32 stereo codec providing analog audio inputs and outputs
- RS-232 UART
- USB 2.0 Host connector
- 10/100/1000 MBS Ethernet Interface
- Configurable boot load options

- External JTAG emulation interface (14 and 20 pins)
- 4 user LEDs and 4 position user switch
- Expansion connectors for daughter card interfaces
- VLYNQ Down Stream Interface
- S/PDIF Interface, analog, and optical
- ATA Hard Disk Interface
- Single voltage power supply (+5V)

## 1.2 Functional Overview of the TMS320DM6467 EVM



The TMS320DM6467 on the EVM interfaces to on-board peripherals through integrated device interfaces and a 8-bit wide EMIF bus. The DDR2 memory is connected to its own dedicated 32 bit wide bus. The EMIF bus is selectable to be connected to the NAND Flash, and daughter card expansion connectors.

Two on board standard video decoders, one high definition video decoder, and on board standard video and high definition video encoder interface video streams to the TMS320DM6467 processor. Dual TVP5147 decoders, one TVP7002, and an on board ADV7343 six channel encoder are standard on the EVM and directly interface to on chip video ports. On screen display functions are implemented in software on the TMS320DM6467 processor.

An on-board AIC32 codec allows the DSP to transmit and receive analog audio signals. The I<sup>2</sup>C bus is used for the codec control interface, while the McASP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks and Dual RCA jacks that correspond to microphone input, line input, line output, and headphone outputs.

The EVM includes 4 user LEDs, and 4 position user DIP switch which can be used to provide the user with interactive feedback. These interfaces are implemented via I<sup>2</sup>C expanders.

VLYNQ, USB II, and ethernet MAC interfaces are integrated peripherals on the DM6467 processor exploiting its system on a chip architecture.

An included +5V external power supply is used to power the board. On-board switching voltage regulators provide the +1.2V CPU core voltage and +3.3V for peripherals and +1.8V for DDR2 memory. The board is held in reset until these supplies are within operating specifications.

Code Composer communicates with the EVM through an embedded emulator or via the 14 pin external JTAG connector.

### **1.3 Basic Operation**

The EVM is designed to work with TI's Code Composer Studio development. Code Composer communicates with the board through the embedded emulator or an external JTAG emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

## 1.4 Memory Map

The DaVinci family of processors have a large byte addressable address space, some limitations to byte addressing are determined by peripheral interconnection to the TMS320DM6467 device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a TMS320DM6467 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF directly interfaces to the DDR2 memory. The NAND Flash is mapped into CS2 space on the other EMIF. When CS2 is used for daughter card interfacing the daughter card enable pin must be brought high.

Address	TMS320DM6467 EVM
0x00000000	Internal ARM RAM (instruction)
0x00008000	Internal ARM ROM (instruction)
0x00010000	Internal ARM RAM (data)
0x00018000	Internal ARM ROM (data)
0x00818000	L2 RAM/Cache (C64x+)
0x00E00000	L1 P Cache (C64x+)
0x00F00000	L1 D RAM/Cache (C64x+)
0x30000000	PCI Address Space
0x42000000	CS2 - NAND Flash
0x4C000000	VLYNQ
0x80000000	DDR2
0xA0000000	

**Figure 1-3, Memory Map, TMS320DM6467 EVM**

### 1.5 Configuration Switch Settings

The EVM has an eight position boot switch that allow users to control the operational state of the processor when it is released from reset. The configuration switch is labeled SW3 on the EVM board.

The switch configures the boot mode that will be used when the CPU starts executing. By default the switches are configured to NAND boot. Refer to the boot load options in Chapter 3 for configuring switch SW3.

### 1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J15), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into +1.2V, +1.8V and +3.3V using Texas Instruments swift voltage regulators and PTH power module. The +1.2V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and other chips on the board. The +1.8 volt supply is used for TMS320DM6467 DDR2 interface, and DDR2 memory.

There are multiple power test points on the EVM. The three main test point pairs provide a convenient mechanism to check the EVM's current for each supply. The table below shows the voltages for each test point and what the supply is used for.

**Table 1: Power Test Points**

Test Point Pair	Voltage	Voltage Use
TP15 & TP16	+1.2 V	TMS320DM6467 Core
TP23 & TP24	+3.3V	DSP I/O and logic
TP18 & TP19	+1.8 V	DDR2 Memory, DSP I/O, and logic

# Chapter 2

## Board Components

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This chapter describes the operation of the major board components on the TMS320DM6467 EVM.

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## **2.1 EMIF Interfaces**

An 8 bit EMIF with multiple chip selects divide up the address space and allow for asynchronous accesses on the EVM. On board the CS2 is used for NAND Flash. This interface is multiplexed with the PCI interface and daughter card interface. The figure below illustrates this multiplexing. when the board is plugged into the PCI slot the CPLD detects this condition and the EMIF is disabled. Furthermore the EMIF signals to the daughter card are disabled. When the board is not plugged into a PCI slot the EMIF is enabled and the NAN flash is available on CS2 along with the ATA drive.

When pulled high, the EMIF\_MODE pin on connector DC\_P3 turns the multiplexers for daughter card usage.

## **2.2 Peripheral Interfaces**

The TMS320DM6467 has several peripheral interfaces which allow the user to interface to external devices. These interfaces are outlined in the following sections.

### **2.2.1 PCI Interface**

The EVM supports a 33 Mhz. PCI interface. The board uses CBT multiplexers to interface the PCI slot, EMIF, and daughter card interface to the TMS320DM6467 device. Furthermore the CBT's also provide compatibility with +5 volt PCI interfaces. The board automatically configures the PCI enable signal on the TMS320DM6467 when the board is plugged into a PCI slot. When the PCI interface is enabled the NAND Flash and ATA interface is disabled on board.

### **2.2.2 VLYNQ Interface**

The TMS320DM6467 brings its internal VLYNQ interface out to a 50 pin Samtec FTSH style connector JP1. The VLYNQ interface is implemented as a down stream peripheral and supports four transmit and receive channels.



### **2.2.3 UART Interface**

The internal UART0 on the TMS320DM6467 device is driven to connector P1. The UART's interface is routed through CBT's to a Texas Instruments MAX3243 RS-232 line driver prior to being brought out to a male DB-9 connector, P8. The on board UART signals can be disabled by pulling the UART0\_EN signal high via the daughter card connectors.

### **2.2.4 ATA Interface**

The TMS320DM6467 EVM integrates a standard ATA interface on chip. This interface is multiplexed with the PCI and I/O daughter card interfaces. When PCI or daughter card interfaces are enabled the ATA interface is not available for development. The EVM can directly interface to a standard lap top hard disk drive via connector JP2. Power to the drive is controlled via I<sup>2</sup>C register implemented in the CPLD.

## **2.3 DDR2 Memory Interface**

The TMS320DM6467 device incorporates a dedicated 32 bit wide DDR2 memory bus. The EVM uses two 1 gigabit 16 bit wide memories on this bus, for a total of 256 megabytes of memory for program, data, and video storage. The internal DDR controller uses a PLL to control the DDR memory timing. The interface supports rates up to 300 Mhz., and is clocked on differential edges for optimal performance. Memory refresh for DDR2 is handled automatically by the TMS320DM6467 internal DDR controller.

## **2.4 NAND Flash Interface**

The TMS320DM6467 has 128 megabytes of NAND Flash mapped into the CS2 space. The NAND Flash memory is used primarily for boot loading. The CS2 space is configured as 8 bits wide on the TMS320DM6467 EVM for NAND flash usage.

The NAND and ATA interface are multiplexed with the PCI or daughter card interface. The NAND and ATA interface can be active when the PCI or daughter card interfaces are disabled.

**2.5 Video Interfaces**

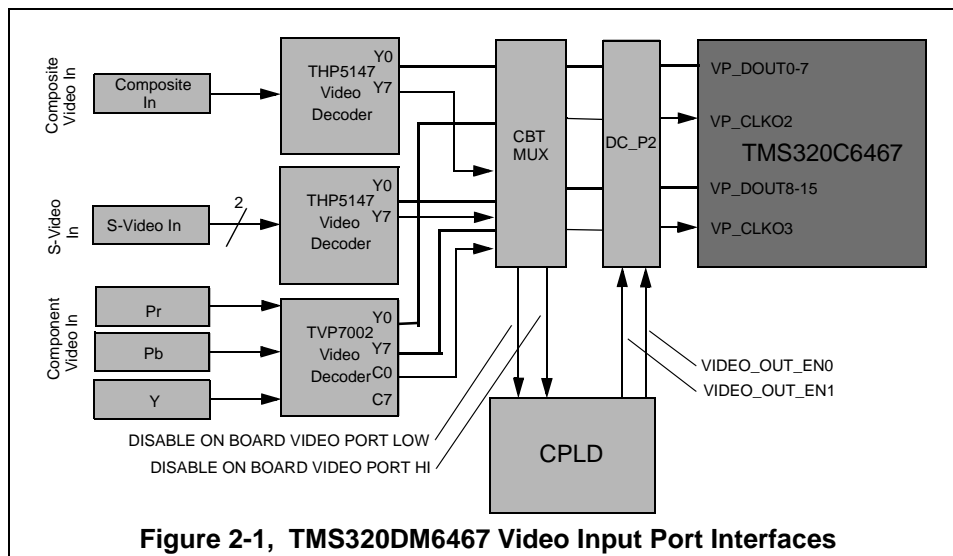
The TMS320DM6467 EVM has a 16 bit dividable video input port and 16 bit dividable output port to support a variety of user applications. Both ports can be used as two eight bit ports when the appropriate interface only requires 8 bits. High definition interfaces require all 16 bits. The EVM incorporates dual TVP5147 decoders or a TVP7002 tied to the input port. An ADV7343 is connected to the output ports providing standard video or component video interfaces.

**2.5.1 Video Input Port Interfaces**

The TMS320DM6467 EVM supports video capture via the devices dual 8 bit or single 16 bit internal video ports. The EVM incorporates dual Texas Instruments TVP5147s to decode composite video or S-video inputs into the TMS320DM6467 device. P7 is used for the S-video inputs and J13 for the composite inputs on the EVM.

Corresponding High Definition component video can be driven into the TMS320DM6467 video input port via a TVP7002 when the video port on the EVM is configured for 16 bit mode. The component inputs are driven into RCA connectors J1, J2, J3.

User inputs can be driven via daughter card connector DC\_P2 when the on board multiplexers are configured for daughter card use. The figure below illustrates the input port configurations. The on board CBT multiplexer input modes are controlled via the CPLD control register 1 as discussed in section 2.12.



## 2.5.2 Video Output Port Interfaces

The TMS320DM6467 EVM has a 16 bit wide video output port which directly interface to an ADV7343 encoder. The video output ports are actually two 8 bit ports which are combined into a single 16 bit port for high definition video applications.

The on board encoder can generate composite video, S-video, or component video. The TMS320DM6467's output port is directly interfaced to the video encoder via CBT multiplexers and switches. The on board encoder video inputs can be directly connected via the daughter card interface in two 8 bit sections when the daughter card asserts VIDEO\_OUT\_EN0 and/or VIDEO\_OUT\_EN1 high.

For the high definition modes Y0-Y7 and C0-C7 inputs are used on the encoder. To change the on board CBT multiplexer to this mode the CPLD control register 1, bit 6 needs to be programmed to the appropriate mode. The diagram below illustrates the video port output configuration on the EVM.

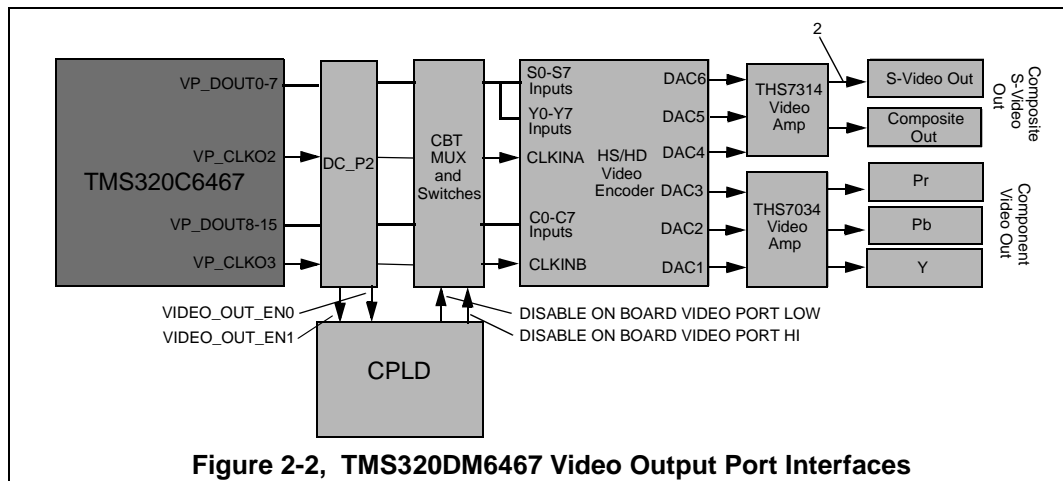


Figure 2-2, TMS320DM6467 Video Output Port Interfaces

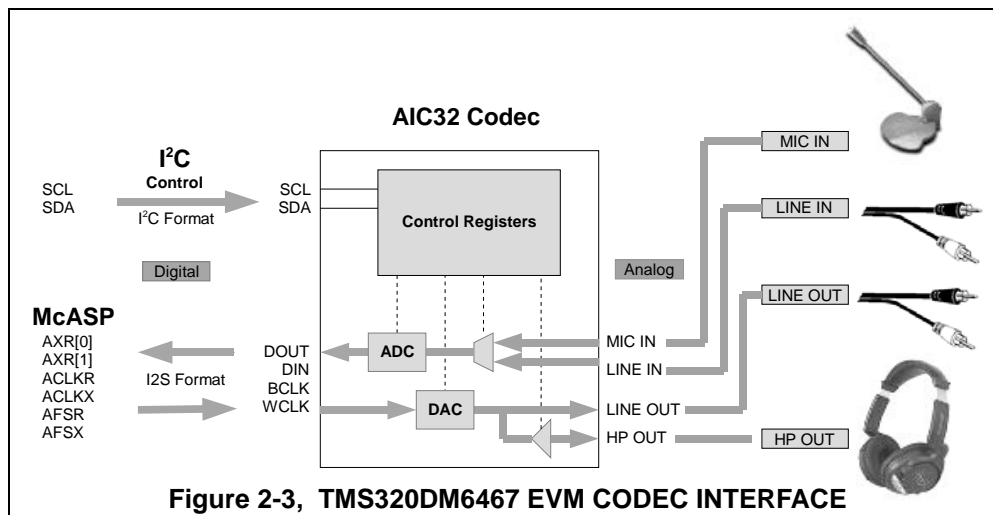
## 2.6 AIC32 Interface

The EVM uses a Texas Instruments TLV320AIC32 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I<sup>2</sup>C bus is used as the unidirectional control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

The bi-directional data channel interfaces to the on chip McASP0. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate for the McASP.

The codec has a programmable clock from a CDCE949 PLL device which is configurable via I<sup>2</sup>C. The default system clock is generated by the CDCE949. The internal sample rate generate subdivides the default clock to generate common frequencies. The sample rate generator in the AIC32 is set by I<sup>2</sup>C command codec registers. The figure below shows the codec interface on the TMS320DM6467 EVM.



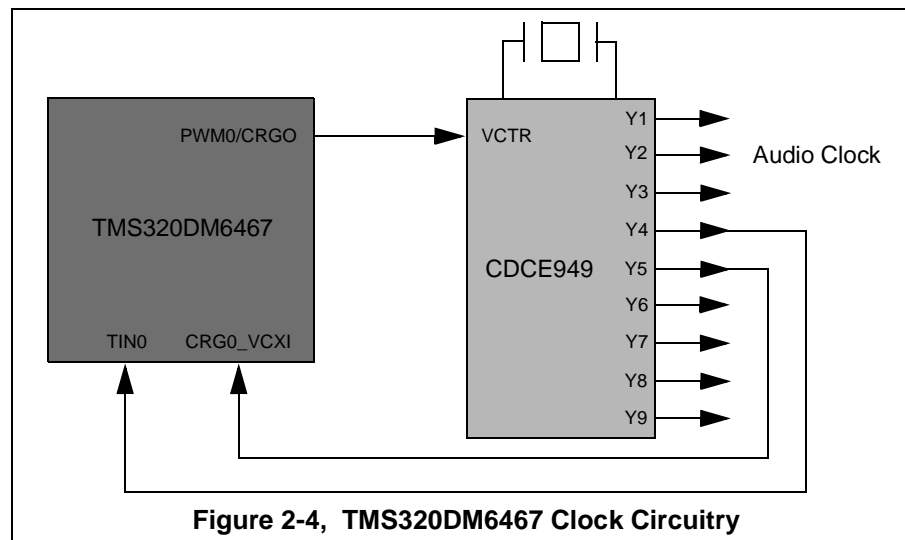
### 2.6.1 Audio PLL/VCXO Circuit/CDCE949 Clock Generator

The TMS320DM6467 EVM implements a multiple PLL clock generator via the CDCE949 for creating the audio and optional video clocks for the board.

In streaming video applications the audio and video sequences can lose synchronization. The TMS320DM6467 uses a VCXO interpolation circuit to incrementally speed up or slow down the clocks to allow for this synchronization to remain locked.

The PWM0 and timer input TIN0 or CRG0 and CRG0\_VCXI are used to control this feature on the EVM. The PWM0 or CRG0 pin drives VCTR on the CDCE949 which is fed back into the timer input pin or the CRG0\_VCXI pin on the DM6467.

This device creates the clocks for the AIC32 Codec, daughter card, and optional video clocks. The CDCE949 is programmable via an I<sup>2</sup>C and support virtually any clock rate by use of its fractional PLL architecture.



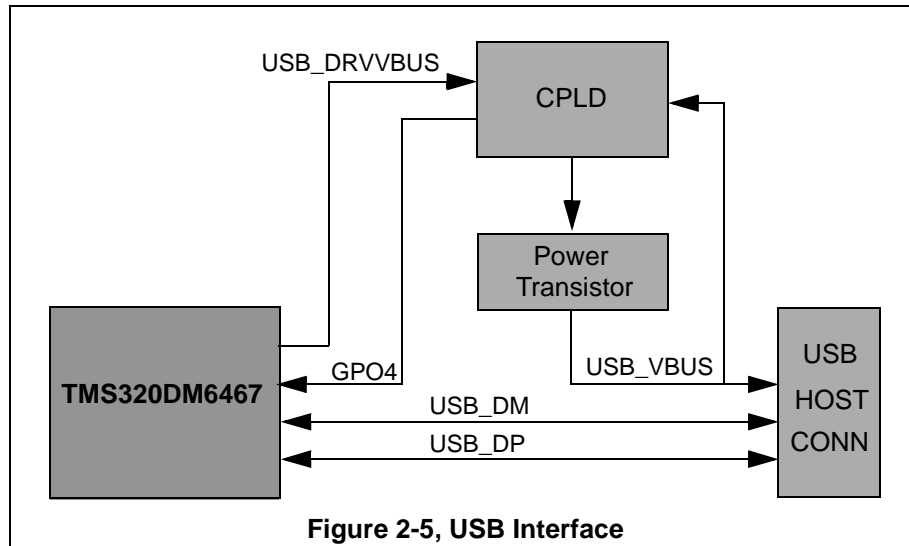
### 2.7 Ethernet Interface

The TMS320DM6467 integrates an GMII/MII ethernet MAC on chip. This interface is routed to the on board PHY via CBT switches. The EVM uses an Agere ET1011C PHY. The interface is isolated and brought out to a RJ-45 connector with integrated magnetics, J4. The ethernet address is stored in the I<sup>2</sup>C serial ROM during manufacturing. The on board PHY can be disabled by pulling the MAC\_EN pin high on the daughter card connector DC\_P1.

The RJ-45 has 2 LEDs integrated into its connector. The green LED indicates the status of the ethernet's link status. When blinking, the yellow LED indicates Re/Tx activity.

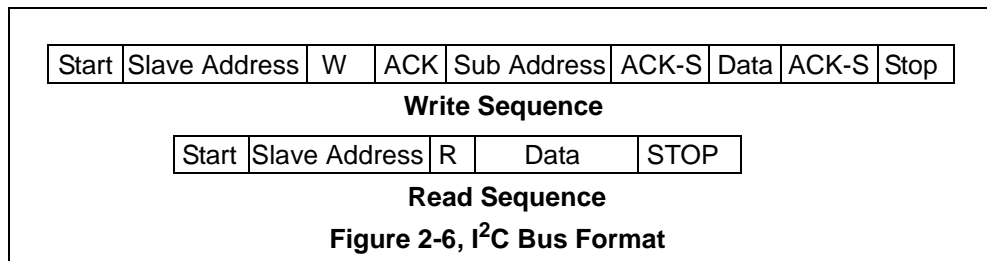
### 2.8 USB Interface

The EVM supports a hostmode USB II connector. The USB power is enabled via the DRV\_BUS signal on the EVM. The VBUS power is feed back to the on board CPLD and is available for sampling on the CPU's GPO4 signal. The feedback on GPO4 must be enabled in the CPLD Control Register 0, bit 6. The figure below illustrates this function.



## 2.9 I<sup>2</sup>C Interface

The I<sup>2</sup>C bus on the TMS320DM6467 is ideal for interfacing to the control registers of many devices. On the TMS320DM6467 EVM the I<sup>2</sup>C bus is used to configure the video decoder, stereo Codec, I/O expanders. An I<sup>2</sup>C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.



The addresses of the on board peripherals are shown in the table below.

**Table 1: I<sup>2</sup>C Memory Map**

Address	Device	R/W
0x18	AIC32	R/W
0x2A	ADV7343	R/W
0x2C	THS7303 - Output	W
0x2E	THS7353 - Input	R
0x38	I/O Expander 0 (LEDs, User Switches)	R/W
0x3A	CPLD Embedded I <sup>2</sup> C Register 1	R/W
0x3B	CPLD Embedded I <sup>2</sup> C Register 2	R/W
0x3C	CPLD Embedded I <sup>2</sup> C Register 3	R/W
0x50	I <sup>2</sup> C ROM	R/W
0x5C	TPV5147 II *	R/W
0x5D	TPV5147 I *	R/W
0x5D	TPV7002	R/W
0x6C	CDE949	R/W

\* I<sup>2</sup>C CPLD control bit 4 at location 0x3B is used to enable 1 device at this address at a time.

**2.9.1 I/O Expander**

The TMS320DM6467 EVM uses an I<sup>2</sup>C expander to interface to user dip switch and user LEDs. The 8 bit I/O expander, a PCF8574A, at reset is initialized to 0xFF, all ones. The bit definition of the I/O expanders is shown in the table below.

**Table 2: U10 I/O Expander**

Pin Number	Function	Description
P0	SW4-0	Read only user switch
P1	SW4-1	Read only user switch
P2	SW4-2	Read only user switch
P3	SW4-3	Read only user switch
P4	LED 1	User LED DS1
P5	LED 2	User LED DS2
P6	LED 3	User LED DS3
P7	LED 4	User LED DS4

**2.9.2 I<sup>2</sup>C EEPROM**

The TMS320DM6467 EVM incorporates an I<sup>2</sup>C eeprom that can be used for booting or general purpose storage.

This eeprom is also used to store the ethernet MAC address and the board's revision. The MAC address is also labeled on the board. Care should be taken not to erase these items when user information is stored in the eeprom. Spectrum Digital uses addresses 0x7F00 to 0x7FFF for manufacturing information. This information is shown in the table below.

**Table 3: TMS320DM6467 MAC Addresses**

Address	Contents
0x7F00	EMAC Address 0 (most significant)
0x7F01	EMAC Address 1
0x7F02	EMAC Address 2
0x7F03	EMAC Address 3
0x7F04	EMAC Address 4
0x7F05	EMAC Address 5
0x7F06	Reserved
0x7F07	Board Revision



### **2.9.3 SPI EEPROM**

The EVM incorporates a 32 Kilobyte SPI ROM. The ROM interfaces via CBTs to the DM6467 SPI interface module. The on board interface can be disabled via the SPI\_ENABLE daughter card pin when the pin is pulled high.

### **2.10 S/PDIF Analog, and Optical Interfaces**

The McASP1's AxR[0] pin on the TMS320DM6467 can be configured to operate as a S/PDIF transmitter. The TMS320DM6467 EVM supports both analog and optical interfaces. The analog S/PDIF output pin is routed to a driver and filter circuit before being output on J5. Another driver is used to interface the optical transmitter P3.

#### **2.10.1 Infrared Sensors**

The EVM incorporates a TSOP34840 40Khz. infrared receiver. The receiver is an input to the CPLD where it is available in non-modulated bit form on pin GPO1 or in modulated form to UART2 Rx pin in CIR format.

Two control bits in CPLD enable or disable this function. The output pins from the CPLD can also be disabled via the daughter card connector.

### 2.11 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for all major interfaces including memory, peripherals, and video expansion.

The pin outs for this interface are documented in Chapter 3.

The connectors provide access to the DSP's EMIF signals, I/O, host port and video ports to interface with memories, memory mapped devices, peripherals, video encoders, video decoders, audio codecs, and streaming interfaces.

There are three daughter card interfaces, DC\_P1, DC\_P2, DC\_P3. These connectors are described in the table below. Several signals are used to disable the on board peripherals so that they can be used by the expansion connector as documented in Chapter 3.

**Table 4: Daughter Card Interfaces**

<b>Interface Name</b>	<b>Function</b>
DC_P1	Ethernet Interface Connector
DC_P2	Video Expansion Connector
DC_P3	I/O Expansion Connector

Other than the buffering, most daughter card signals are not modified on the board.

## 2.12 CPLD

The on board CPLD incorporates glue logic and I<sup>2</sup>C control registers to minimize logic on the EVM. The CPLD incorporates 3 control registers at addresses 0x3A, 0x3B, and 0x3C. The table below specifies the functions of the I<sup>2</sup>C control registers.

**Table 5: CPLD I<sup>2</sup>C Control Registers**

Address	Register Name
0x3A	I/O Control
0x3B	Video Control
0x3C	Version

### 2.12.1 CPLD Register 0, I/O Control, 0x3A

The table below shows the bit definitions of CPLD register 0 at address 0x3A on the I<sup>2</sup>C bus. The bits in this register are used for I/O control.

**Table 6: CPLD Register 0, I/O Control, 0x3A**

Bit #	Name	Function If 0	Function If 1
0	ATA_RSTn	* ATA Normal	ATA Reset
1	ATA_PWD	* ATA +5V	ATA 0V
2	VSCALEON	* VSCALE[0:1]=High	VSCALE[0:1]=VDDADJ[0:1]
3	VLYNQ_RSTn	* VLYNQ Normal	VLYNQ Reset
4	IR_GPIO	Disable	Put unmodulated IR Output to GPO1
5	IR_UART	Disable	Put modulated IR Output to UART2 RX
6	I <sup>2</sup> C_INT	* INT Enable	INT Disable
7	USB_FB	* USB Feedback Enable	USB Feedback Disable

**2.12.2 CPLD Register 1, Video Control, 0x3B**

The table below shows the bit definitions of CPLD register 1 at address 0x3B on the I<sup>2</sup>C bus. The bits in this register are used for video control.

**Table 7: CPLD Register 1, Video Control 0x3B**

Bit #	Name	Function If 0	Function If 1
0	TVP5147_RST	* TVP5147 Normal	TVP5147 Reset
1	TVP5147_PWD	* TVP5147 Normal Mode	TVP5147 Power Down
2	TVP7002_RST	* TVP7002 Normal	TVP7002 Reset
3	TVP7002_PWB	* TVP7002 Normal Mode	TVP7002 Power Down
4	TVP_SELECT	* Select TVP5147	Select TVP7002
5	VID_IN_MODE	* Standard Def In (CV/SV)	High Def In (HD_Y/HD_C)
6	VID_OUT_MODE	* Standard Def Out (ADV_S)	High Def Out (ADV_Y/ADV_C)
7			

**2.12.3 CPLD Register 2, CPLD Revision, 0x3C**

The table below shows the bit definitions of CPLD register 2 at address 0x3C on the I<sup>2</sup>C bus. The bits in this register represent the revision of the CPLD.

**Table 8: CPLD Register 3, Version, 0x3C**

Bit #	Name	R/W	Description
7:0	Version ID	R	Current CPLD Revision

### **2.13 TMS320DM6467 Core CPU Clock**

The TMS320DM6467 EVM uses a 27 Megahertz crystal to generate the input clock and a 24 Mhz crystal to generate some of the peripheral clock sources. The TMS320DM6467 has an internal PLLs which can multiply the input clock to generate higher speed internal clocks. The PLL multipliers are set via software on the TMS320DM6467 device.

### **2.14 TMS320DM6467 Core Voltage Select**

The TMS320DM6467 EVM has the ability to adjust the core voltage between 1.2 volts and 1.05 volts. GPIO6 and GPIO7 from the DM7467 are used to enable these pins when they are enabled during the boot sequence via the boot switch.

Furthermore the CPLD has a voltage scaling control bit that must be enabled to allow the board to operate in voltage scaling mode.



# Chapter 3

## Physical Description

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This chapter describes the physical layout of the TMS320DM6467 EVM and its interfaces.

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### 3.1 Board Layout

The TMS320DM6467 EVM is a 10.0 x 4.2 inch (254 x 107 mm.) fourteen (14) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 and Figure 3-2 show the layout of the TMS320DM6467 EVM.

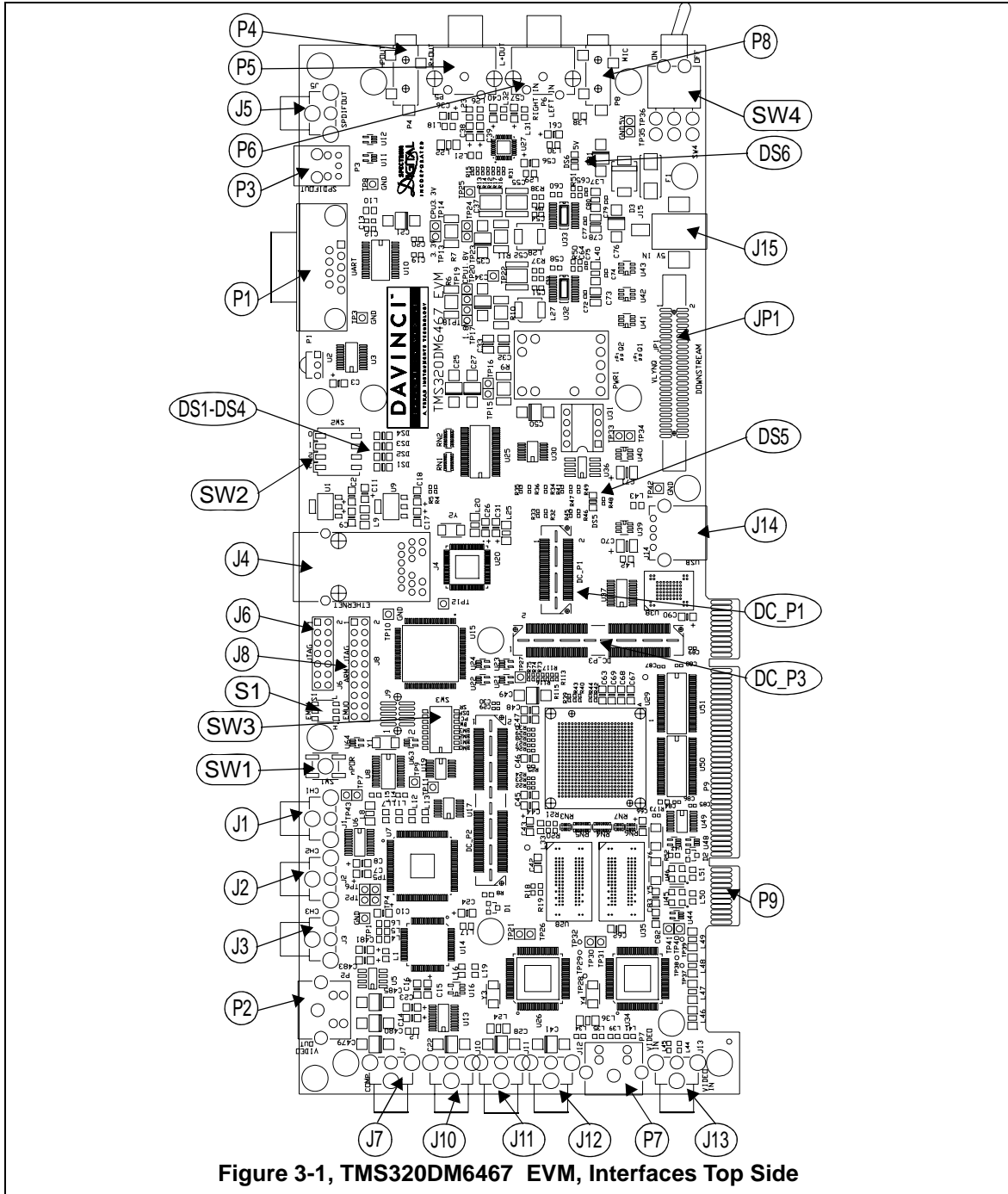


Figure 3-1, TMS320DM6467 EVM, Interfaces Top Side

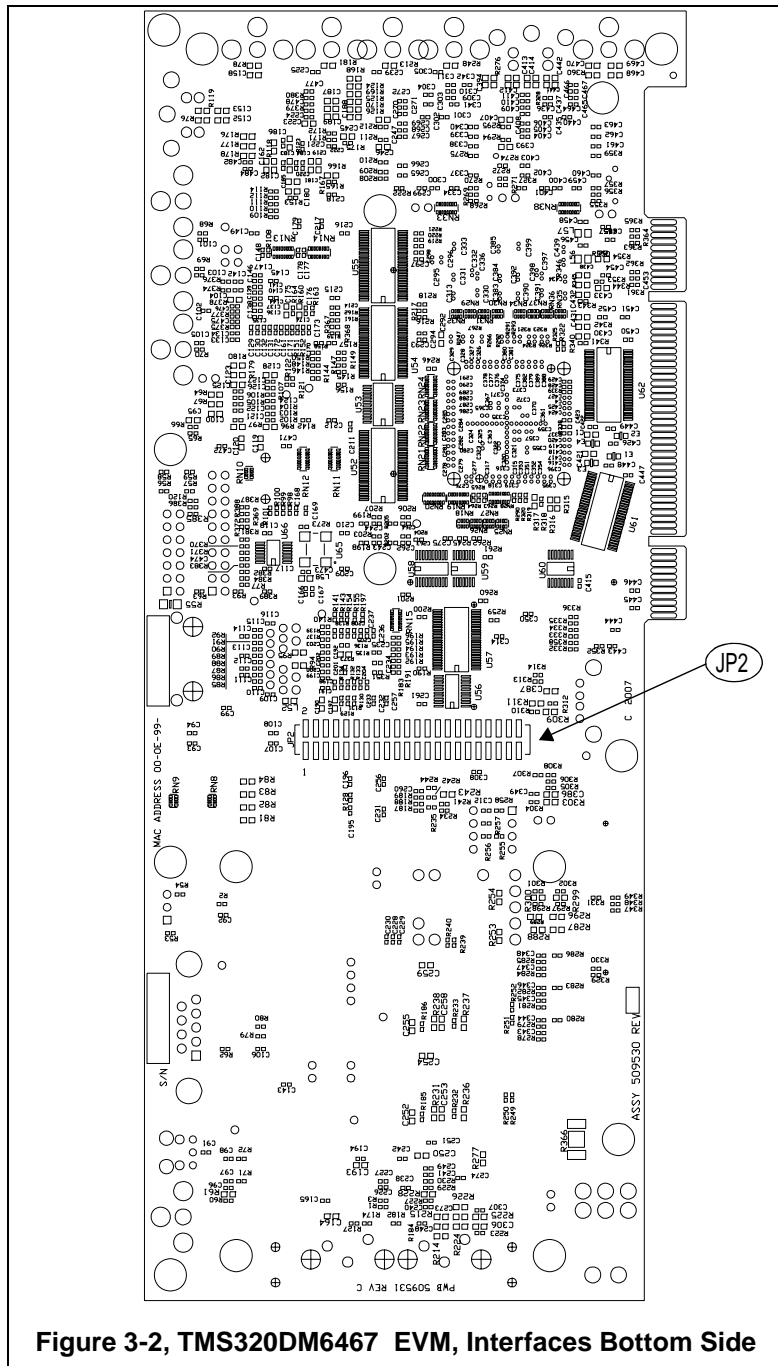


Figure 3-2, TMS320DM6467 EVM, Interfaces Bottom Side

### 3.2 Connectors

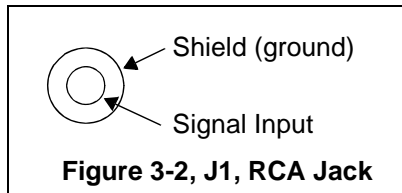
The EVM has twenty nine (29) interfaces to various peripherals. These interfaces are described in the following sections.

**Table 1: Connectors**

Connector	Size	Function
J1	RCA	HD Video In, Component (Pb)
J2	RCA	HD Video In, Component (Y)
J3	RCA	HD Video In, Component (Pr)
J4	RJ-45	Ethernet
J5	RCA	S/PDIF Analog Out
J6	14	14 Pin TI Emulation Header
J7	RCA	Composite Video Out
J8	20	20 Pin ARM Emulation Header
J10	RCA	HD Video Out Component (Pr)
J11	RCA	HD Video Out Component (Y)
J12	RCA	HD Video Out Component (Pb)
J13	RCA	Composite Video In
J14	4 Pin	USB Host
J15	2.5 mm	+5V In
P1	9 Pin D-sub	RS-232 UART
P2	4 Pin DIN	Composite S-Video Out
P3	RJ-45	S/PDIF Optical Output
P4	3.5 mm	Headphone Out
P5	Dual RCA	Stereo Line In
P6	Dual RCA	Stereo Line Out
P7	4 Pin DIN	S-Video In
P8	3.5 mm	Microphone In
P9	PCI	PCI
U2		IR Interface
JP1	25 x 2	Downstream VLYNQ
JP2	22 x 2	Hard Disk Drive Interface
DC_P1	30 x 2	Ethernet Interface Connector
DC_P2	60 x 2	Video Expansion Connector
DC_P3	60 x 2	I/O Expansion Connector

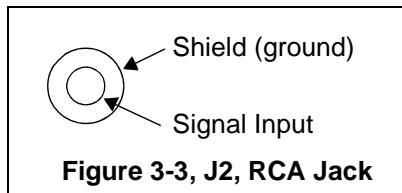
### 3.2.1 J1, HD Component Video In, (Pb)

J1 is an RCA input jack used to bring a channel of HD component (Pb) video to the TMS320DM6467 EVM. This signal is input to the TVP7002 codec. The pinout of this connector is shown below.



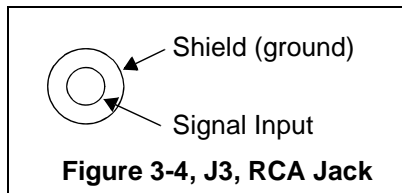
### 3.2.2 J2, HD Component Video In, (Y)

J2 is an RCA input jack used to bring a channel of HD component (Y) video to the TMS320DM6467 EVM. This signal is input to the TVP7002 codec. The pinout of this connector is shown below.



### 3.2.3 J3, HD Component Video In, (Pr)

J3 is an RCA input jack used to bring a channel of HD component (Pr) video to the TMS320DM6467 EVM. This signal is input to the TVP7002 codec. The pinout of this connector is shown below.



### 3.2.4 J4, Ethernet Interface

The J4 connector is used to provide an 10/100/1000 Mbps Ethernet interface. This is a standard RJ-45 connector. The cable end pinout for the J4 connector is shown in the table below.

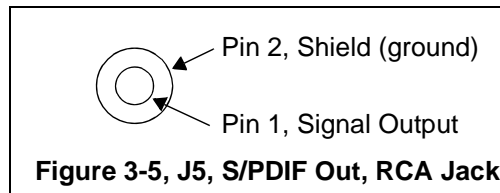
**Table 2: J4, Ethernet Interface**

Pin #	Signal	Pin #	Signal
1	D0+	2	D0-
3	D1-	4	D2+
5	D2-	6	D1-
7	D3+	8	D3-

Two LEDs are embedded into the connector to report link status (green LED) and transmit/receive status of the PHY (yellow LED).

### 3.2.5 J5, S/PDIF Analog Output

J5 is an RCA jack used as an analog output from the McASP1 AxR[0] signal on the DSP. This connector brings out the SPDIF signal. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.



**Figure 3-5, J5, S/PDIF Out, RCA Jack**

**Table 3: J5, S/PDIF, RCA Jack**

Pin #	Signal Name
1	S/PDIF Analog output
2	GND

### 3.2.6 J6, 14 Pin External JTAG Connector

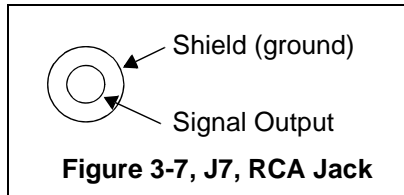
The TMS320DM6467 EVM is supplied with a 14 pin header interface, J6. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown in the figure.

TMS	1	2	TRST-	Header Dimensions
TDI	3	4	GND	
PD (+3.3V)	5	6	<b>no pin (key)</b>	
TDO	7	8	GND	Pin-to-Pin spacing, 0.100 in. (X,Y)
TCK-RET	9	10	GND	Pin width, 0.025-in. square post
TCK	11	12	GND	Pin length, 0.235-in. nominal
EMU0	13	14	EMU1	

**Figure 3-6, JTAG INTERFACE**

### 3.2.7 J7, Composite Video Out

J7 is an RCA output jack which brings out a composite video signal. The pinout of this connector is shown below.



### 3.2.8 J8, Emulation Header, 20 Pin ARM

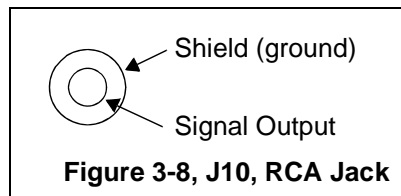
The J8 emulation 20 pin header is located on the top side of the board and is used to provide an interface to ARM JTAG emulators. The pinout for the J1 connector is shown in the table below.

**Table 4: J8, Emulation Header**

Pin #	Signal	Pin #	Signal
1	+3.3 Volts	2	+3.3 Volts
3	TRSTn	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	TCK_RET	12	GND
13	TDO	14	GND
15	ARM-RSTn	16	GND
17	NC	18	GND
19	NC	20	GND

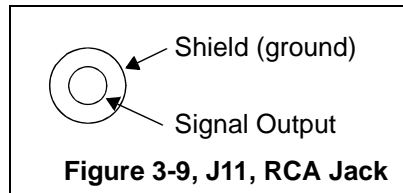
### 3.2.9 J10, Component Video Output, (Pr)

J10 is an RCA jack used to provide High Definition component video (Pr) output to a video monitor. This connector is driven directly by the ADV7343 via an THS7303 driver. The pinout of this connector is shown below.



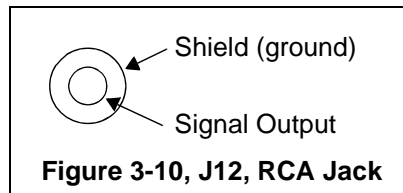
### 3.2.10 J11, Component Video Output, (Y)

J11 is an RCA jack used to provide High Definition component video (Y) output to a video monitor. This connector is driven directly by the ADV7343 via an THS7303 driver. The pinout of this connector is shown below.



### 3.2.11 J12, Component Video Output, (Pb)

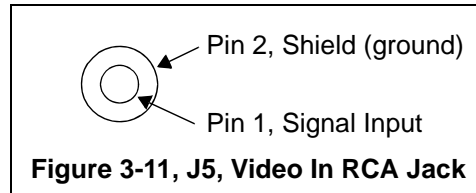
J12 is an RCA jack used to provide High Definition component video (Pb) output to a video monitor. This connector is driven directly by the ADV7343 via an THS7303 driver. The pinout of this connector is shown below.





### 3.2.12 J13, Composite Video In

J13 is an RCA jack used as a video input to the TVP51467 video decoder. This connector brings in a video signal to the TVP5147. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.



**Table 5: J5, Video In, RCA Jack**

Pin #	Signal Name
1	Pin 8, TVP5147
2	GND

### 3.2.13 J14, USB Connector

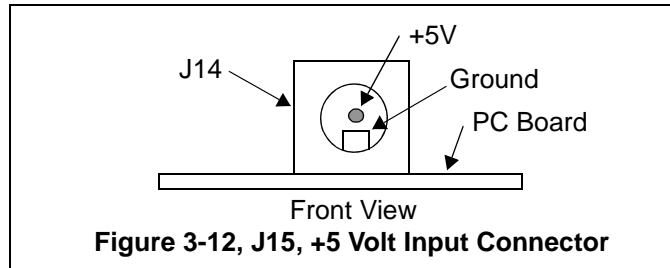
Connector J14 is a USB connector. Three different connectors can be mounted at location J14. The default connector is USB host. The three tables below show the signals on each possible connector.

**Table 6: J14, USB Host Connector**

Pins	Signal
1	USB_VBUS
2	USB_DM
3	USB_DP
4	GND

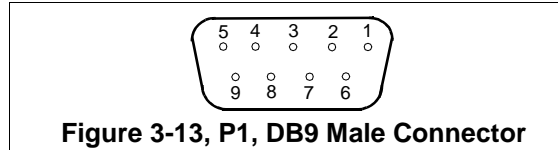
### 3.2.14 J15, +5V Input

Connector J15 is the input power connector. This connector bring in +5 volts to the EVM. This is a 2.5 mm. jack. The figure below shows this connector as viewed from the card edge.



### 3.2.15 P1, RS-232 UART Connector

The TMS320DM6467 EVM has an RS-232 connector which brings out the UART0 transmit, receive, and control signals to be used as UART. This UART uses the MAX3243 RS-232 line driver and is routed to a male 9 pin D-connector, P1. The pin positions for the P1 connector as viewed from the edge of the printed circuit board are shown below.



**Figure 3-13, P1, DB9 Male Connector**

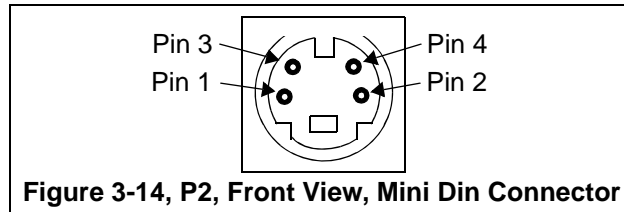
The pin numbers and their corresponding signals are shown in the table below. This corresponds to a DB-9 connector interface used on personal computers.

**Table 7: P1, RS-232 UART Pinout**

Pin #	Signal Name
1	No Connect
2	RXD
3	TXD
4	No Connect
5	GND
6	No Connect
7	RTS
8	CTS
9	No Connect

**3.2.16 P2, Video Out**

Connector P2 is a four pin mini din connector which interfaces to an S-video output display device. The ADV7343 drives this output via a THS7314 video driver. This connector brings out the DAC B and DAC C. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.



**Table 8: P2, Video Out, Mini Din Connector**

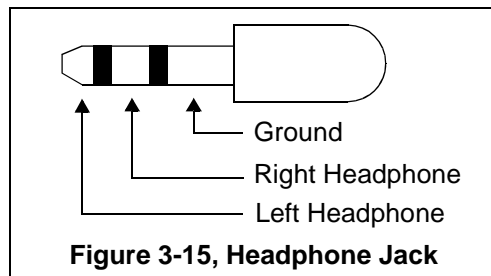
Pin #	Signal Name
1	Ground
2	Ground
3	Luma
4	Chroma

**3.2.17 P3, S/PDIF Out (Optical)**

P3 is an optical transmitter connector used as an output from the McASP1 AxR[0] signal on the TMS320DM6467 DSP. This connector brings out an optical S/PDIF signal. Do **NOT** plug into this connector with the power on.

**3.2.18 P4, Headphone Connector**

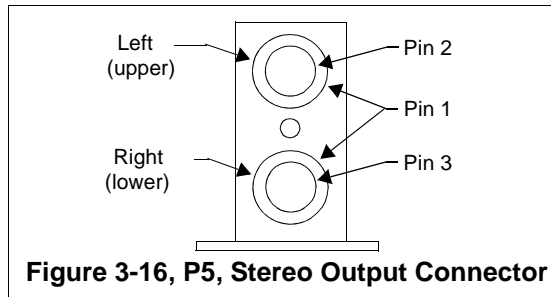
Connector P4 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below.



**Figure 3-15, Headphone Jack**

### 3.2.19 P5, Stereo Line Output Connector

The P5 connector provides a stereo output from the TVL320AIC32 on the EVM. The upper connector is the left channel, and the lower connector is the right channel. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.



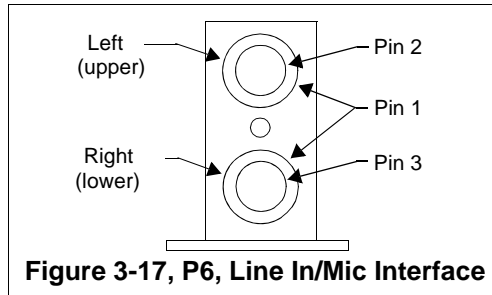
**Figure 3-16, P5, Stereo Output Connector**

**Table 9: P5, Stereo Output Connector**

Pin #	Signal
1	Isolated Ground
2	LEFT_LO+
3	RIGHT_LO+

### 3.2.20 P6, Stereo Line Input Connector

The P6 connector provides a stereo line input to the TVL320AIC32 on the EVM. The upper connector is the left channel, and the lower connector is the right channel. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.



**Figure 3-17, P6, Line In/Mic Interface**

**Table 10: P6, Line In/Mic Interface**

Pin #	Signal	Input
1	Isolated Ground	Mic
2	LINE1L	Mic
3	LINE2L	Mic

### 3.2.21 P7, S-Video In

Connector P7 is a four pin mini din S-video connector which interfaces to the TVP5147 encoder. This connector brings in a video signal (LUMA) to pin 9 on the TVP5147. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

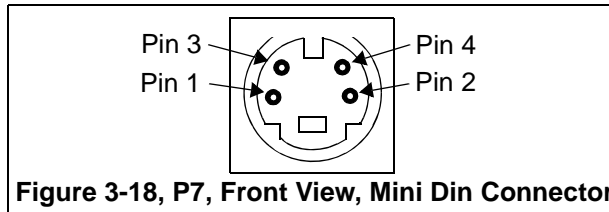


Figure 3-18, P7, Front View, Mini Din Connector

Table 11: P7, Video In, Mini Din Connector

Pin #	Signal Name
1	GND
2	GND
3	LUMA
4	Chroma

### 3.2.22 P8, Microphone Connector

The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

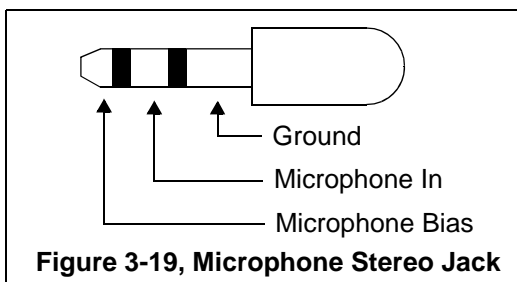


Figure 3-19, Microphone Stereo Jack

**3.2.23 P9, PCI Connector**

The P9 connector is a card edge PCI interface. This connector has an “A” and “B” side. Because of the card seating notches the pin numbers are not contiguous. The “B” side is the top component side. The I/O direction field is referenced from the PCI slot.

**Table 12: P9, PCI Connector, “A” Side**

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	TRST-		Not Used	2	+12 Volts		Not Used
3	TMS		Not Used	4	TDI	I/O	Tied to TDO
5	+5 Volts		+5 Volts Power	6	INTA-	O	Interrupt Out
7	INTC-	O	Interrupt Out	8	+5 Volts		+5 Volts Power
9	Rsvd.0		Not Used	10	+V I/O		Not Used
11	Rsvd.1		Not Used	12	Key.1		Key
13	Key.2		Key	14	+3.3 Vaux		Not Used
15	RST-	I	PCI_Resetn	16	+V I/O	O	Not Used
17	GNT-	O	Grant-	18	GND		Ground
19	PME-			20	AD30	I/O/Z	Address/Data 30
21	+3.3 Volts		Not Used	22	AD28	I/O/Z	Address/Data 28
23	AD26	I/O/Z	Address/Data 26	24	GND		
25	AD24	I/O/Z	Address/Data 24	26	IDSEL	I	Initialization Device Select
27	+3.3 Volts		Not Used	28	AD22	I/O/Z	Address/Data 22
29	AD20	I/O/Z	Address/Data 20	30	GND		Ground
31	AD18	I/O/Z	Address/Data 18	32	AD16	I/O/Z	Address/Data 16
33	+3.3 Volts		Not Used	34	FRAME-	I	Frame
35	GND		Ground	36	TRDY-	I/O/Z	Target Ready
37	GND		Ground	38	STOP-	I/O/Z	Stop Direction
39	+3.3 Volts		Not Used	40	SDONE	O	Done
41	SBO-			42	GND		Ground
43	PAR	I/O/Z	Parity	44	AD15	I/O/Z	Address/Data 15
45	+3.3 Volts		Not Used	46	AD13	I/O/Z	Address/Data 13
47	AD11	I/O/Z	Address/Data 11	48	GND		Ground
49	AD9	I/O/Z	Address/Data 9	50	Key.3		Key
51	Key.4		Key	52	C/BE0		Command/Byte Enable0
53	+3.3 Volts		Not Used	54	AD6	I/O/Z	Address/Data 6
55	AD4	I/O/Z	Address/Data 4	56	GND		Ground
57	AD2	I/O/Z	Address/Data 2	58	AD0	I/O/Z	Address/Data 0
59	+V I/O		Not Used	60	REQ64-		Not Used
61	+5 Volts		+5 Volts Power	62	+5 Volts		+5 Volts Power



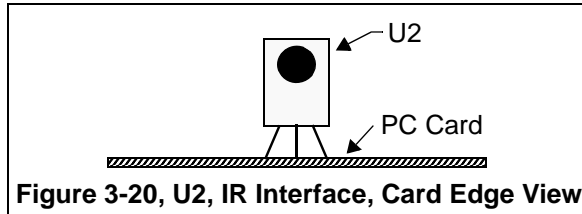
The signals on the “B” side of the connector are shown in the table below.

**Table 13: P9, PCI Connector, “B” Side**

Pin	Signal	I/O	Description	Pin	Signal	I/O	Description
1	-12 Volts		Not Used	2	TCK	I	Not Used
3	GND		Ground	4	TDO	I	Tied to TDO
5	+5 Volts		+5 Volt Power	6	+5 Volts	I	+5 Volt Power
7	INTB-		Interrupt OUT	8	INTD-		Interrupt Out
9	PRSNT1-	O	Power Requirement	10	Rsvd.2		
11	PRSNT2-	O	Power Requirement	12	Key.5		Key
13	Key.6		Key	14	Rsvd.3		
15	GND		Ground	16	CLK		System Clock
17	GND		Ground	18	REQ-		
19	+V I/O		Not Used	20	AD31	I/O/Z	Address/Data 31
21	AD29	I/O/Z	Address/Data 29	22	GND		Ground
23	AD27	I/O/Z	Address/Data 27	24	AD25	I/O/Z	Address/Data 25
25	+3.3 Volts		Not Used	26	C/BE3	I/O/Z	Command/Byte Enable 3
27	AD23	I/O/Z	Address/Data 23	28	GND		Ground
29	AD21	I/O/Z	Address/Data 21	30	AD19	I/O/Z	Address/Data 19
31	+3.3 Volts		Not Used	32	AD17	I/O/Z	Address/Data 17
33	C/BE2-	I/O/Z	Command/Byte Enable 2	34	GND		Ground
35	IRDY-	I	Initiator Ready	36	+3.3 Volts		Not Used
37	DEVSEL-	I/O/Z	Device Select	38	GND		Ground
39	LOCK-	I	Resource Locked	40	PERR-	I/O/Z	Parity Error
41	+3.3 Volts		Not Used	42	SERR-	O	System Error
43	+3.3 Volts		Not Used	44	C/BE1-	I/O/Z	Command/Byte Enable 1
45	AD14	I/O/Z	Address/Data 14	46	GND		Ground
47	AD12	I/O/Z	Address/Data 12	48	AD10	I/O/Z	Address/Data 10
49	M66EN	O	66 Mhz Enable	50	Key.7		Key
51	Key.8		Key	52	AD8	I/O/Z	Address/Data 8
53	AD7	I/O/Z	Address/Data 7	54	+3.3 Volts		Not Used
55	AD5	I/O/Z	Address/Data 5	56	AD3	I/O/Z	Address/Data 3
57	GND		Ground	58	AD1	I/O/Z	Address/Data 1
59	+V I/O		Not Used	60	ACK64-		Not Used
61	+5 Volts		+5 Volt Power	62	+5 Volts		+5 Volt Power

### 3.2.24 U2, IR Interface

Interface U2 provides an Infrared interface to the TMS320DM6467 EVM. This is a receiver only for consumer remote controls. The view of U2 is shown from a board edge view in the figure below.



**Figure 3-20, U2, IR Interface, Card Edge View**

### 3.2.25 JP1, Downstream VLYNQ Connector

The JP1 is a 50 pin SAMTEC FTSH-125-01-L-DV-EJ-K connector which allows the user to connect the VLYNQ interface to up stream VLYNQ interfaces. The pinout for the JP1 connector is shown in the table below.

**Table 14: JP1, VLYNQ Header**

Pin #	Signal	Pin #	Signal
1	VLYNQ_SCRUN	2	GROUND
3	VLYNQ_RESETn	4	GROUND
5	VCC_5V	6	GROUND
7	VCC_5V	8	GROUND
9	NC	10	GROUND
11	NC	12	GROUND
13	NC	14	GROUND
15	NC	16	GROUND
17	VLYNQ_RXD3	18	GROUND
19	VLYNQ_RXD2	20	GROUND
21	VLYNQ_RXD1	22	UVLYNQ WS2
23	VLYNQ_RXD0	24	UVLYNQ WS1
25	VLYNQ_CLK	26	UVLYNQ WS0
27	VLYNQ_TXD0	28	UVLYNQ WS1
29	VLYNQ_TXD1	30	UVLYNQ WS2
31	VLYNQ_TXD2	32	GROUND
33	VLYNQ_TXD3	34	GROUND
35	NC	36	GROUND
37	NC	38	GROUND
39	NC	40	GROUND
41	NC	42	GROUND
43	VCC_5V	44	GROUND
45	VCC_5V	46	GROUND
47	NC	48	GROUND
49	NC	50	GROUND

### 3.2.26 JP2, ATA Interface Connector

The JP1 connector is located on the bottom side of the board and is used to provide an ATA interface to a hard disk drive. This is a 2 x 22 2mm. pin male connector. The pinout for the JP1 connector is shown in the table below.

**Table 15: JP2, ATA Interface**

Pin #	Signal	Pin #	Signal
1	ATA RESETn	2	GND
3	ATA.DD7	4	ATA.DD8
5	ATA.DD6	6	ATA.DD9
7	ATA.DD5	8	ATA.DD10
9	ATA.DD4	10	ATA.DD11
11	ATA.DD3	12	ATA.DD12
13	ATA.DD2	14	ATA.DD13
15	ATA.DD1	16	ATA.DD14
17	ATA.DD0	18	ATA.DD15
19	GND	20	NC
21	ATA.DMARQ	22	GND
23	ATA.DIOW	24	GND
25	ATA.DIOR	26	GND
27	ATA.IORDY	28	ATA_CSEL, TP34
29	ATA.DMACK	30	GND
31	ATA.INTRQ	32	GND
33	ATA.DA1	34	TP33
35	ATA.DA0	36	ATA.DA2
37	ATA.CS0	38	ATA.CS1
39	ATA.DASPN	40	GND
41	VCC_5V	42	VCC_5V
43	GND	44	NC

### 3.2.27 DC\_P1, Ethernet Interface Connector

The DC\_P1 is a high speed SAMTEC connector allows the user to interface to the Ethernet logic on the TMS320DM6467 EVM. The pinout for the DC\_P1 connector is shown in the table below.

**Table 16: DC\_P1, Ethernet Interface Connector**

Pin #	Signal	Pin #	Signal
1	MII_MTXD0	2	MII_MTXD1
3	MII_MTXD2	4	MII_MTXD3
5	MII_MTXD4	6	MII_MTXD5
7	MII_MTXD6	8	MII_MTXD7
9	GROUND	10	GROUND
11	MII_MRXD6	12	MII_MRXD7
13	MII_MRXD4	14	MII_MRXD5
15	MII_MRXD2	16	MII_MRXD3
17	MII_MRXD0	18	MII_MRXD1
19	GROUND	20	GROUND
21	NC	22	NC
23	MII_MRXDV	24	NC
25	GROUND	26	MII_MRXR
27	MII_MRCLK	28	MII_MCOL
29	GROUND	30	GROUND
31	MII_MCRS	32	NC
33	GROUND	34	GROUND
35	NC	36	MII_MTCLK
37	NC	38	GROUND
39	GROUND	40	MDIO_MDIO
41	MII_RFTCLK	42	MDIO_MDCLK
43	GROUND	44	GROUND
45	MII_MTXEN	46	MII_GMTCLK
47	NC	48	GROUND
49	MAC_ENABLE *	50	NC
51	NC	52	NC
53	GROUND	54	GROUND
55	VCC_3V3	56	VCC_3V3
57	GROUND	58	GROUND
59	VCC_5V	60	VCC_5V

\* The MAC\_ENABLE signal disables the on board PHY when pulled to +3.3 volts.

**3.2.28 DC\_P2, Video Expansion Connector**

The DC\_P2 is a 120 pin SAMTEC high speed connector allows the user to interface to the video logic on the TMS320DM6467 EVM. The pinout for the pins 1-60 of the DC\_P2 connector are shown in the table below.

**Table 17: DC\_P2, Video Expansion Connector, Pins 1-60**

Pin #	Signal	Pin #	Signal
1	NC	2	VPIF_CLKOUT2
3	GROUND	4	GROUND
5	NC	6	NC
7	GROUND	8	GROUND
9	VPIF_DOUT1	10	VPIF_DOUT0
11	VPIF_DOUT3	12	VPIF_DOUT2
13	VPIF_DOUT5	14	VPIF_DOUT4
15	VPIF_DOUT7	16	VPIF_DOUT6
17	GROUND	18	GROUND
19	VPIF_DOUT9	20	VPIF_DOUT8
21	VPIF_DOUT11	22	VPIF_DOUT10
23	VPIF_DOUT13	24	VPIF_DOUT12
25	VPIF_DOUT15	26	VPIF_DOUT14
27	GROUND	28	GROUND
29	VIDEO_OUT_EN1 **	30	VIDEO_OUT_EN0 *
31	GROUND	32	GROUND
33	VPIF_CLKIN3	34	VPIF_CLKIN2
35	GROUND	36	GROUND
37	VPIF_CLKOUT3	38	VPIF_CLKIN2_EN
39	GROUND	40	GROUND
41	PTSI_CLK	42	STSI_CLK
43	GROUND	44	GROUND
45	DC_VOXO_CLK_EN	46	DC_ALT_VOXO_EN
47	DC_VOXO_CLK	48	DC_ALT_VOXO
49	GROUND	50	GROUND
51	UART0_RIN	52	UART0_DCDn
53	UART0_DSRn	54	UART0_DTRn
55	UART0_CTSn	56	UART0_RTSn
57	UART0_TXD	58	UART0_RXD
59		60	UART0_EN

\* VIDEO\_OUT\_EN0 disables on board video port low VPIF\_DOUT0 - VPIF\_DOUT7 and VPIF\_CLKOUT2 when pulled high.

\*\* VIDEO\_OUT\_EN1 disables on board video port low VPIF\_DOUT8 - VPIF\_DOUT15 and VPIF\_CLKOUT3 when pulled high.

The pinout for the pins 61-120 of the DC\_P2 connector are shown in the table below.

**Table 18: DC\_P2, Video Expansion Connector, Pins 61-120**

Pin #	Signal	Pin #	Signal
61	GROUND	62	GROUND
63	UART1_CTSn	64	UART1_RTSn
65	UART1_TXD	66	UART1_RXD
67	GROUND	68	GROUND
69	UART2_CRG_EN_30	70	UART2_EN *****
71	UART2_CTSn	72	UART2_RTsn
73	UART2_TXD	74	UART2_RXD
75	GROUND	76	GROUND
77	I2C_SDA	78	I2C_SCL
79	PWM1	80	PWM0_CRG0
81	GROUND	82	PWM_EN
83	CLKOUT0	84	SYS_RESEtN
85	GROUND	86	NC
87	VIDEO_IN_EN1 ****	88	VIDEO_IN_EN0 ***
89	GROUND	90	GROUND
91	VPIF_CLKIN1	92	VPIF_CLKIN0
93	GROUND	94	GROUND
95	VPIF_DIN1	96	VPIF_DIN0
97	VPIF_DIN3	98	VPIF_DIN2
99	VPIF_DIN5	100	VPIF_DIN4
101	VPIF_DIN7	102	VPIF_DIN6
103	GROUND	104	GROUND
105	VPIF_DIN9	106	VPIF_DIN8
107	VPIF_DIN11	108	VPIF_DIN10
109	VPIF_DIN13	110	VPIF_DIN12
111	VPIF_DIN15	112	VPIF_DIN14
113	GROUND	114	GROUND
115	VCC_3V3	116	VCC_3V3
117	GROUND	118	GROUND
119	VCC_5V	120	VCC_5V

\*\*\* VIDEO\_IN\_EN0 disables on board video input port VPIF\_DIN0 - VPIF\_DIN7 when pulled high.

\*\*\*\* VIDEO\_IN\_EN1 disables on board video input port VPIF\_DIN8 - VPIF\_DIN15 when pulled high.

\*\*\*\*\* UART2\_EN disables on board UART when pulled high.

### 3.2.29 DC\_P3, I/O Expansion Connector

The DC\_P3 connector allows the user to interface to the I/O logic on the TMS320DM6467 EVM. The pinout for the pins 1-60 of the DC\_P3 connector are shown in the table below.

**Table 19: DC\_P3, I/O Expansion Connector, Pins 1-60**

Pin #	Signal	Pin #	Signal
1	SYS_RESET	2	
3	I2C_DCL	4	
5	GROUND	6	GROUND
7	MCASP0_AHCLKR	8	MCASP0_ACLKR
9	MCASP0_AHCLKX	10	MCASP0_ACLKX
11	MCASP0_AMUTE	12	MCASP0_AFSR
13	MCASP0_AFSX	14	MCASP0_AMUTEIN
15	MCASP0_AXR[3]	16	MCASP0_AXR[2]
17	MCASP0_AXR[1]	18	MCASP0_AXR[0]
19	DC_AUDIO_CLK_OUT	20	AUDIO_CLK_EN
21	GROUND	22	GROUND
23	SPI_MOSI	24	SPI_MISO
25	SPI_SCS1	26	SPI_EN
27	SPI_SCS0	28	SPI_SCLK
29	GROUND	30	GROUND
31	SPI_ENABLE	32	TOUT4
33	TIMER_EN	34	TOUT3
35	TIN0	36	TOUT2
37	TIN1	38	TOUT1
39	TIN2	40	TOUT0
41	GROUND	42	GROUND
43	GPO7	44	GPO6
45	DC_GPIO5	46	GPO4
47	GPO3	48	GPO2
49	GPO1	50	GPO0
51	EMIF_MODE	52	GROUND
53	DC_GPIO10	54	DC_GPIO11_EMCS5n
55	DC_GPIO12_EMCSN4n	56	DC_EMRnW
57	DC_HD30_EMA14	58	DC_HD31_EMA15
59	DC_HD28_EMA12	60	DC_HD29_EMA13



The pinout for the pins 61-120 of the DC\_P3 connector are shown in the table below.

**Table 20: DC\_P3, I/O Expansion Connector, Pins 61-120**

Pin #	Signal	Pin #	Signal
61	DC_HD26_EMA10	62	DC_HD27_EMA11
63	DC_HD24_EMA8	64	DC_HD25_EMA9
65	DC_HD22_EMA6	66	DC_HD23_EMA7
67	DC_HD20_EMA4	68	DC_HD21_EMA5
69	DC_HD18_EMA2	70	DC_HD19_EMA3
71	DC_HD16_EMA0	72	DC_HD17_EMA1
73	GROUND	74	GROUND
75	DC_HDS2n_EMCS2n	76	DC_HRWn_EMCS3n
77	DC_HINTn_EMBA0	78	DC_HRDYn_EMA17
79	DC_HHWILn_EMA16	80	DC_HNCT1_EMBA1
81	DC_HDS1n_EM_OEn	82	DC_HCNTL0_EMWENn
83	DC_HASn_EMDQM0n	84	DC_HCSn_EMDQM1n
85	NC	86	NC
87	DC_GPIO19_EMWAIT3	88	DC_GPIO18_EMA23
89	DC_GPIO17_EMA20	90	DC_GPIO16_EMA21
91	ATA_DA2_GPIO13_EMA22	92	XDK_B_EM_WAIT0
93	ATA_IORDY_GPIO21_EMWAIT1	94	ATA_DIOW_GPIO20_EMWAIT2
95	DC_GPIO33_EMA18	96	DC_GPIO32_EMA19
97	GROUND	98	GROUND
99	DC_HD14_EMD14	100	DC_HD15_EMD15
101	DC_HD12_EMD12	102	DC_HD13_EMD13
103	DC_HD10_EMD10	104	DC_HD11_EMD11
105	DC_HD8_EMD8	106	DC_HD9_EMD9
107	DC_HD6_EMD6	108	DC_HD7_EMD7
109	DC_HD4_EMD4	110	DC_HD5_EMD5
111	DC_HD2_EMD2	112	DC_HD3_EMD3
113	DC_HD0_EMD0	114	DC_HD1_EMD1
115	VCC_3V3	116	VCC_3V3
117	GROUND	118	GROUND
119	VCC_5V	120	VCC_5V

### 3.3 LEDs

The TMS320DM6467 EVM has SIX (6) LEDs. Four of these LEDs (DS1-4) are under user control and addressed over the I<sup>2</sup>C bus. LED DS5 indicates the presence of +5 volts on the board. LED DS6 indicates the power has been turned on via SW4. The LED functions are summarized in the table below.

**Table 21: LEDs**

LED #	Use	Color
DS1	User Defined	Green
DS2	User Defined	Green
DS3	User Defined	Green
DS4	User Defined	Green
DS5	Disk Drive Activity	Green
DS6	+5V On	Green

### 3.4 Switches

The TMS320DM6467 EVM has five (5) switches. These switches are used to create certain actions on the board or to select certain functions on the board. The switch functions are summarized in the table below.

**Table 22: Switches**

SW #	Function
SW1	Power On Reset Switch
SW2	4 Position User Readable
SW3	Boot Mode/Muxing Configuration
SW4	+5 Volt Power Switch
S1	EMU0/1 Select Switch

#### 3.4.1 SW1, Power On Reset Switch

Switch SW1 is a momentary switch that asserts power on reset to the TMS320DM6467 device, and the on board devices.

### 3.4.2 SW2, 4 Position User Readable

Switch SW2 is a 4 position bank of user readable switches via the I<sup>2</sup>C expander. The individual switches can be placed in any position and read by the user software from the expander. See the section on I<sup>2</sup>C expanders for more information.

### 3.4.3 SW3, Boot Mode/Muxing Configuration

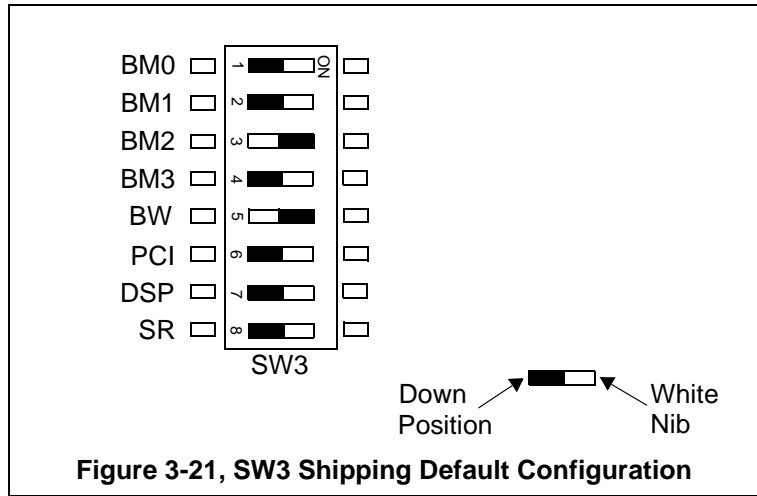
Switch SW3 is an 8 position switch used to select the source of the bootload and configuration. Four (4) of the eight (8) positions are used for the boot mode. The selections are shown in the table below.

**Table 23: SW3, Bootload Mode Select**

Boot Mode Pin	SW3[4:1]	Boot Description
0000	1111	No Boot (Emulation Mode)
0001	1110	Reserved
0010	1101	HPI Boot (16-bit width) (if PCIEN=0)
0010	1101	PCI Boot without auto-initialization (if PCIEN=1)
0011	1100	HPI Boot (32-bit width) (if PCIEN=0)
0011	1100	PCI Boot with auto-initialization (if PCIEN=1)
0100	1011	EMIFA Direct Boot (ROM/NOR) (PCIEN=0)
0101	1010	Reserved
0110	1001	I <sup>2</sup> C Boot
0111	1000	NAND Flash Boot (PCIEN=0)
1000	0111	UART0 Boot
1001	0110	Emulation Boot
1010	0101	VLYNQ Boot
1011	0100	EMAC Boot
1100	0011	Reserved
1101	0010	Reserved
1110	0001	SPI Boot
1111	0000	Reserved

x = don't care, \* these boot modes must be accompanied with FASTBOOT = 1.

The figure below shows the as shipped boot configuration for SW3, booting from Flash ROM.



**Figure 3-21, SW3 Shipping Default Configuration**

SW3, Position 5, sets the EMIF A data bus width at reset. If the switch is UP or “0” on the “ON” side EMIF A is 8 bit data bus CS2. When the switch is in the DOWN or “1” EMIF A is a 16 bit data bus for CS2. These two positions are shown in the table below.

**Table 24: SW3, Position 5, BW**

ON Side	Pin	Function
Up	“0”	EMIF A is 8 bit data bus for CS2
Down	“1”	EMIF A is 16 bit data bus for CS2

SW3, Position 6, is the PCI enable switch that configures the DM6467 pin muxing. When the switch has the “ON” side in the “UP” position as shown above pin muxing defaults to EMIF or HPI. If the switch has the “ON” side pushed down PCI pin multiplexing is enabled on the DM6467. These two positions are shown in the table below.

**Table 25: SW3, Position 6, PCI**

ON Side	Pin	Function
Up	“0”	Pin muxing defaults to EMIF or HPI
Down	“1”	PCI pin multiplexing enabled on DM6467

SW3, Position 7, is the DSP switch that allows the user to control the DSP booting. If the switch has the “ON” side pushed “DOWN” the DSP boots via EMIF A if ARM HPI or PCI boot mode is not enabled. When the switch has the “ON” side “UP” position the DSP is booted via the ARM. These two positions are shown in the table below.

**Table 26: SW3, Position 7, DSP**

ON Side	Pin	Function
Up	“0”	DSP is booted via the ARM processor
Down	“1”	DSP is booted via EMIF A if ARM HPI or PCI boot mode is not enabled

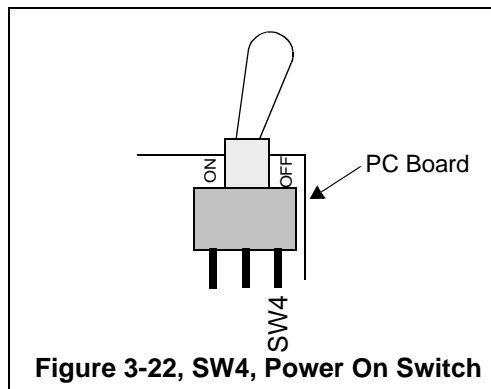
SW3, Position 8, is the SR switch that allows the user to enable the core voltage adjustment on two of the GPIO pins. If the switch has the “ON” pushed down GPIO pins 6 and 7 are core voltage enabled. When the switch has the “ON” side “UP” GPIO pins 6 and 7 assume their standard function. These two positions are shown in the table below.

**Table 27: SW3, Position 8, SR**

ON Side	Pin	Function
Up	“0”	GPIO6 and GPIO7 Standard Function
Down	“1”	GPIO6 and GPIO7 Core Voltage Enabled

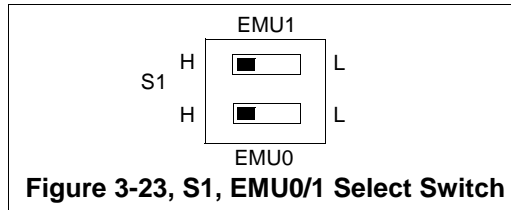
#### 3.4.4 SW4, Power On Switch

Switch SW4 is toggle switch. when moved to the on position power is supplied to the components on the board.



### 3.4.5 S1, EMU0/1 Select Switch

S1 is a 2 position DIP switch providing 4 options in selecting the state of the EMU0 and EMU1 pins on the processor. A view of the switch is shown in the figure below. The selection options with this switch are in the table below.



**Table 28: S1, EMU0/1 Select**

State at Reset EMU0      EMU1		Function
L	L	Emulation Debug ARM JTAG Enabled
L	H	Not Defined
H	L	Not Defined
H	H	Emulation Debug * Both ARM & DSP JTAG Enabled

\* is the factory shipped configuration

### 3.5 Test Points

The EVM has 43 test points. All test points appear on the top of the board. The following figure identifies the position of each test point. the next table list each test point and the signal appearing on that test point.

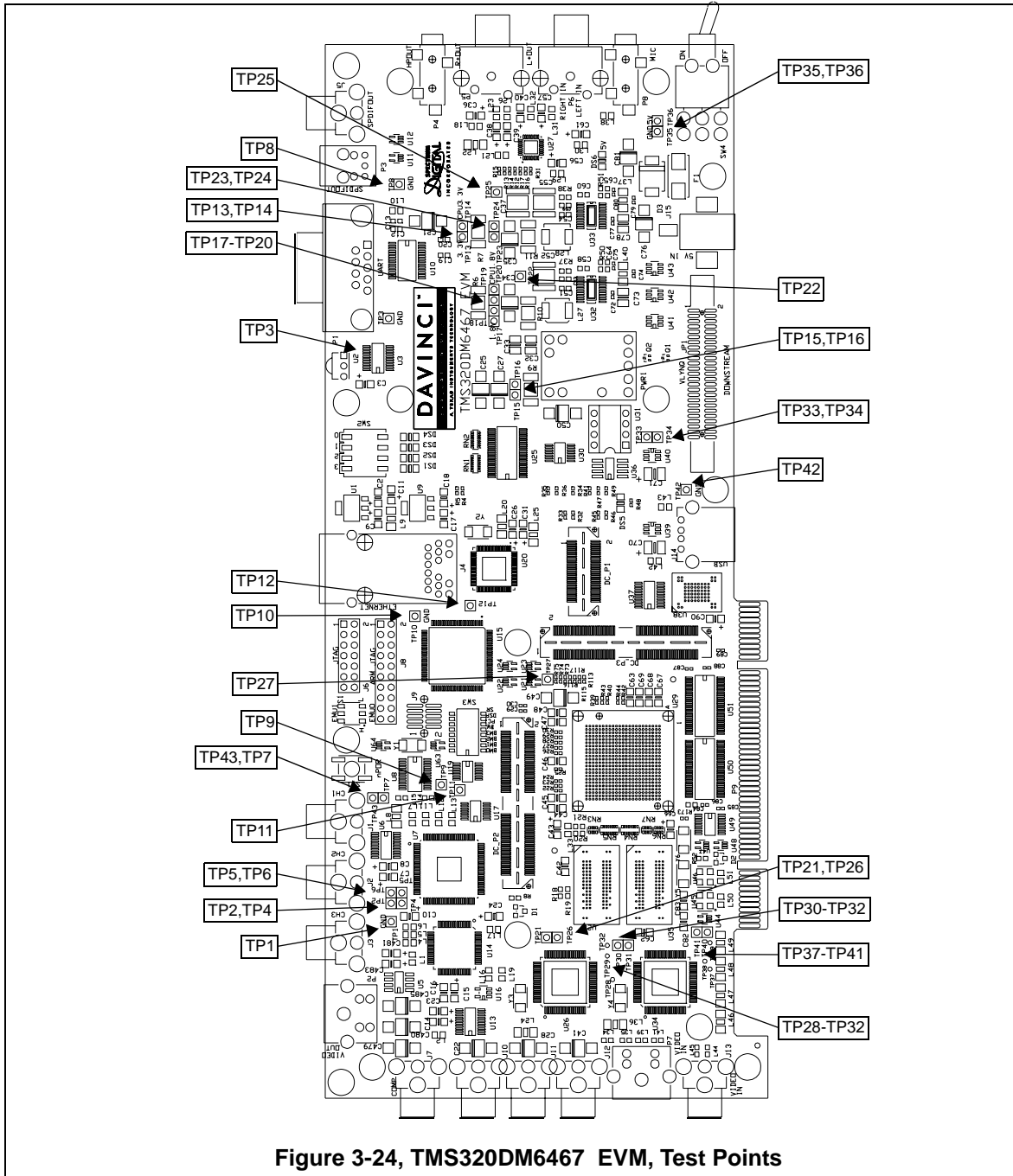


Figure 3-24, TMS320DM6467 EVM, Test Points

**Table 29: TMS320DM6467 EVM Test Points**

Test Point #	Signal	Test Point #	Signal
TP1	GROUND	TP23	VCC_3V3
TP2	TVP7002 HSYNC Output	TP24	3.3 Volt Output
TP3	GROUND	TP25	3.# Volt Power Good
TP4	TVP7002 SYNC Green Output	TP26	TVP5147 (U26) Vertical Sync Output
TP5	TVP7002 VSYNC Output	TP27	ACLKX1
TP6	TVP7002 Frame ID Output	TP28	INTREQ, TVP5147, U26
TP7	CDCE949 VCXO Input	TP29	AVID/GPIO, TVP5147, U26
TP8	GROUND	TP30	TVP5147 (U34) Horizontal Sync Output
TP9	CDCE949 Y6 Clock Output	TP31	TVP5147 (U34) Vertical Sync Output
TP10	GROUND	TP32	GLCO/I2CA, TVP5147, U26
TP11	TVP7002 External Clock Pin	TP33	ATA_CSEL
TP12	ET1011C Enet PHY Interrupt Pin	TP34	Pin 34, JP2
TP13	VCC_3V3	TP35	GROUND
TP14	CPU_3.3V	TP36	VCC_5V
TP15	CPU_1.2V	TP37	INTREQ, TVP5147, U34
TP16	1.2Volt Output from PTH08T240 Module	TP38	AVID/GPIO, TVP5147, U34
TP17	VCC_1V8	TP39	GLCO/I2CA, TVP5147, U34
TP18	VCC_1V8	TP40	GROUND
TP19	1.8 Volt Output	TP41	RSV5
TP20	CPU_1.8V	TP42	GROUND
TP21	TVP5147 (U26) Horizontal Sync Output	TP43	CDCE949 Y9 Clock Output
TP22	1.8 Volt Power good		



# Appendix A

## Schematics

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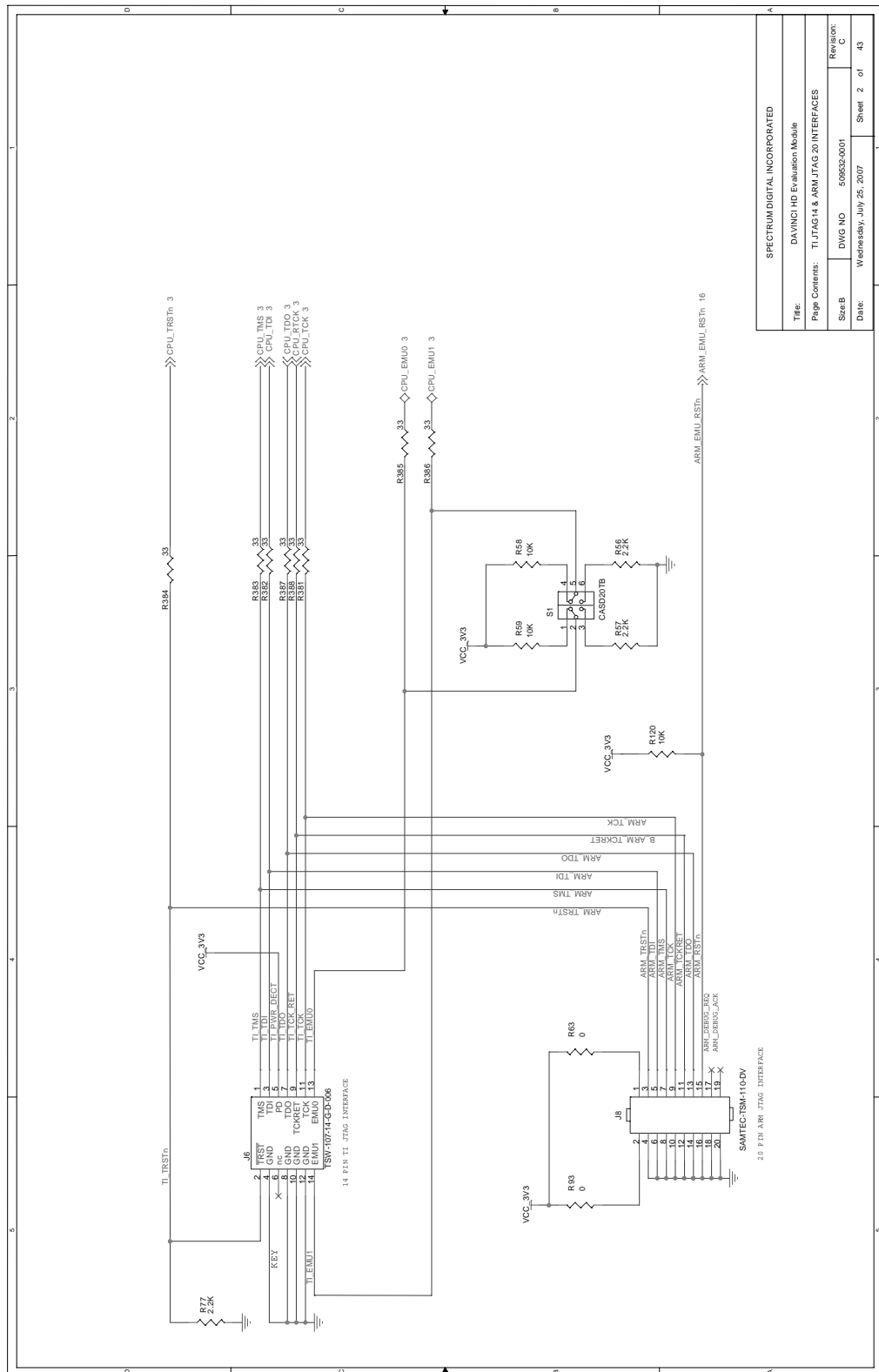
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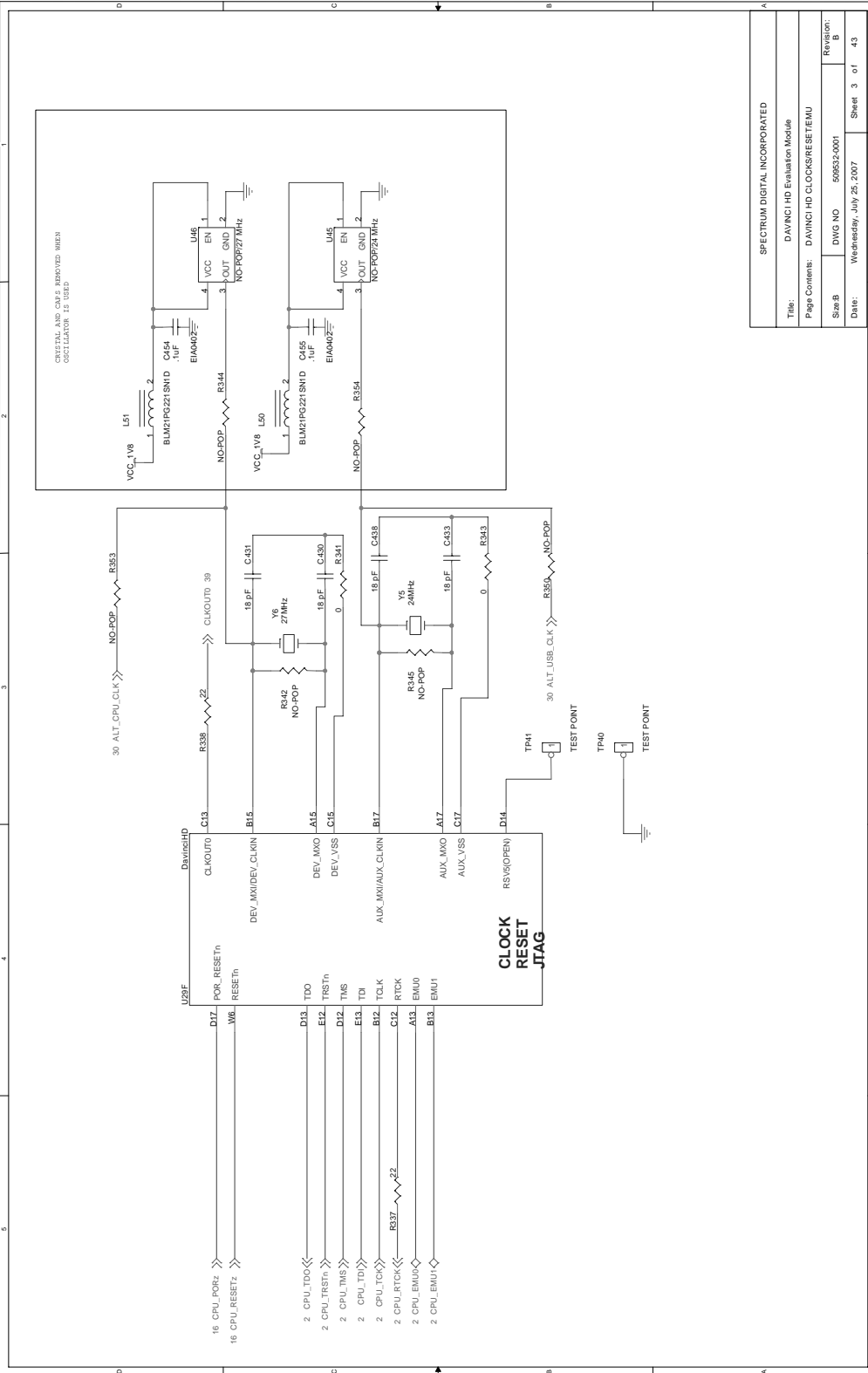
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This appendix contains the schematics for the TMS320DM6467 EVM.

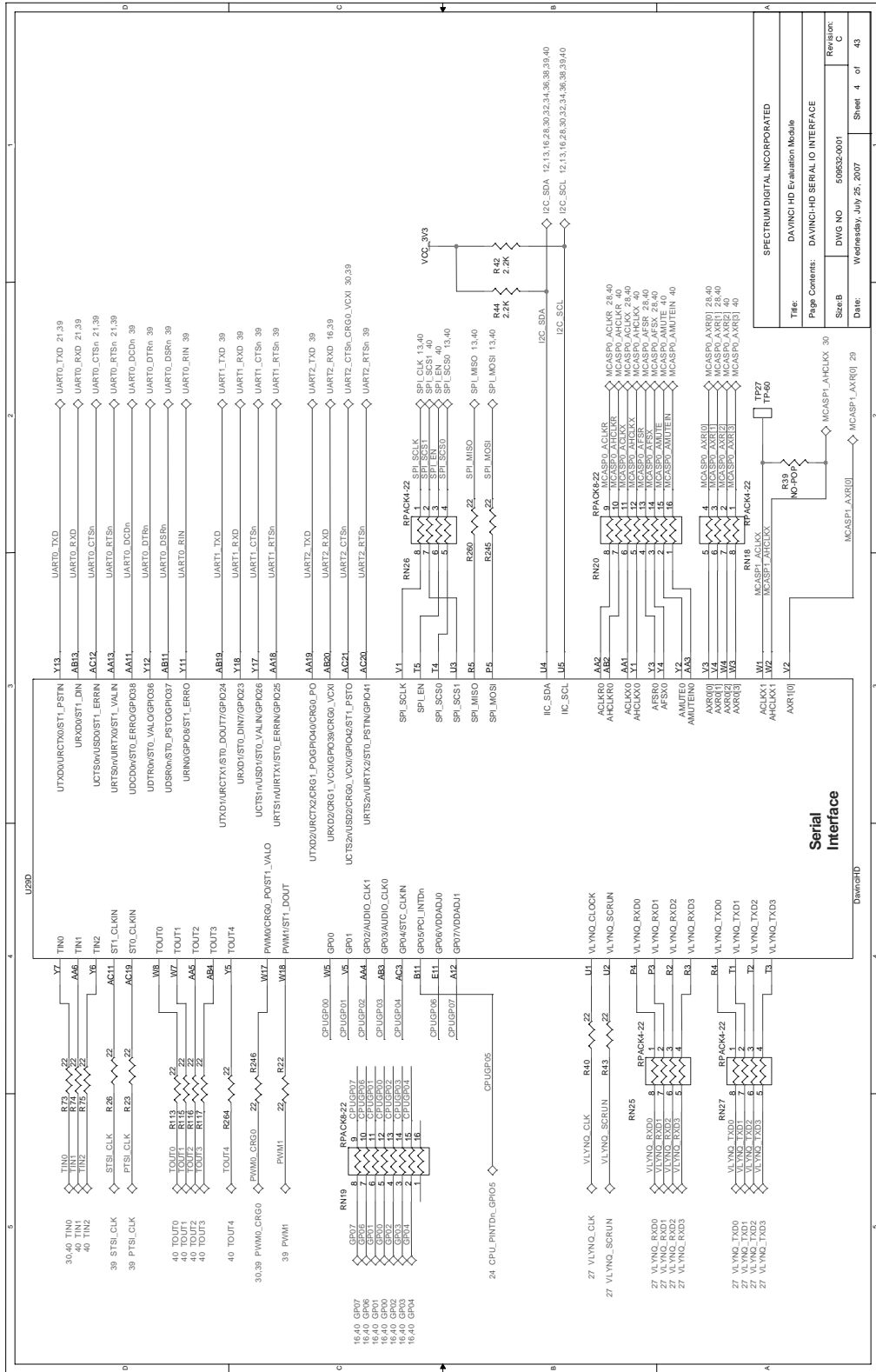




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Size:	DWG NO 50652-001
Date:	Wednesday, July 25, 2007
Revision:	C
Sheet	2 of 43

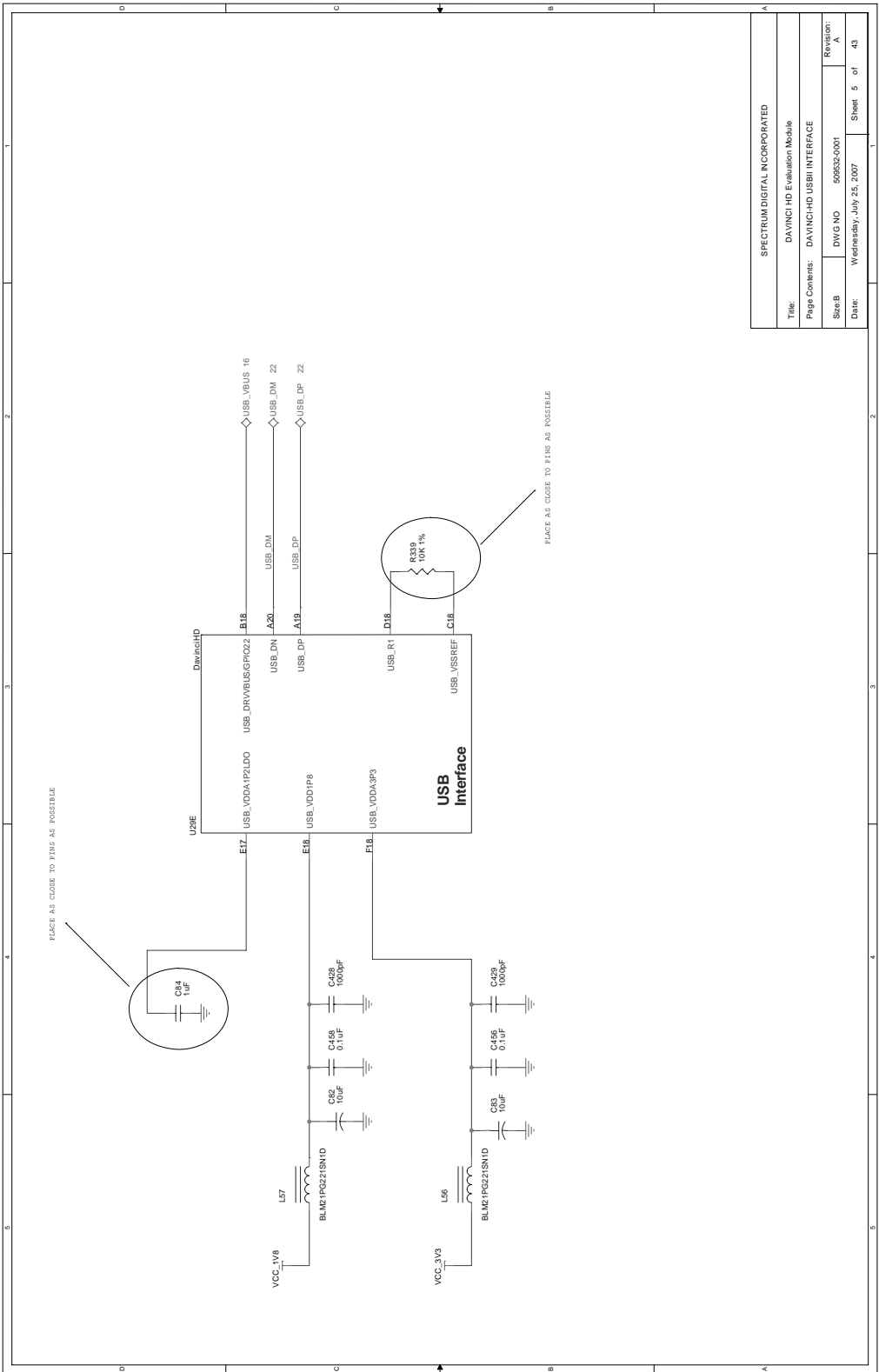


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Size B	DWG NO	509532-0001	Revision: B
Date:	Wednesday, July 25, 2007		
	Sheet	3	of 43

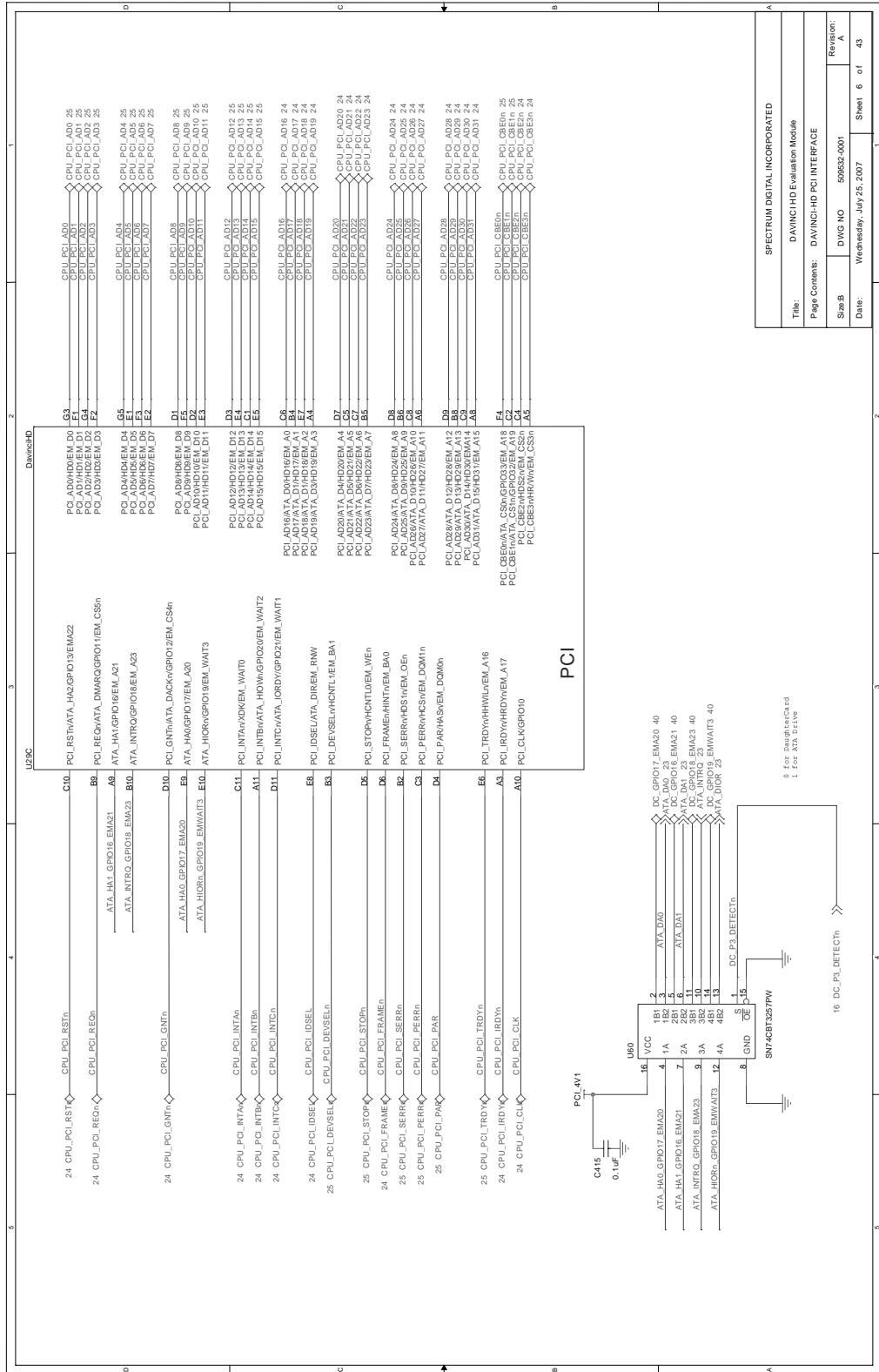


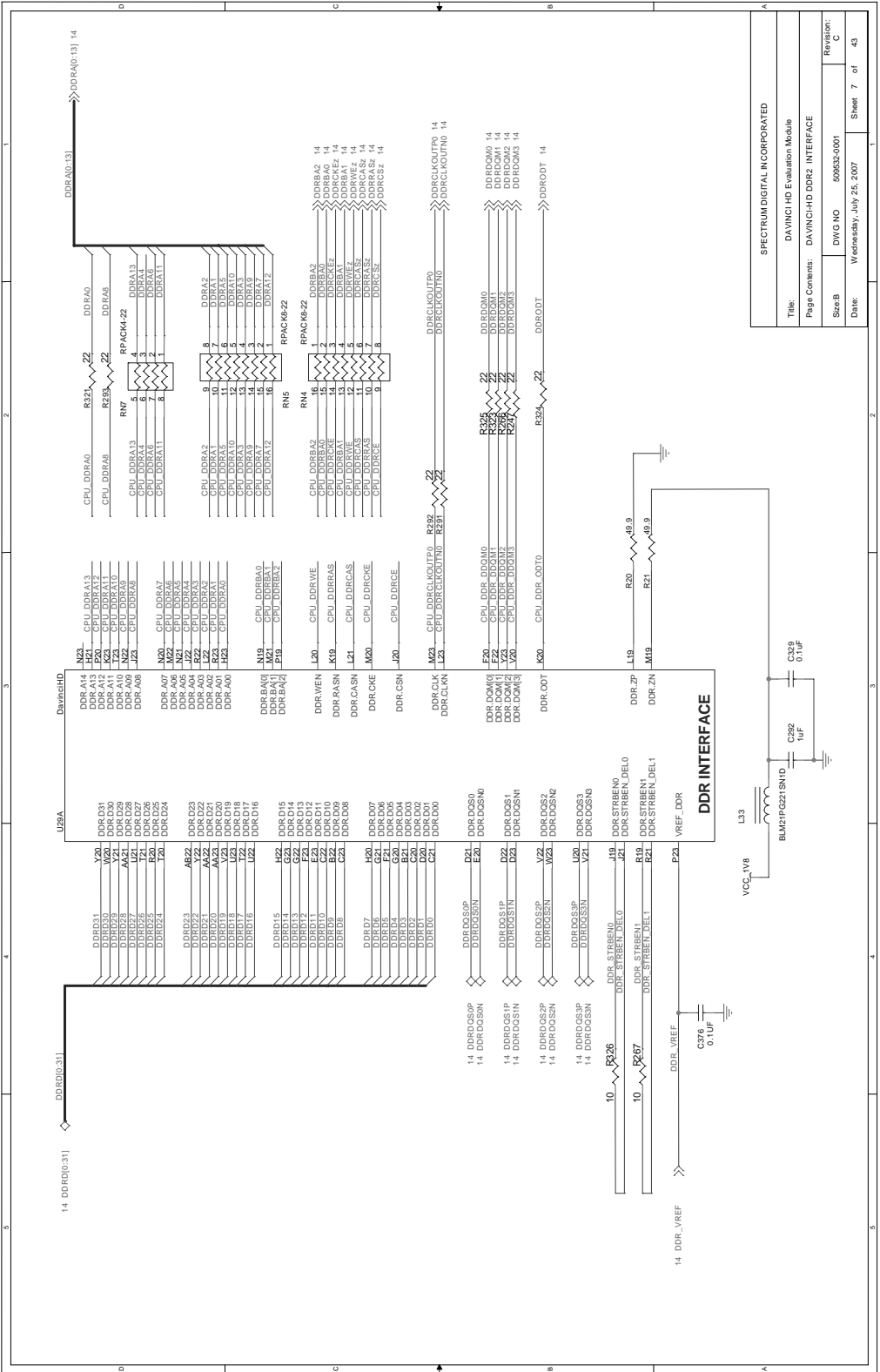
Serial Interface

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Date:	Wednesday, July 25, 2007	Sheet:	4 of 43



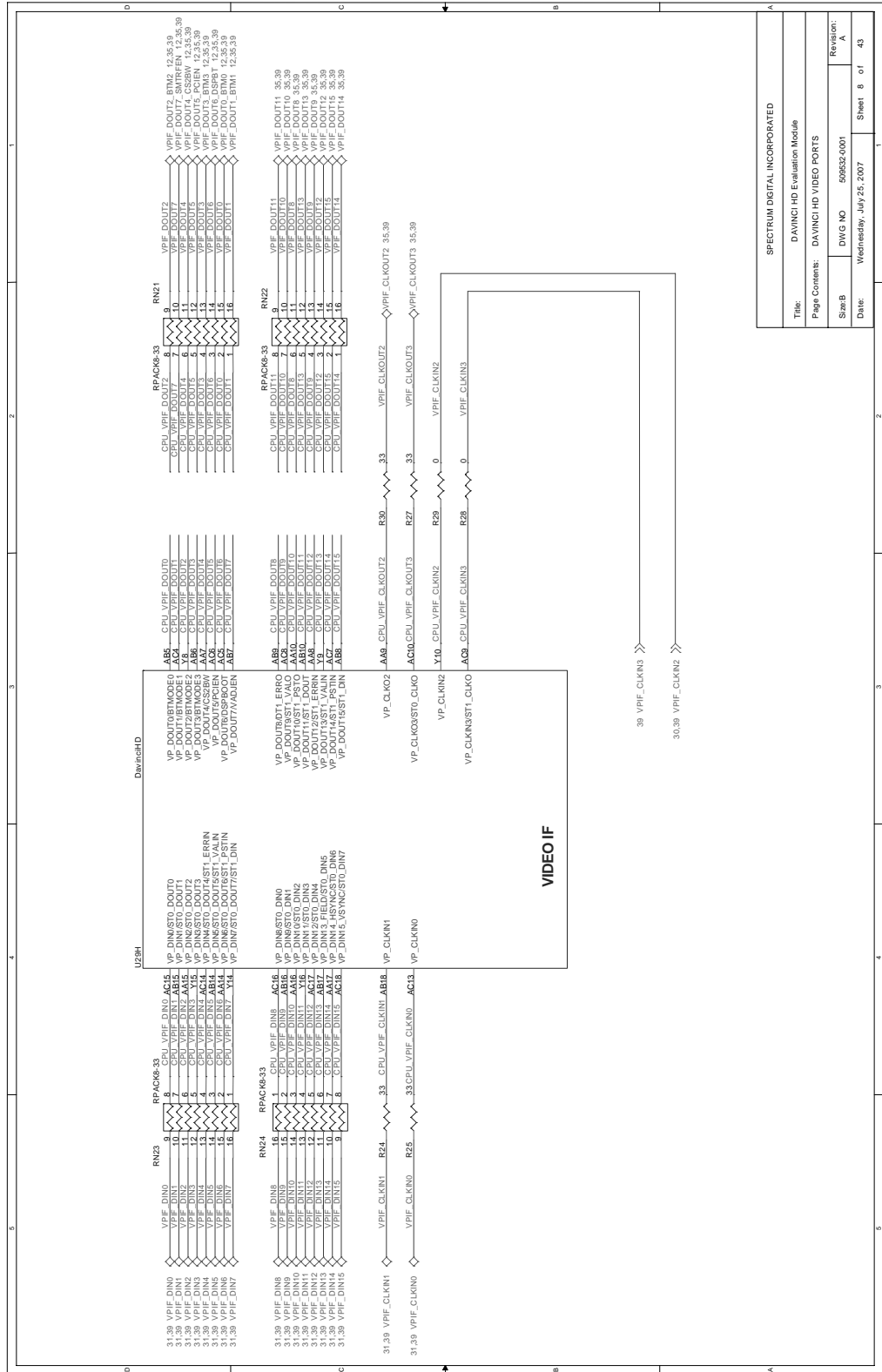
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SizeB:	DWG NO 59953-0001
Date:	Wednesday, July 25, 2007
Revision:	A
Sheet	5 of 43



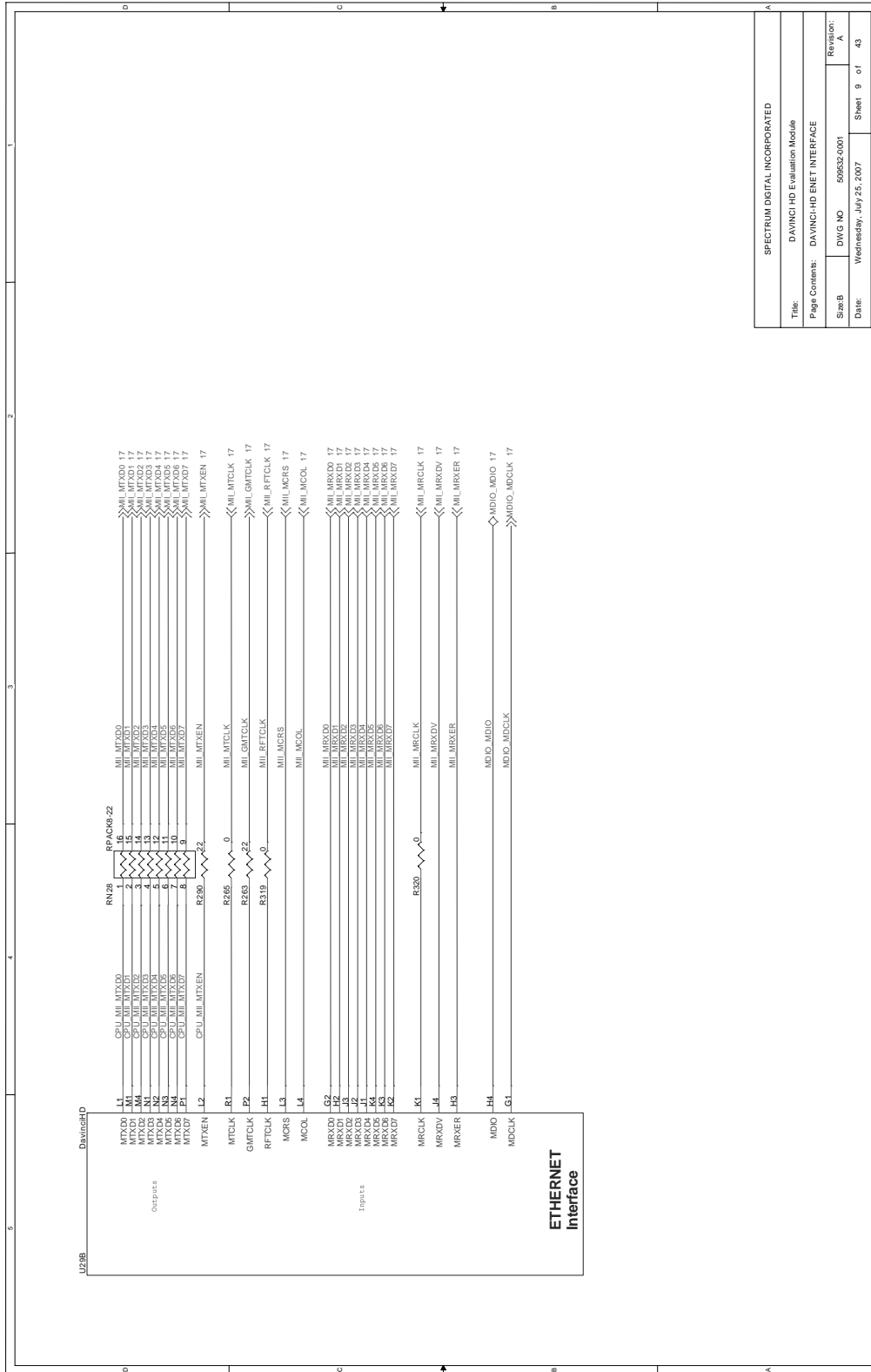


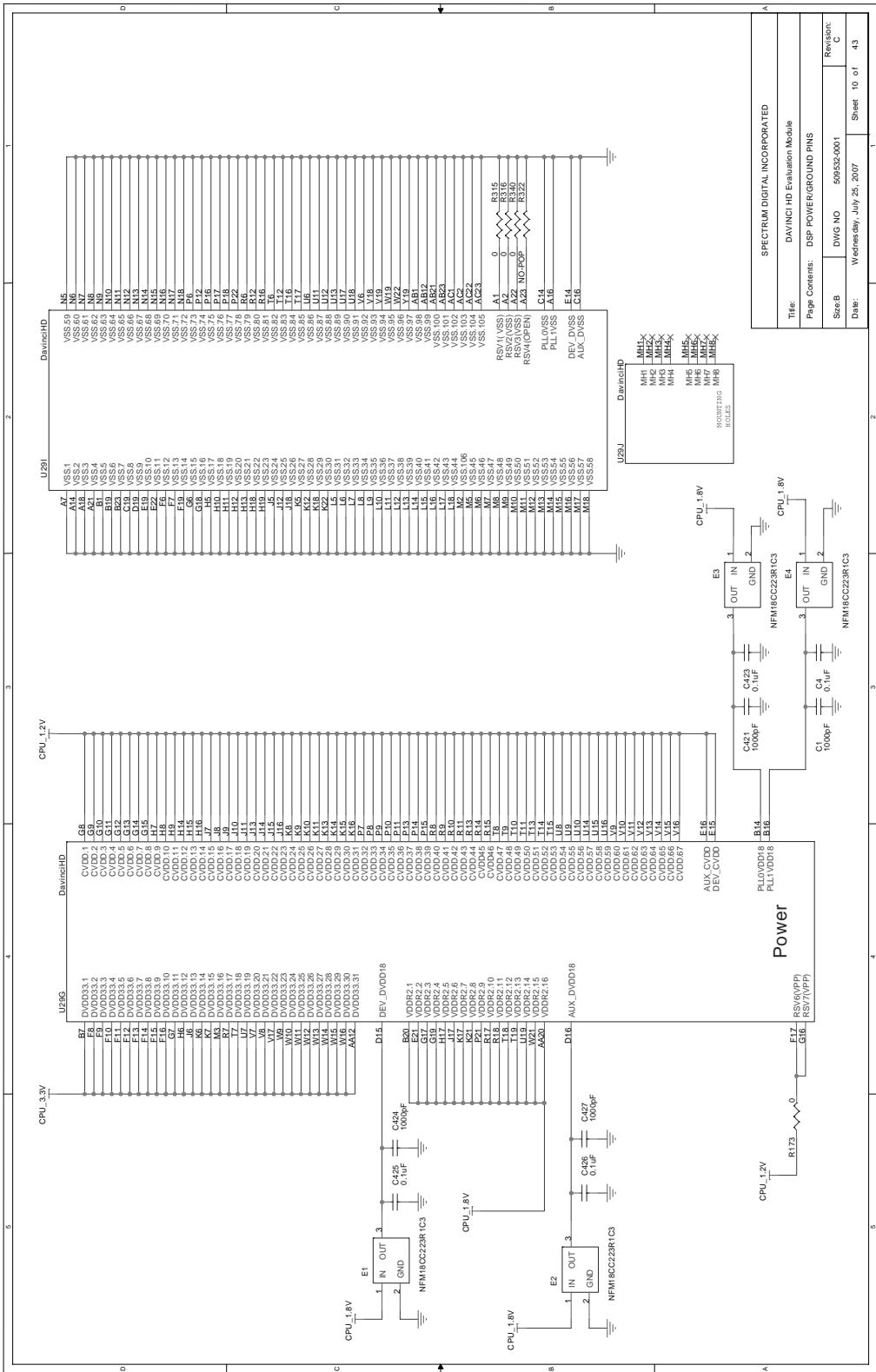
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SizeB:	DWG NO 50952-0001
Date:	Wednesday, July 25, 2007
Revision:	Rev C
Sheet 7 of 43	

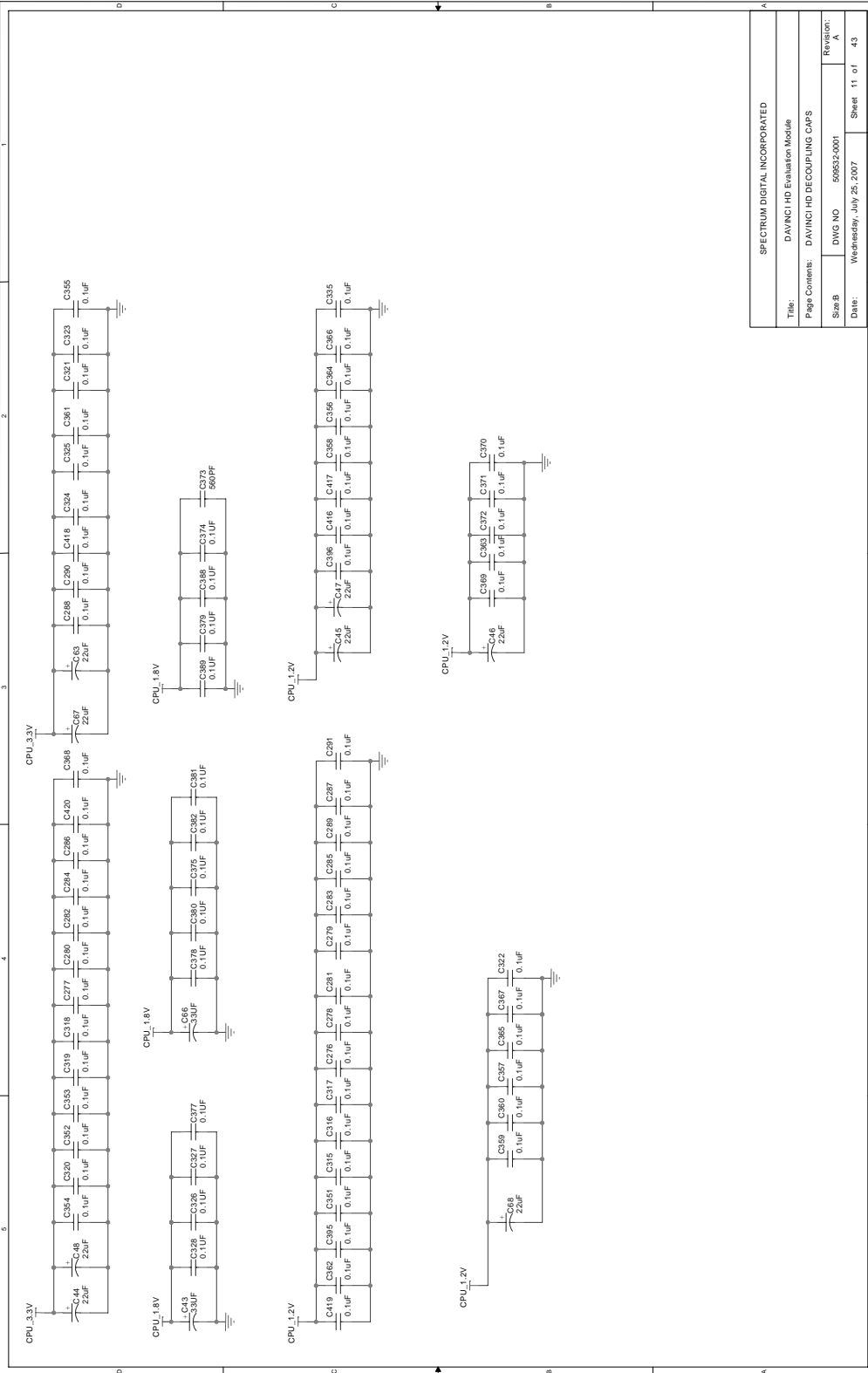


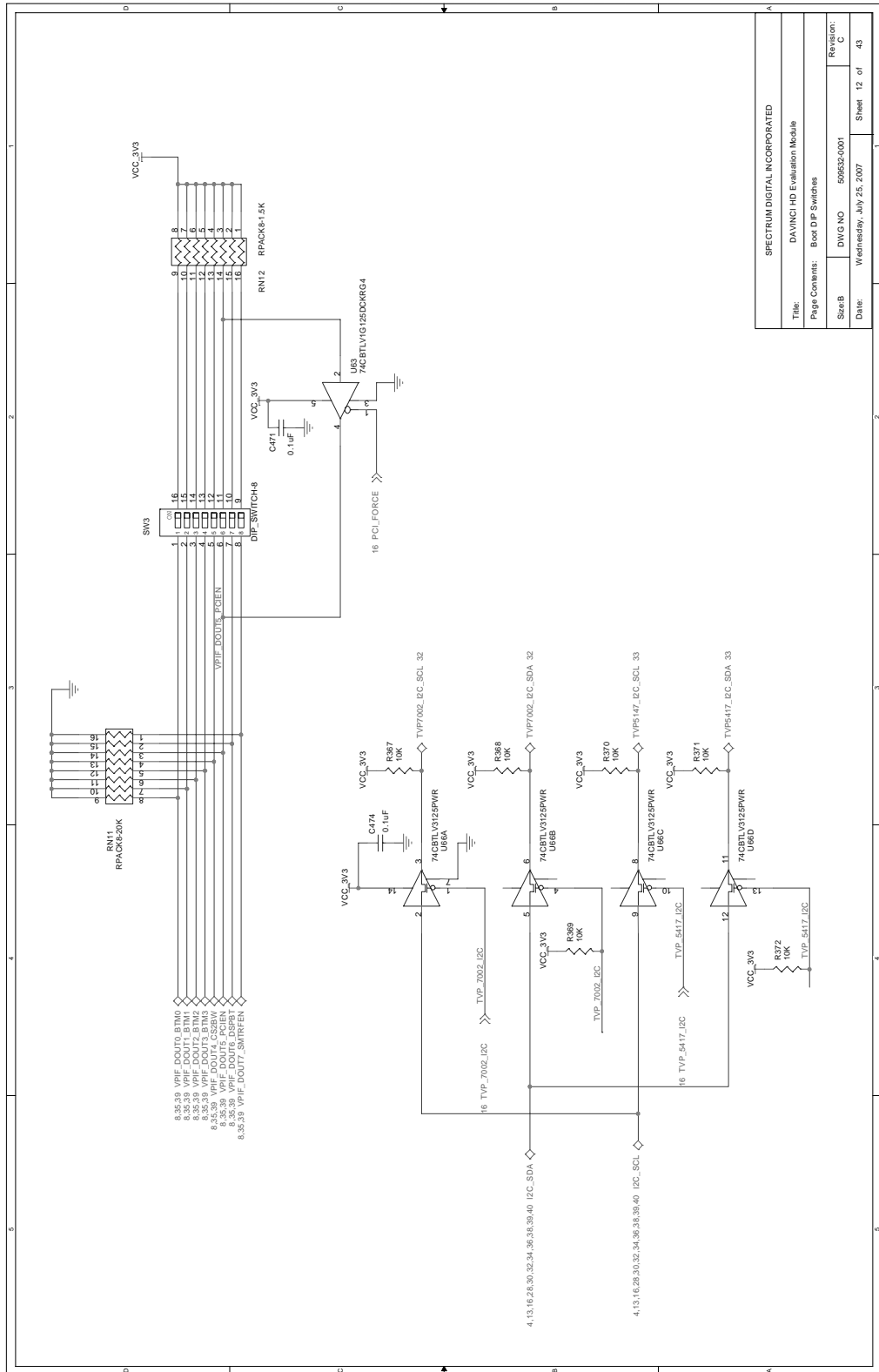


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DWG NO	59552-001
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Sheet	8 of 43

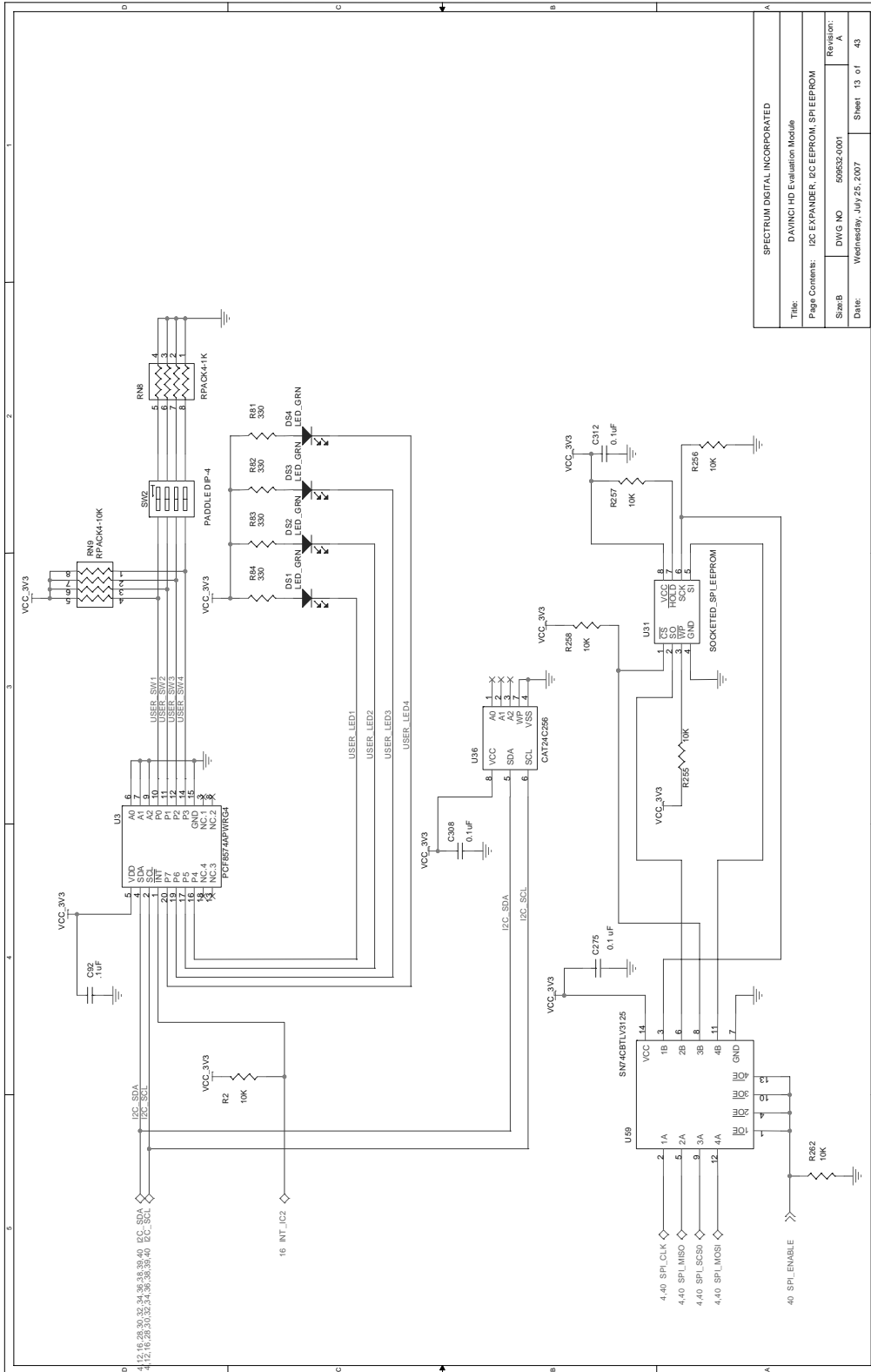




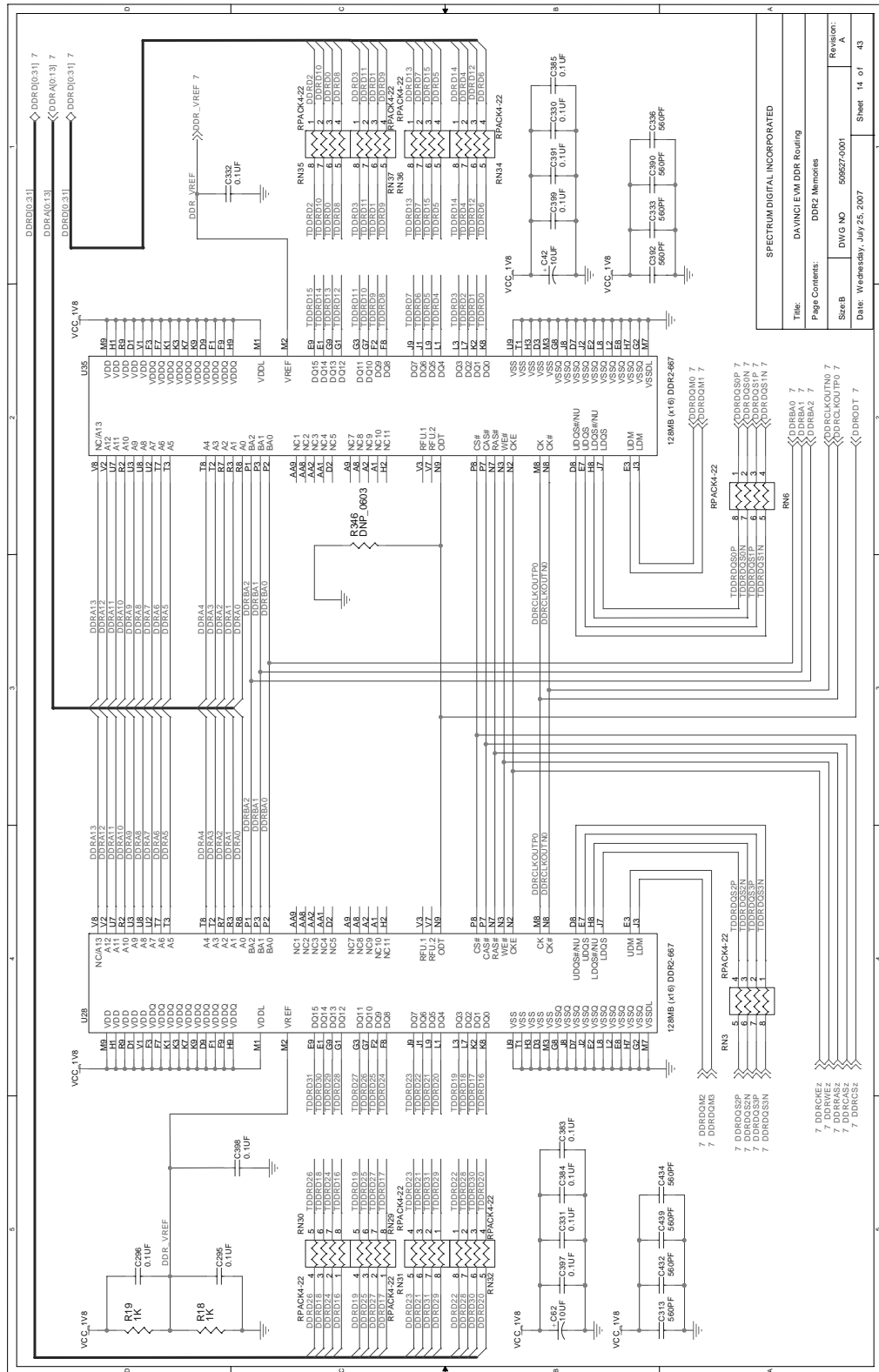




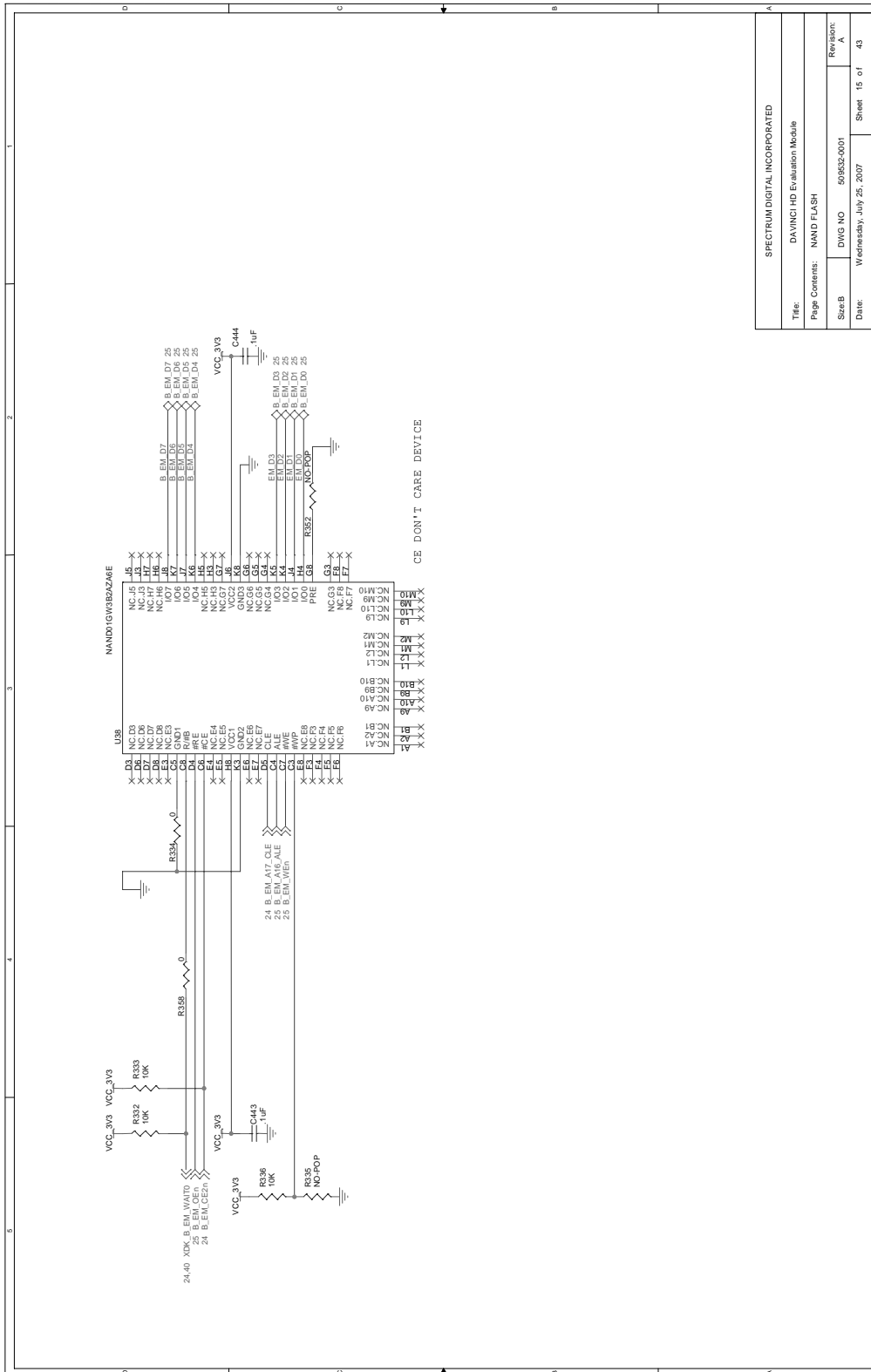
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Size B	DWG NO 59552-0001
Date: Wednesday, July 25, 2007	Revision: C
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SPECTRUM DIGITAL INCORPORATED			
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Size/B	DWG NO	509532-0001	Revision:
Date:	Wednesday, July 25, 2007	Sheet	13 of 43

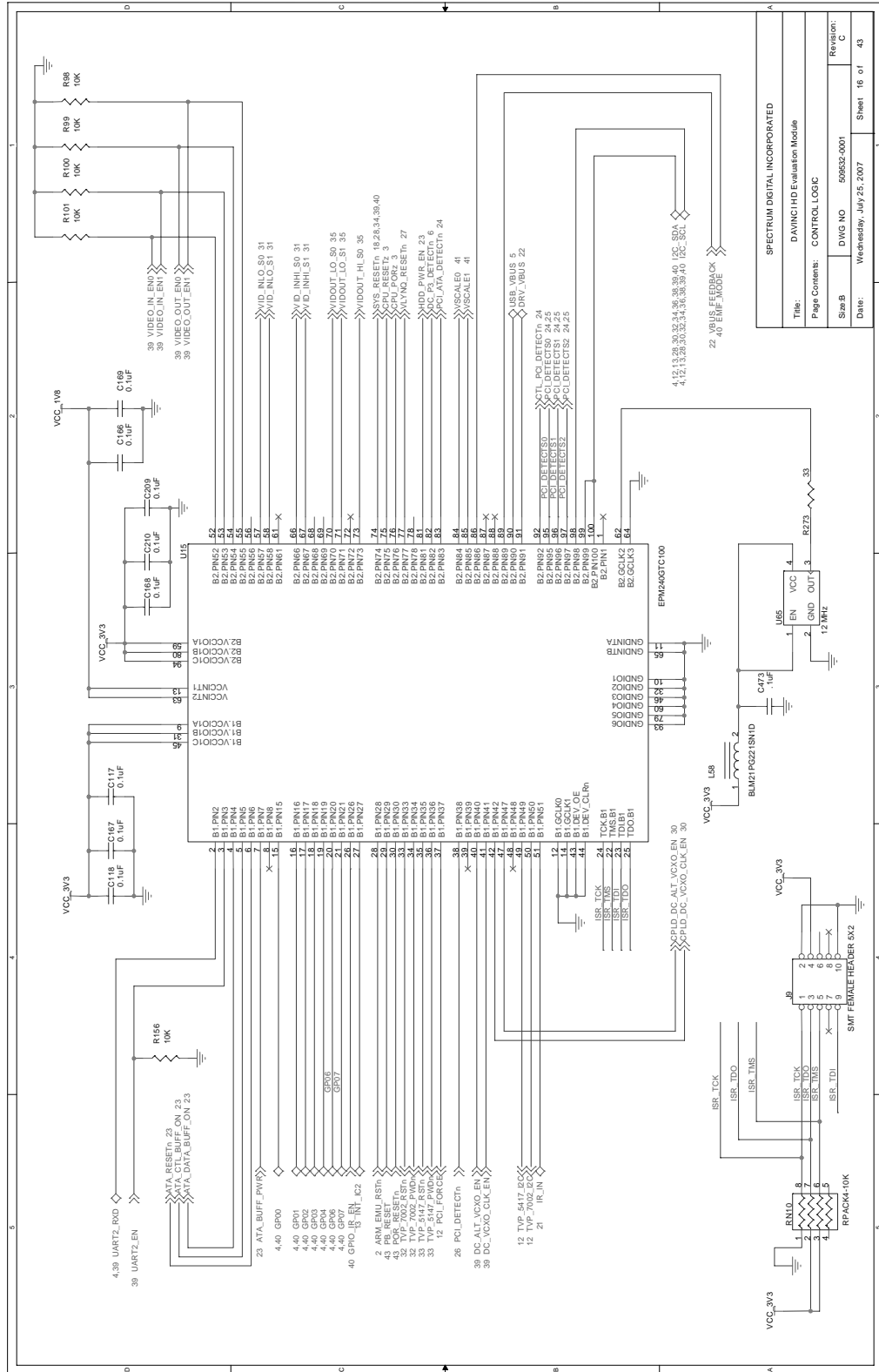


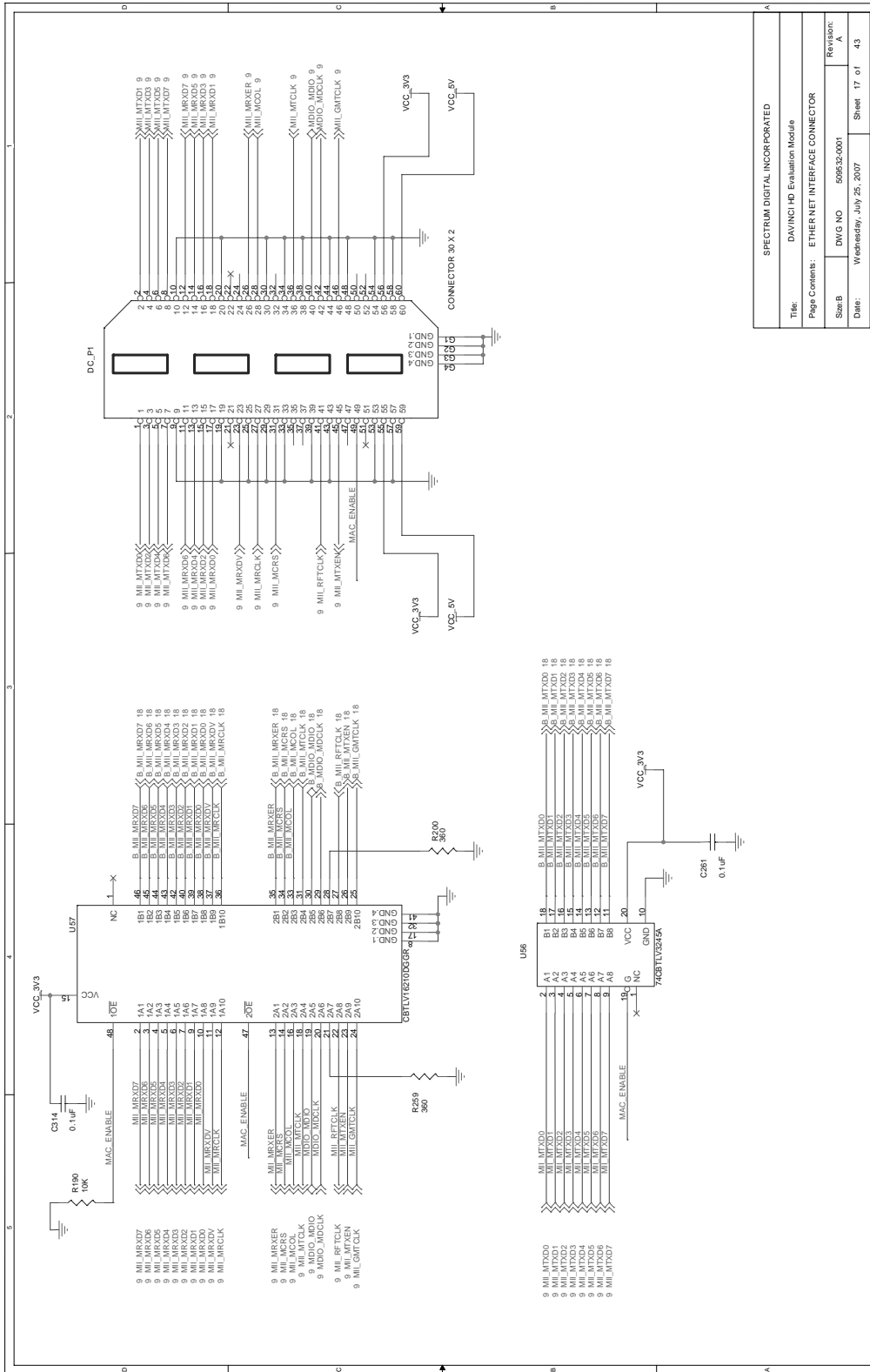
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Sheet:	14 of 43



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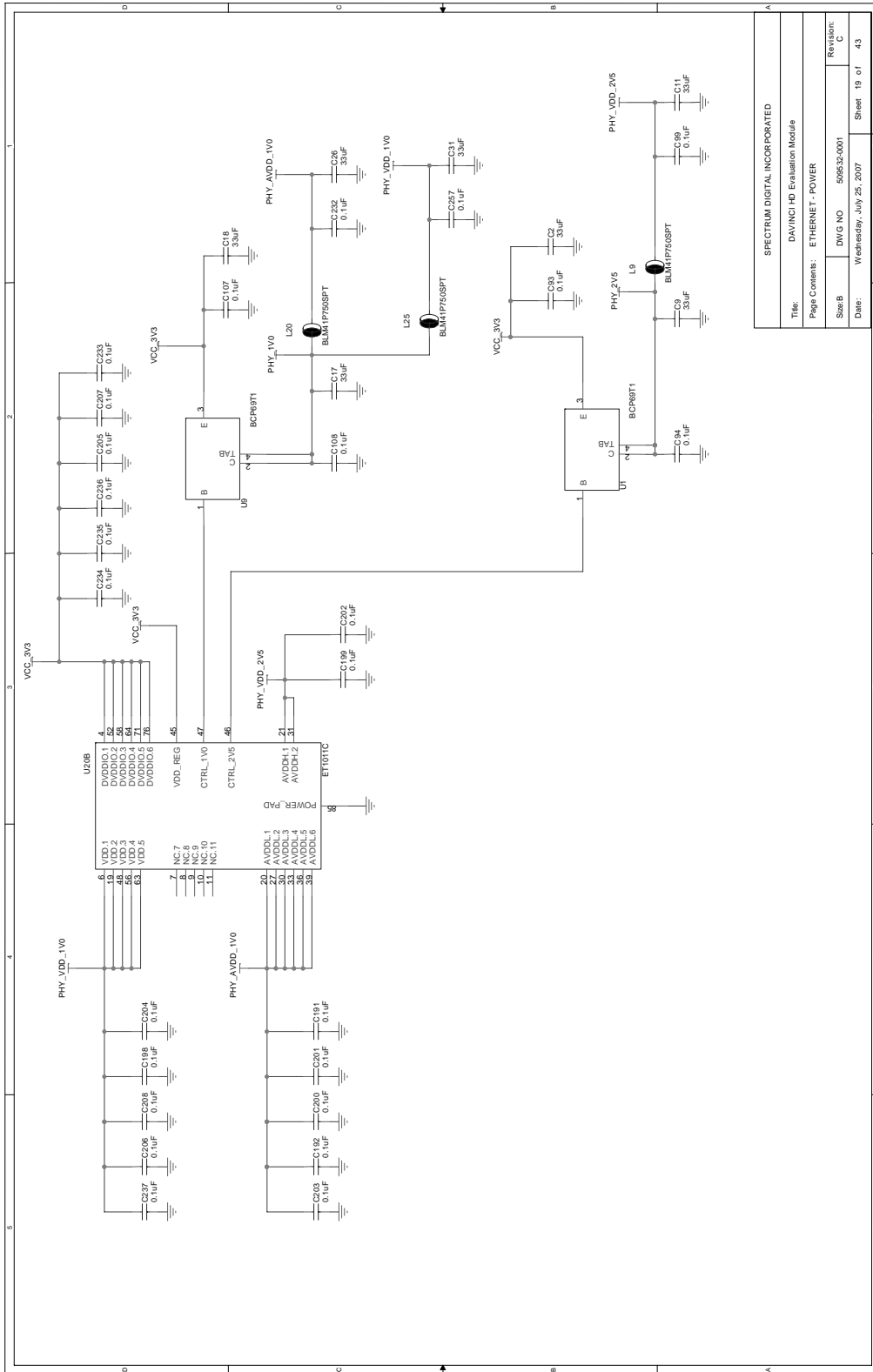




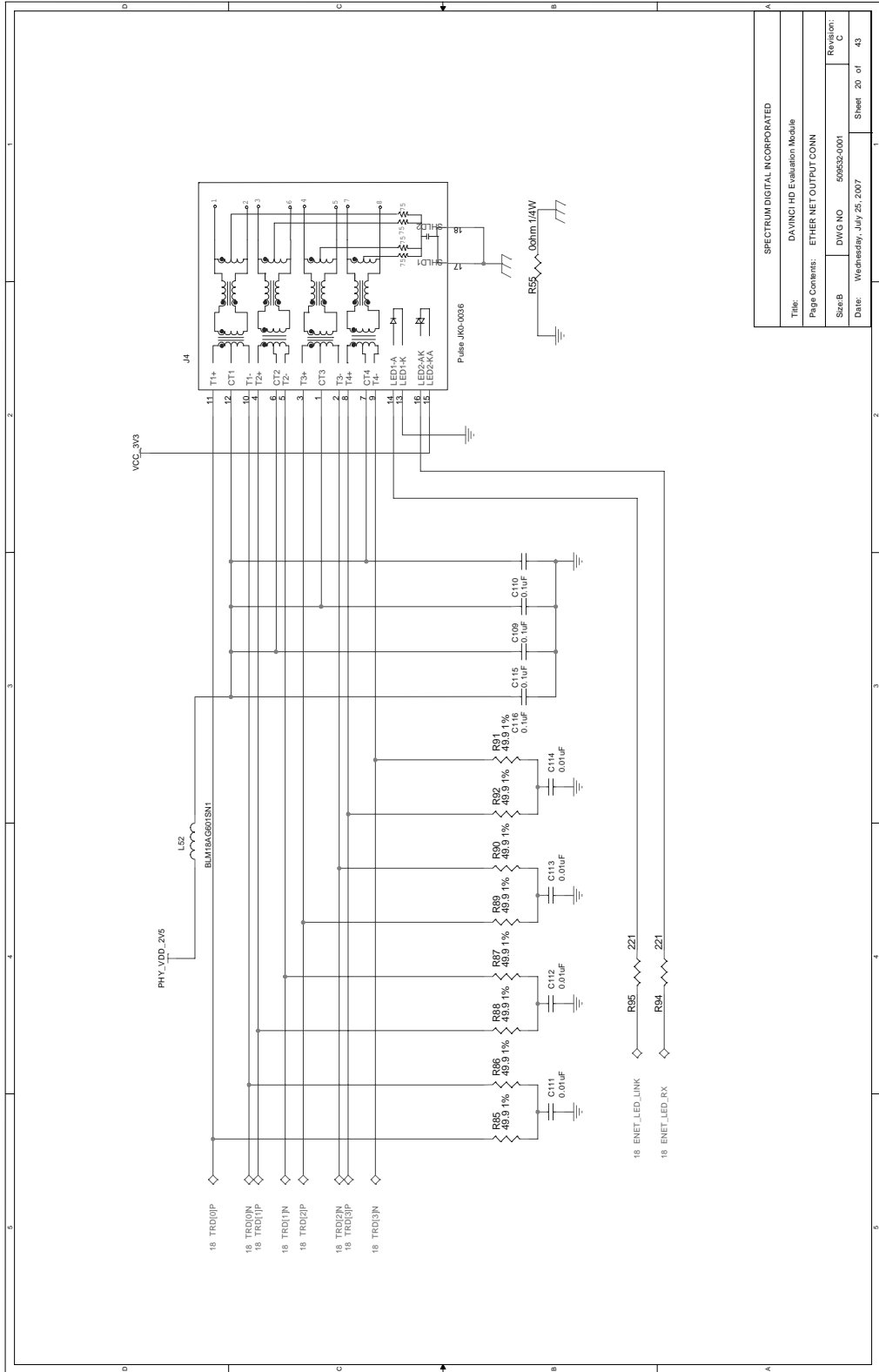


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Sheet 17 of 43	

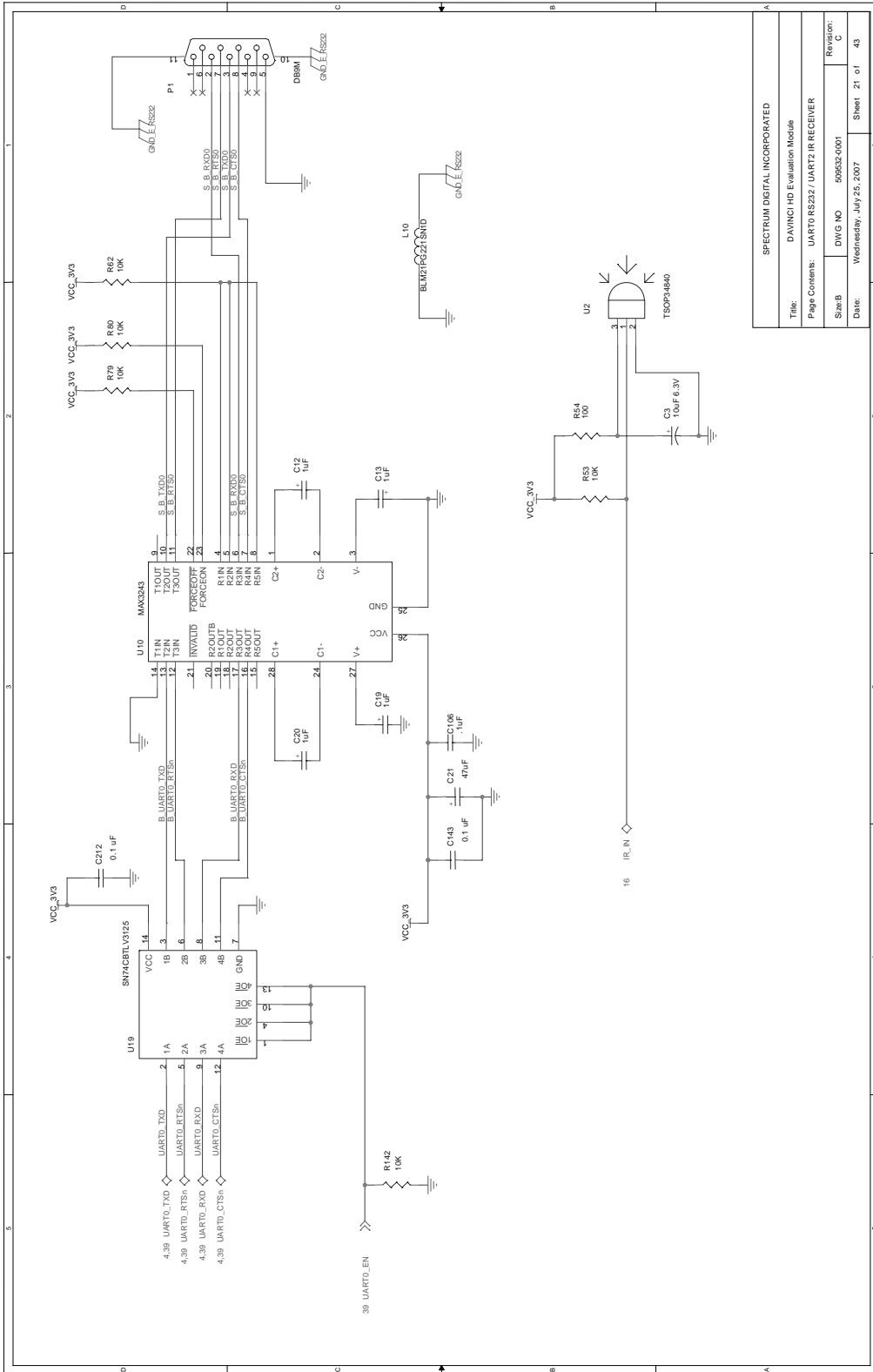




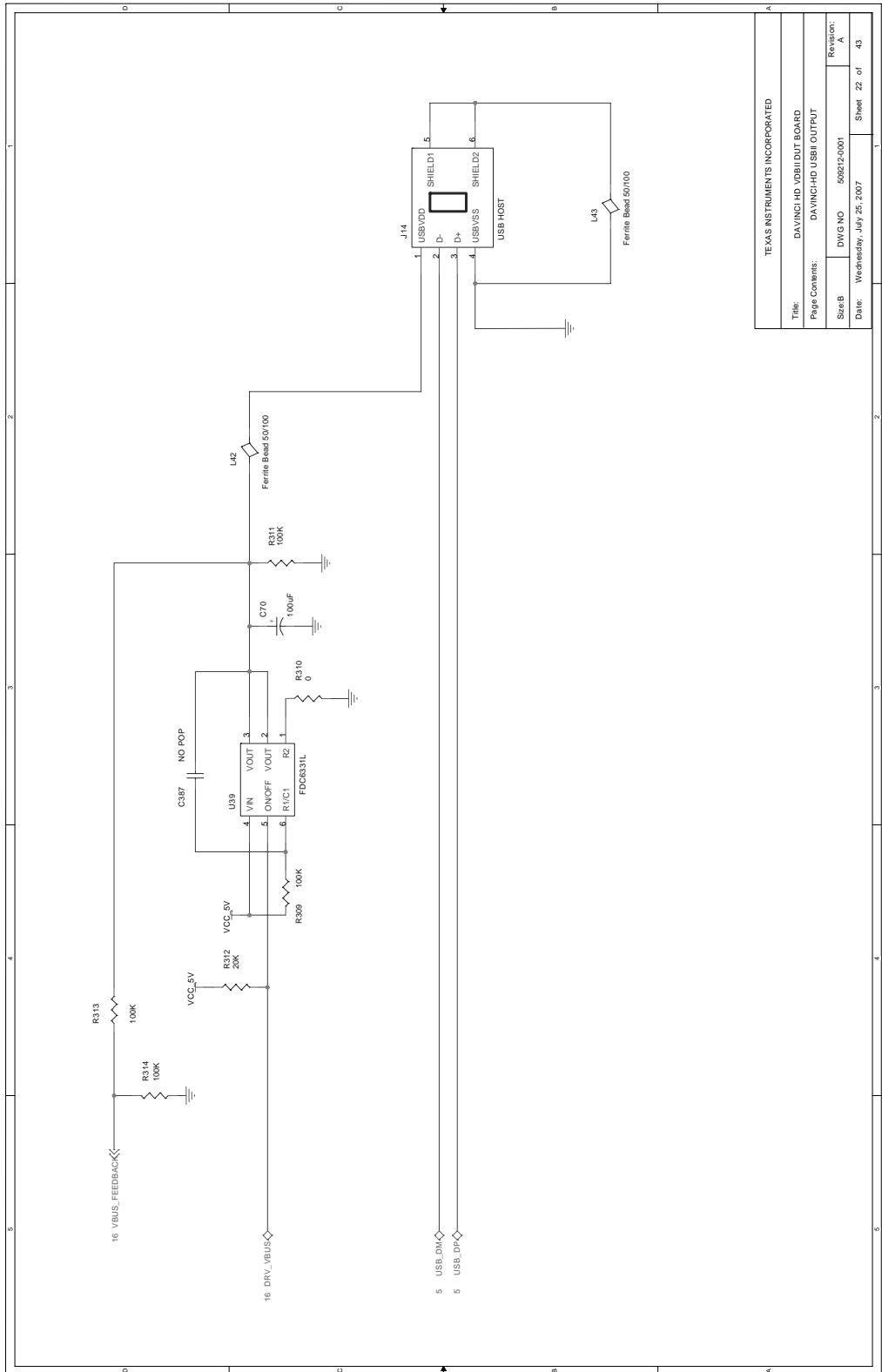
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Sheet 19 of 43	



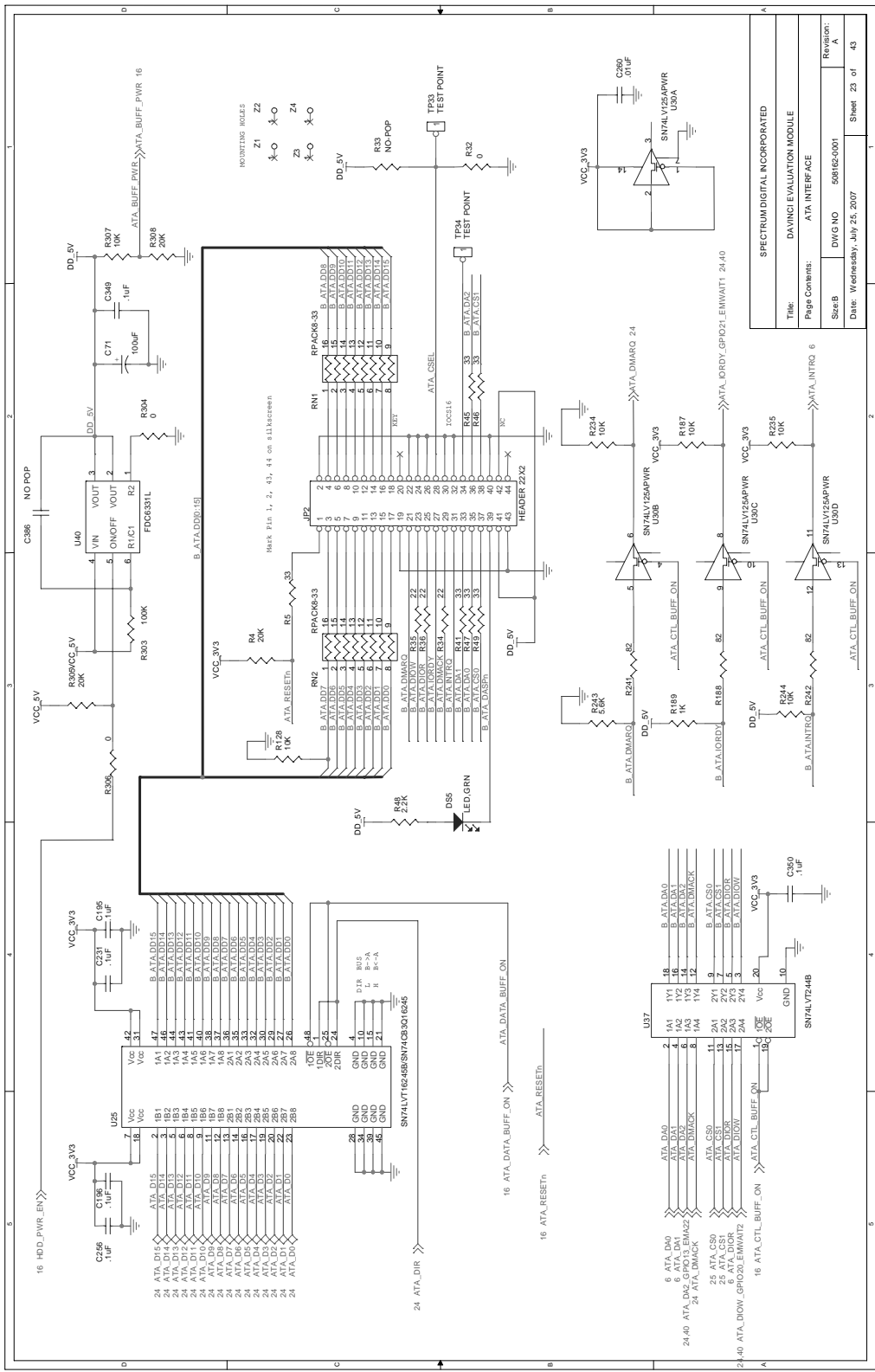
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Revision:	C
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Rev:	C
Date:	Wednesday, July 25, 2007

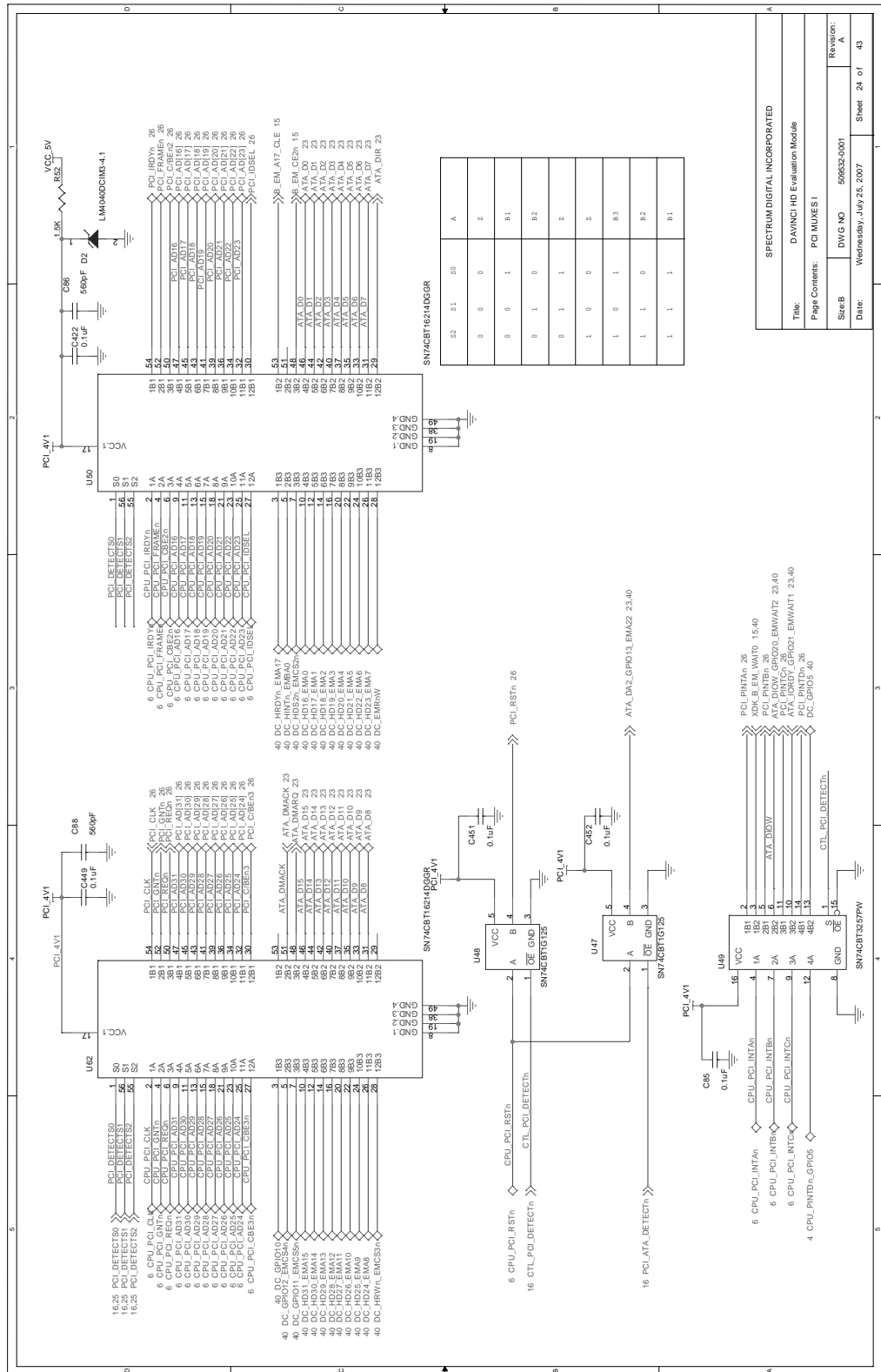


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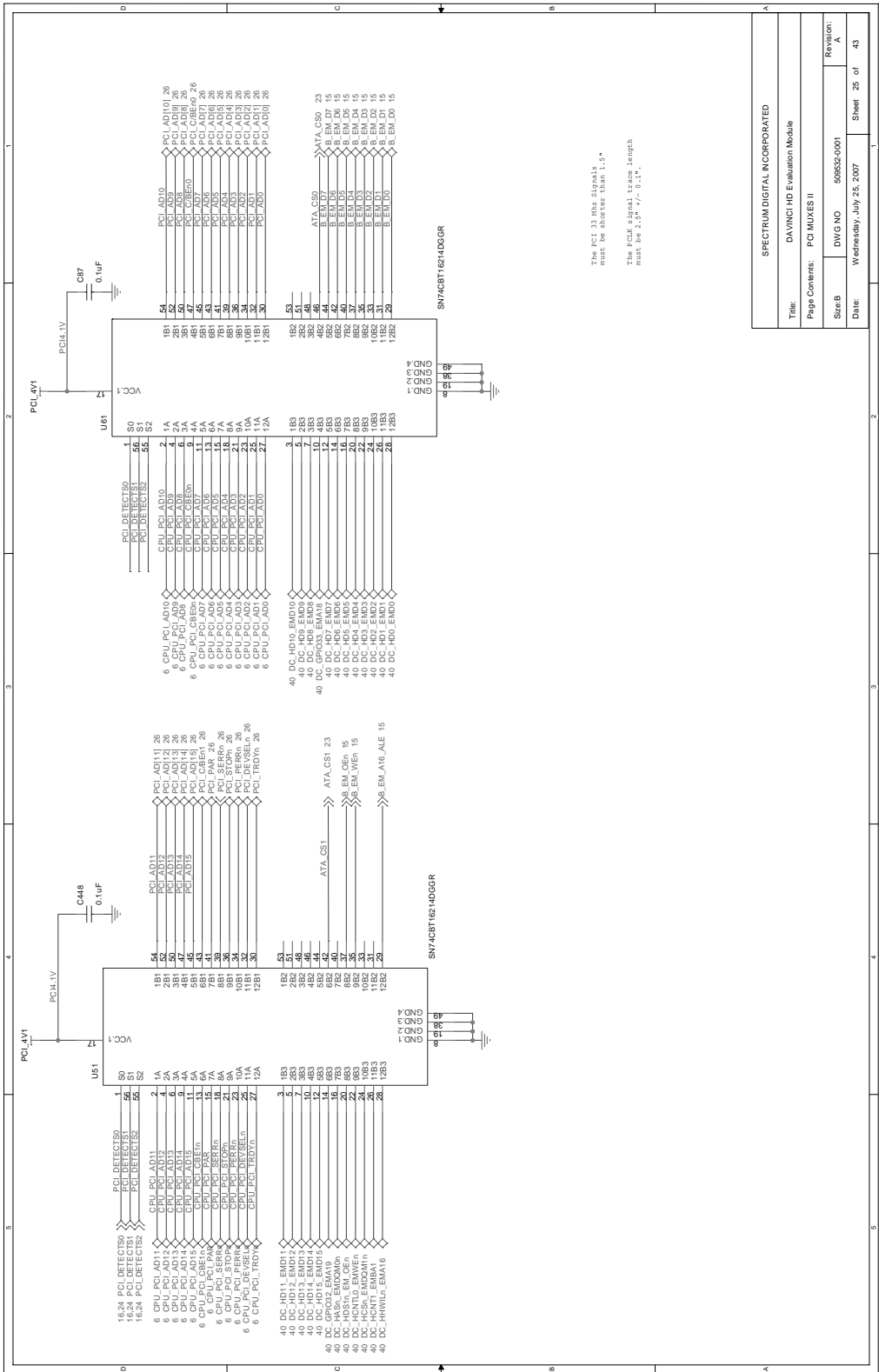


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Sheet 23 of 43	



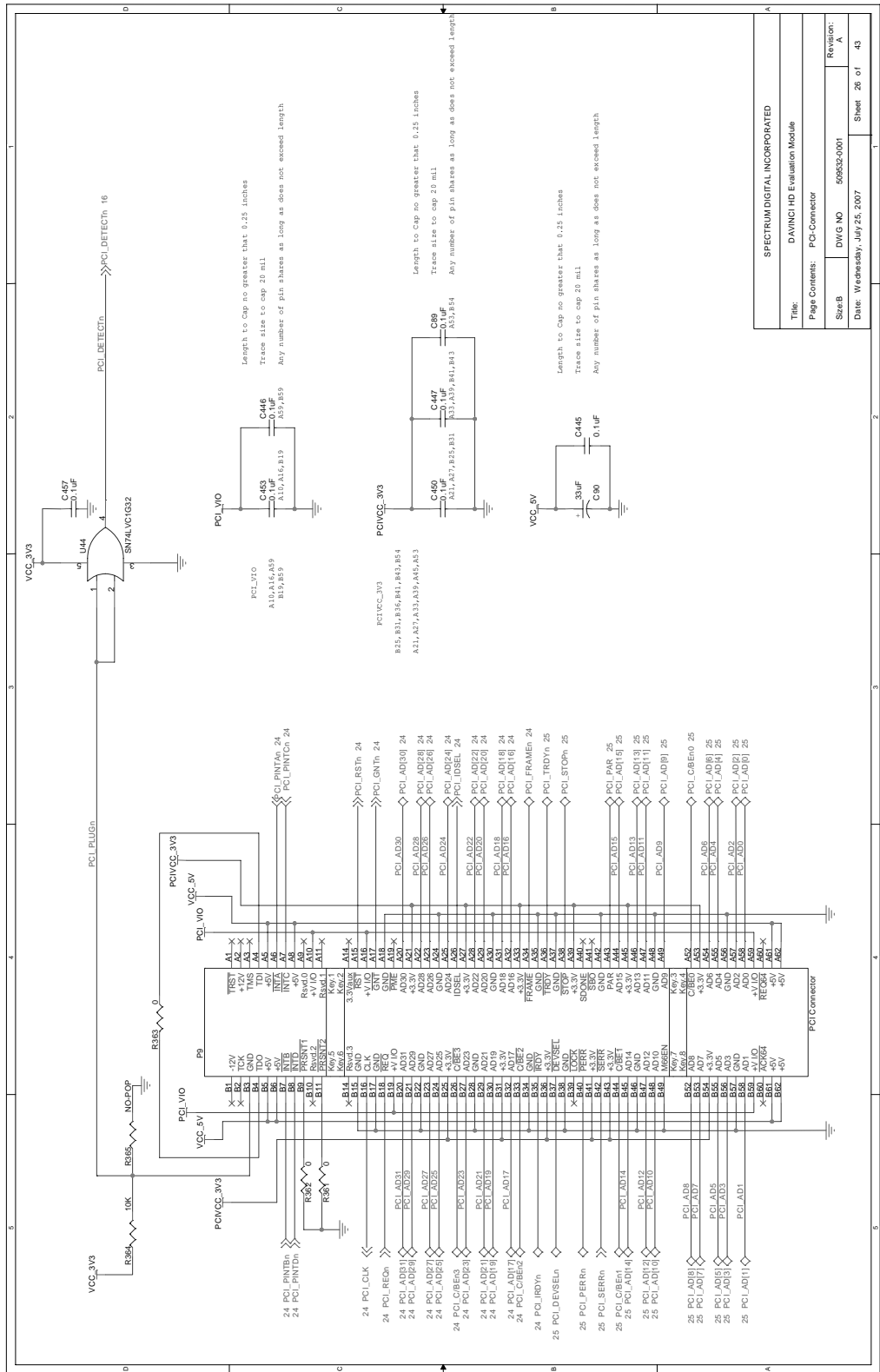


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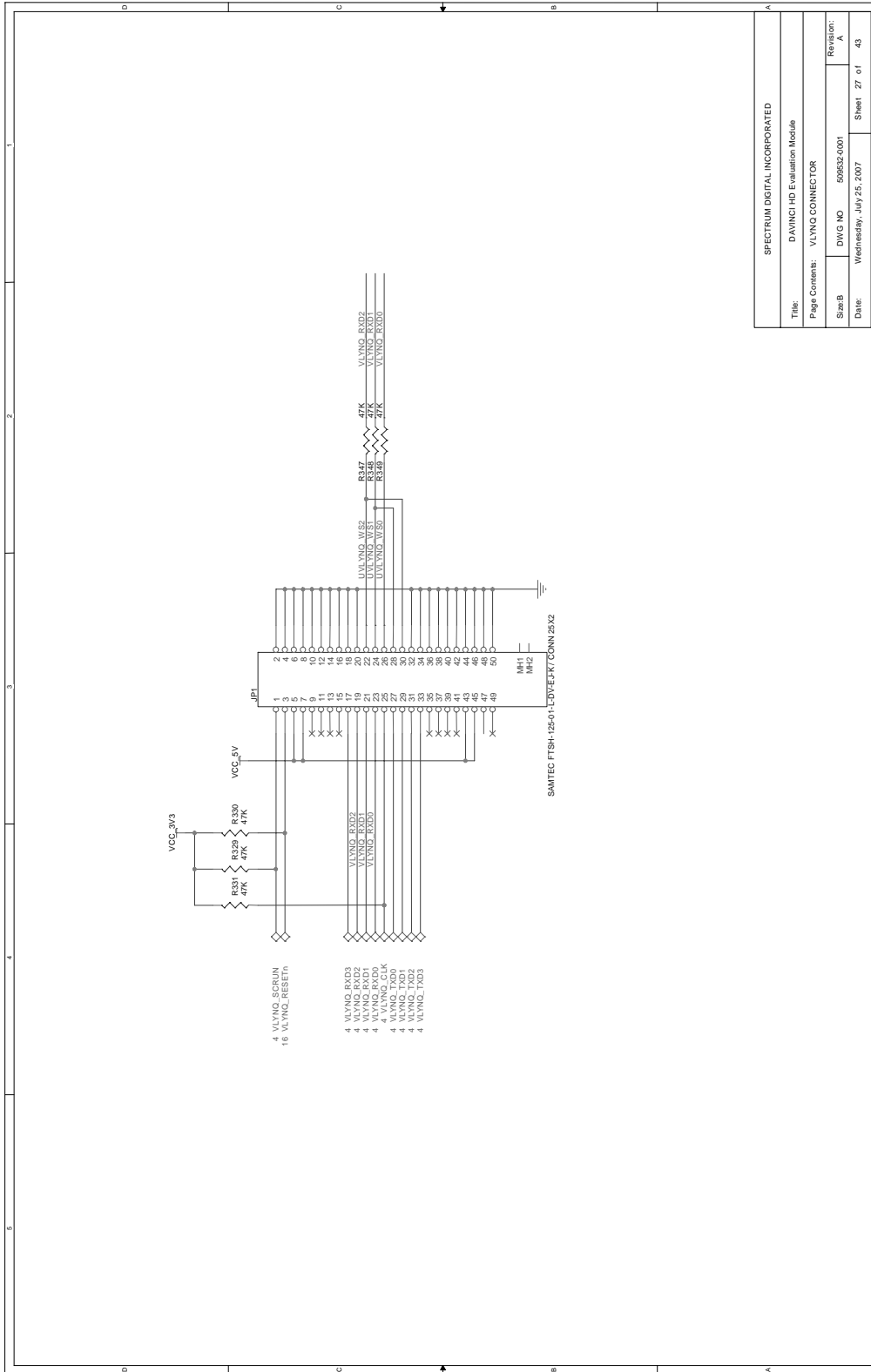


The PCI 33 Mhz signals must be shorter than 1.3".  
The PCB signal trace length must be 2.2" +/- 0.1".

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Date:	Wednesday, July 25, 2007
Revision:	A
Sheet	25 of 43

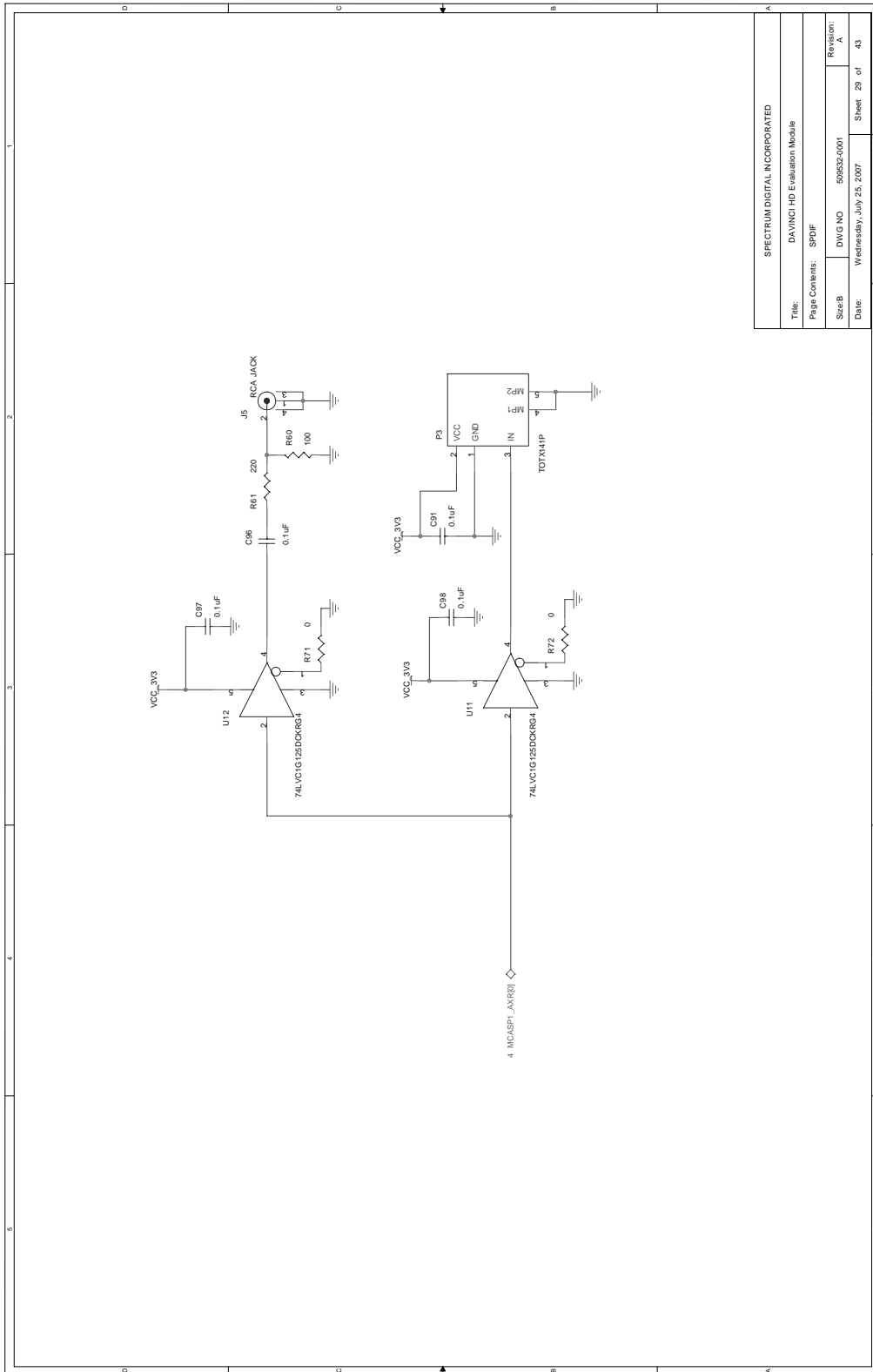


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Sheet	26 of 43

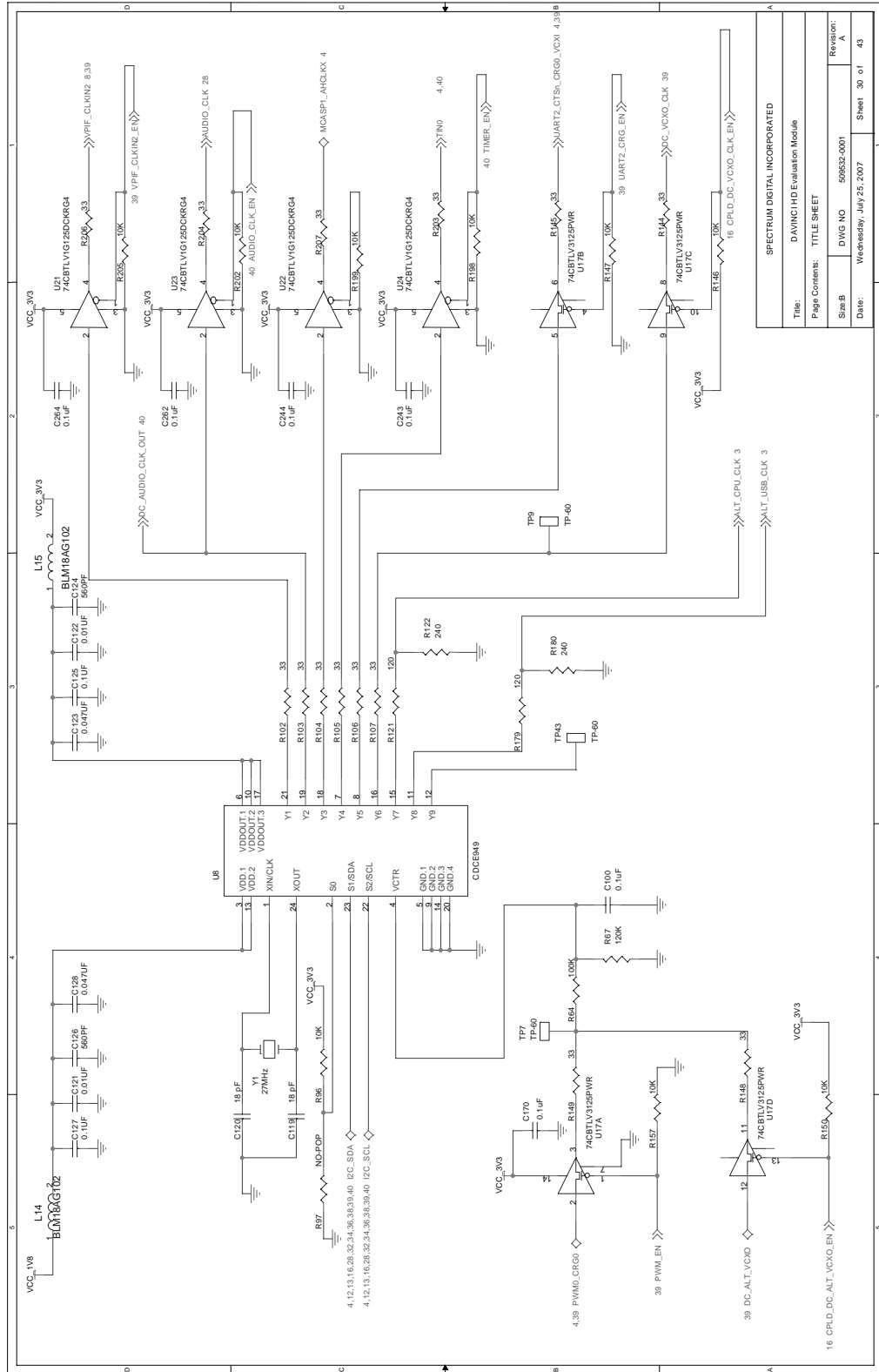


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Date: Wednesday, July 25, 2007	Revision: A
Sheet: 27 of 43	

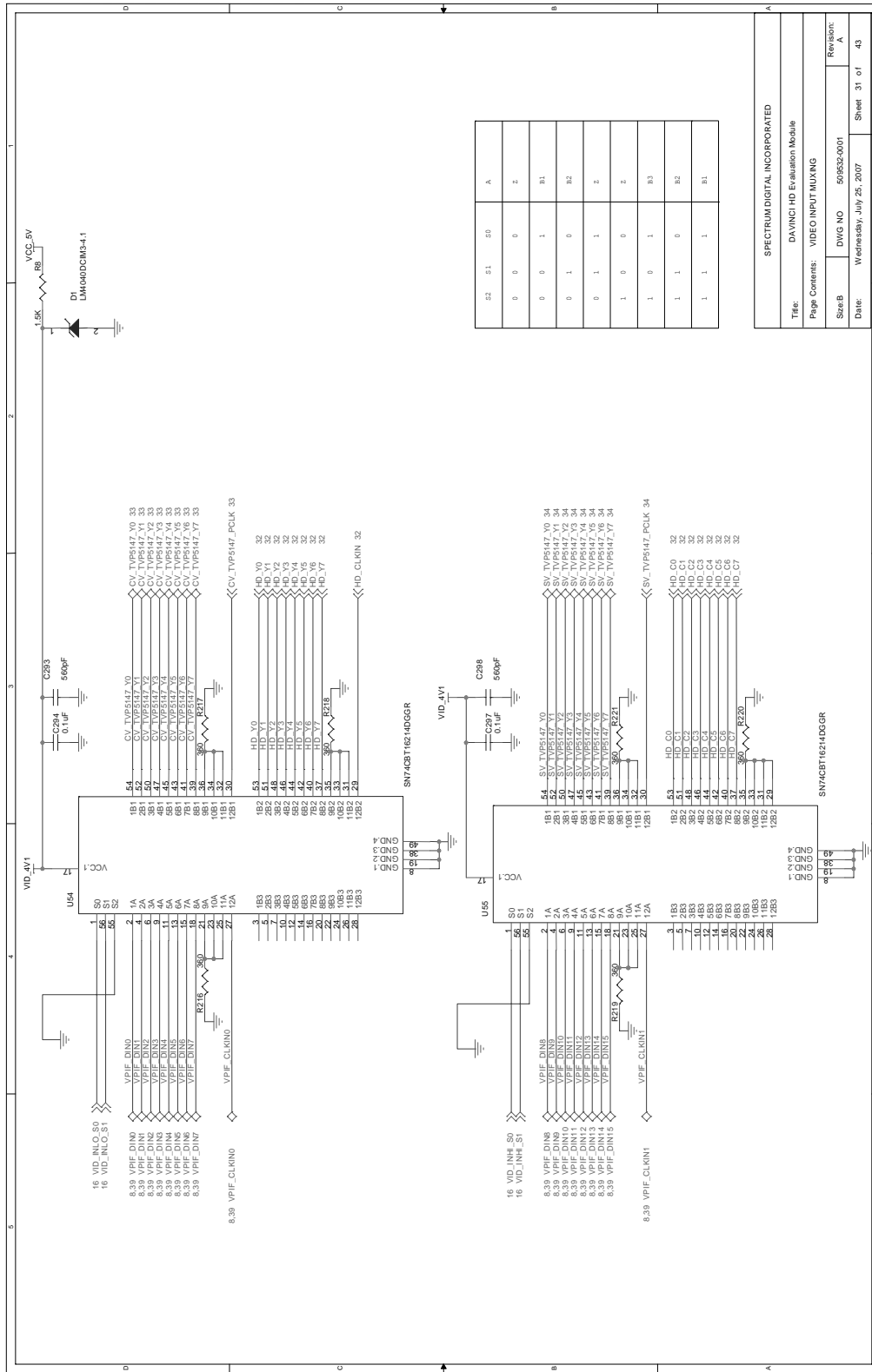




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Revision:	A
Sheet	29 of 43



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Page Contents:		DAVINCI HD Evaluation Module	
StarB	DWG NO	59552-001	Revision:
Date:	Wednesday, July 25, 2007		A
		Sheet	30 of 43



Page Contents:	Page No
DAVINCI HD Evaluation Module	509552-001
VIDEO INPUT MIXING	A

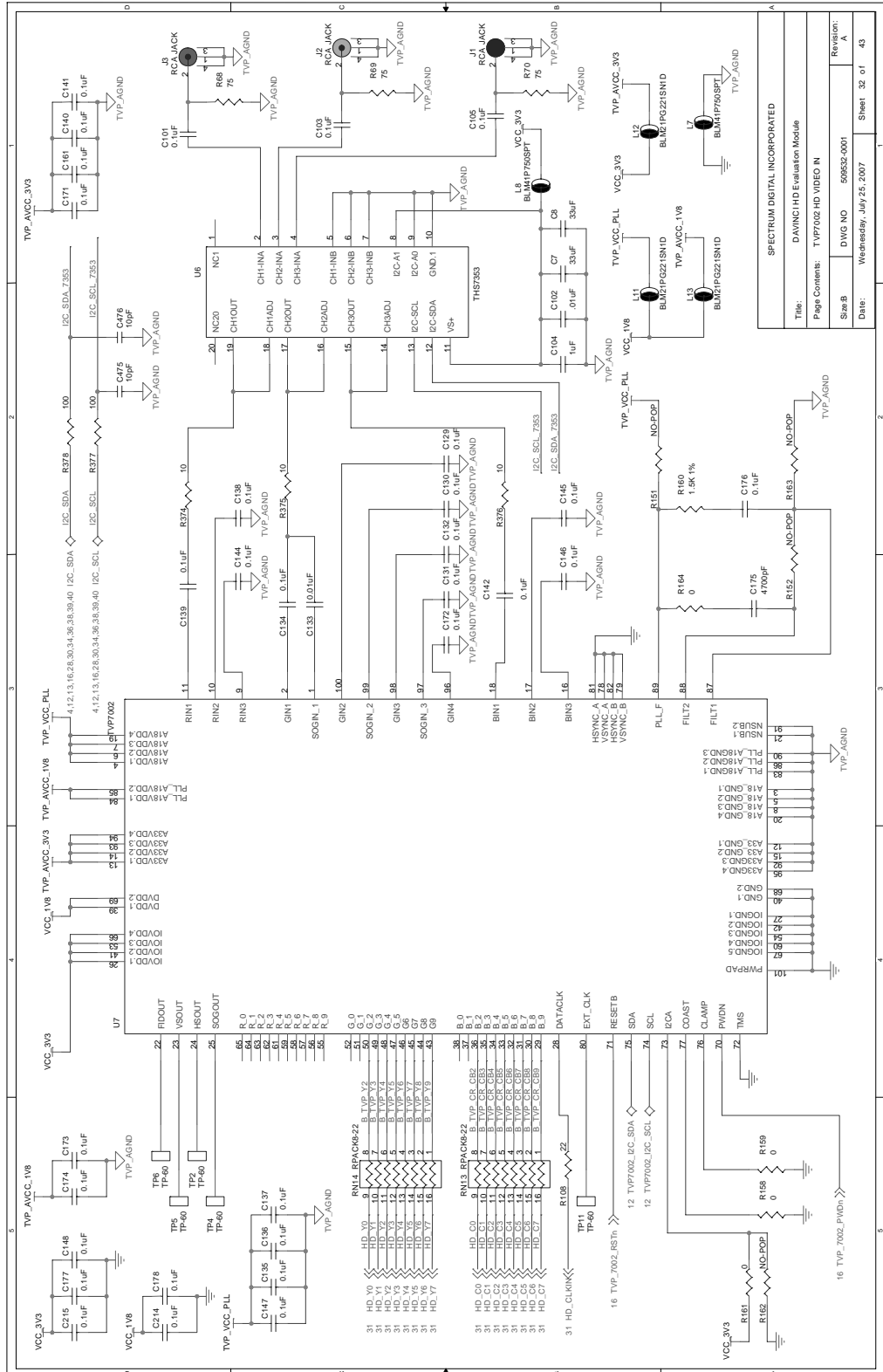
  

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31	43

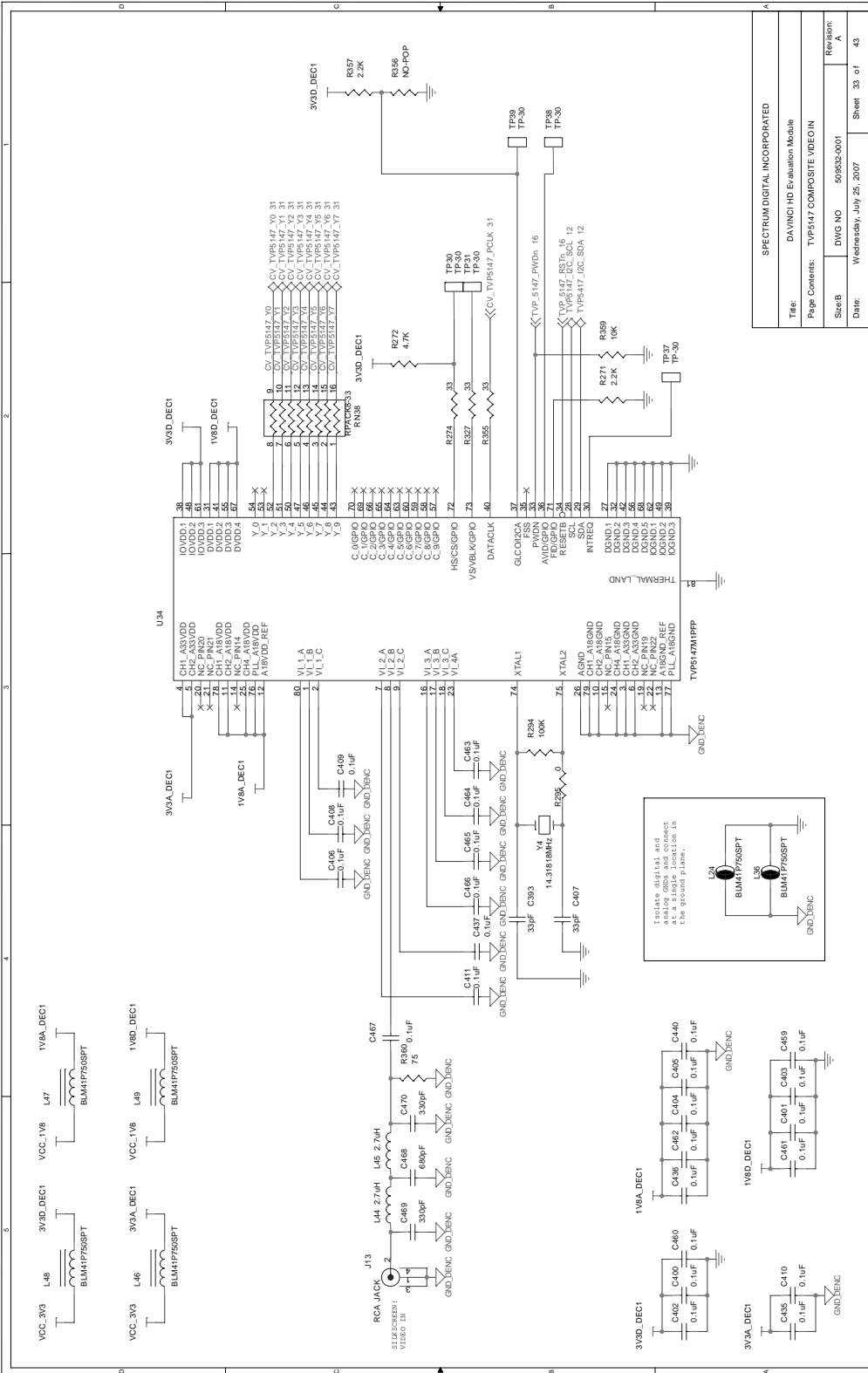
  

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Wednesday, July 25, 2007	A



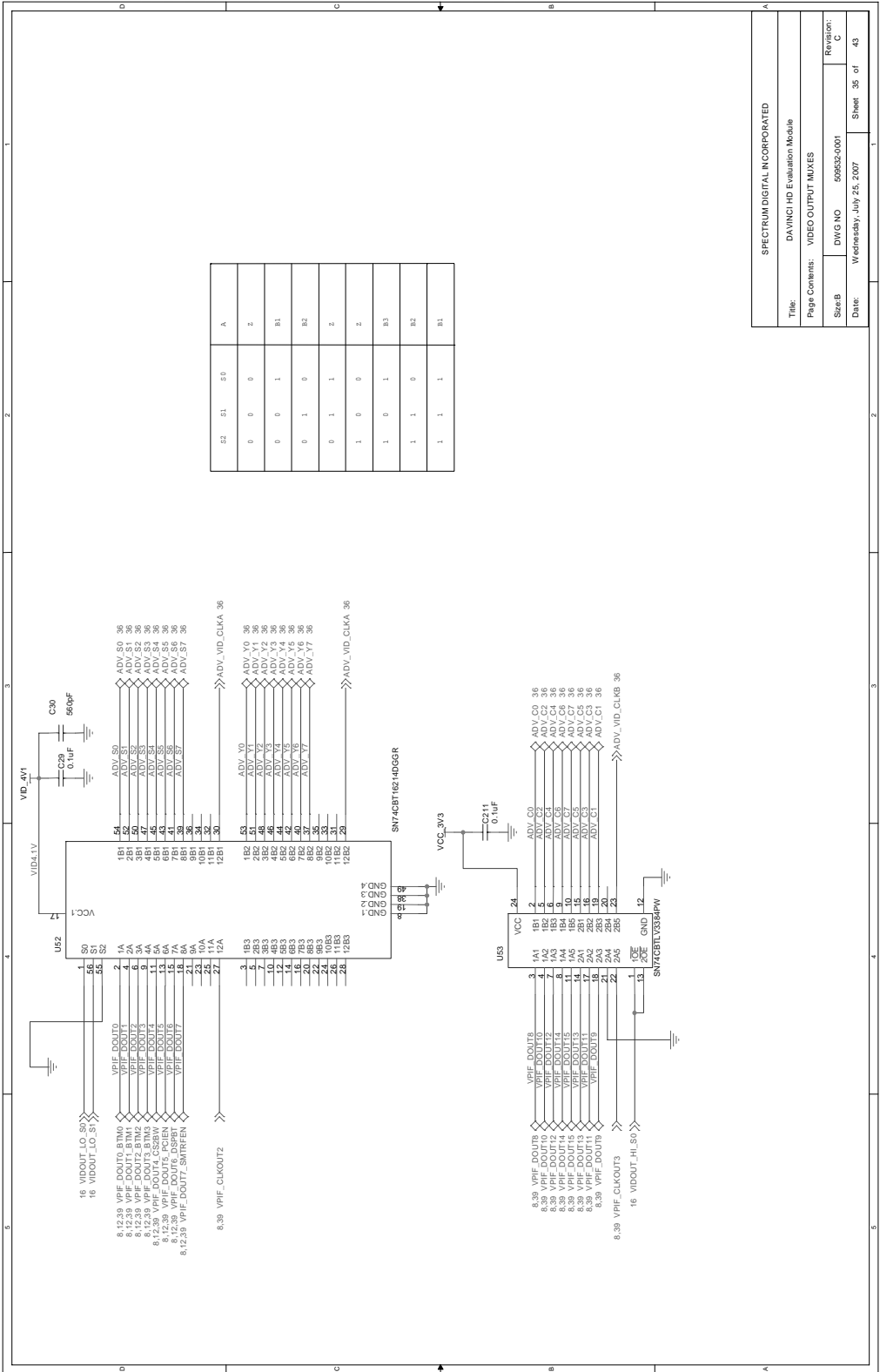


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Revision:	A
Sheet	32 of 43



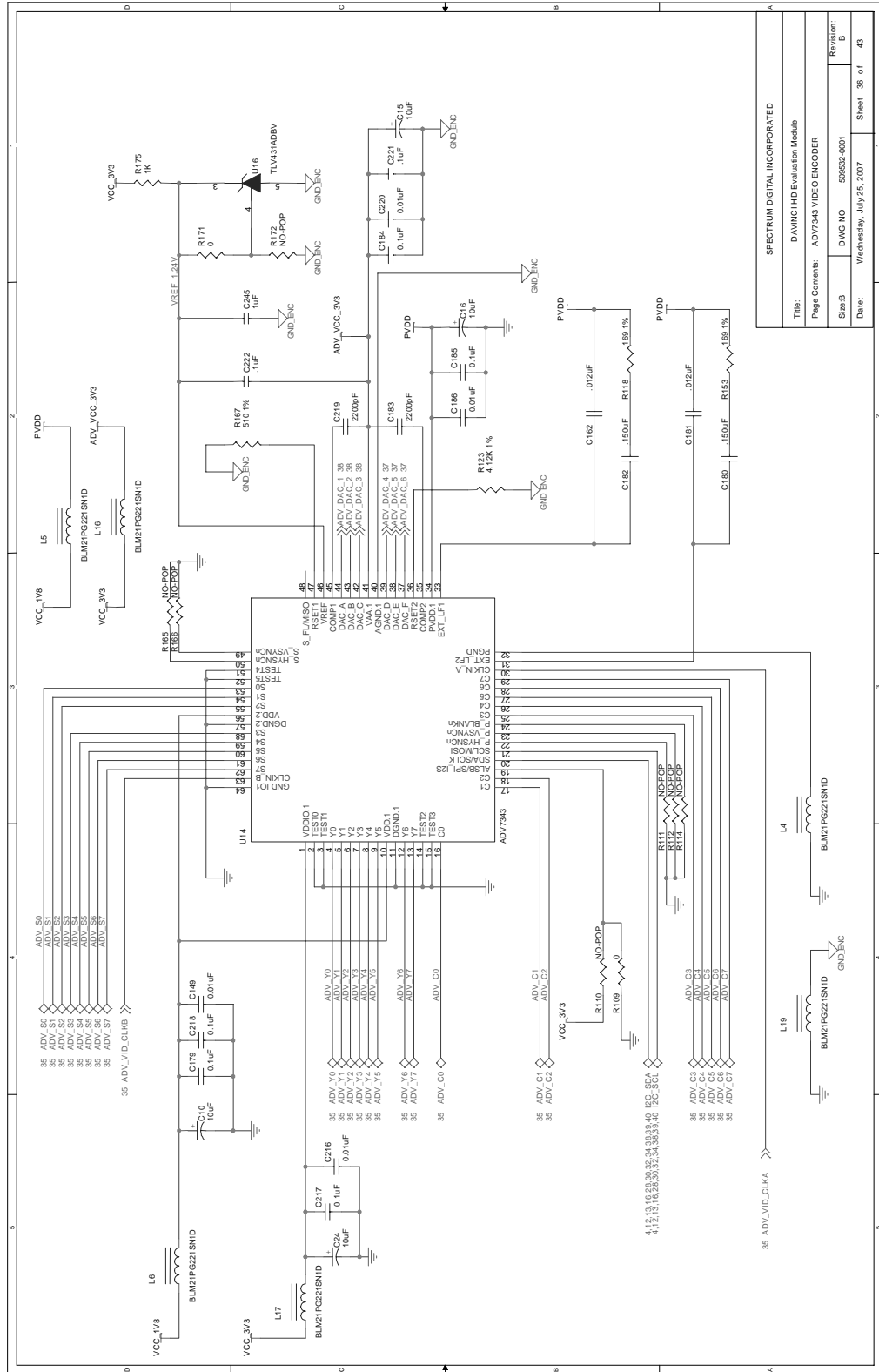
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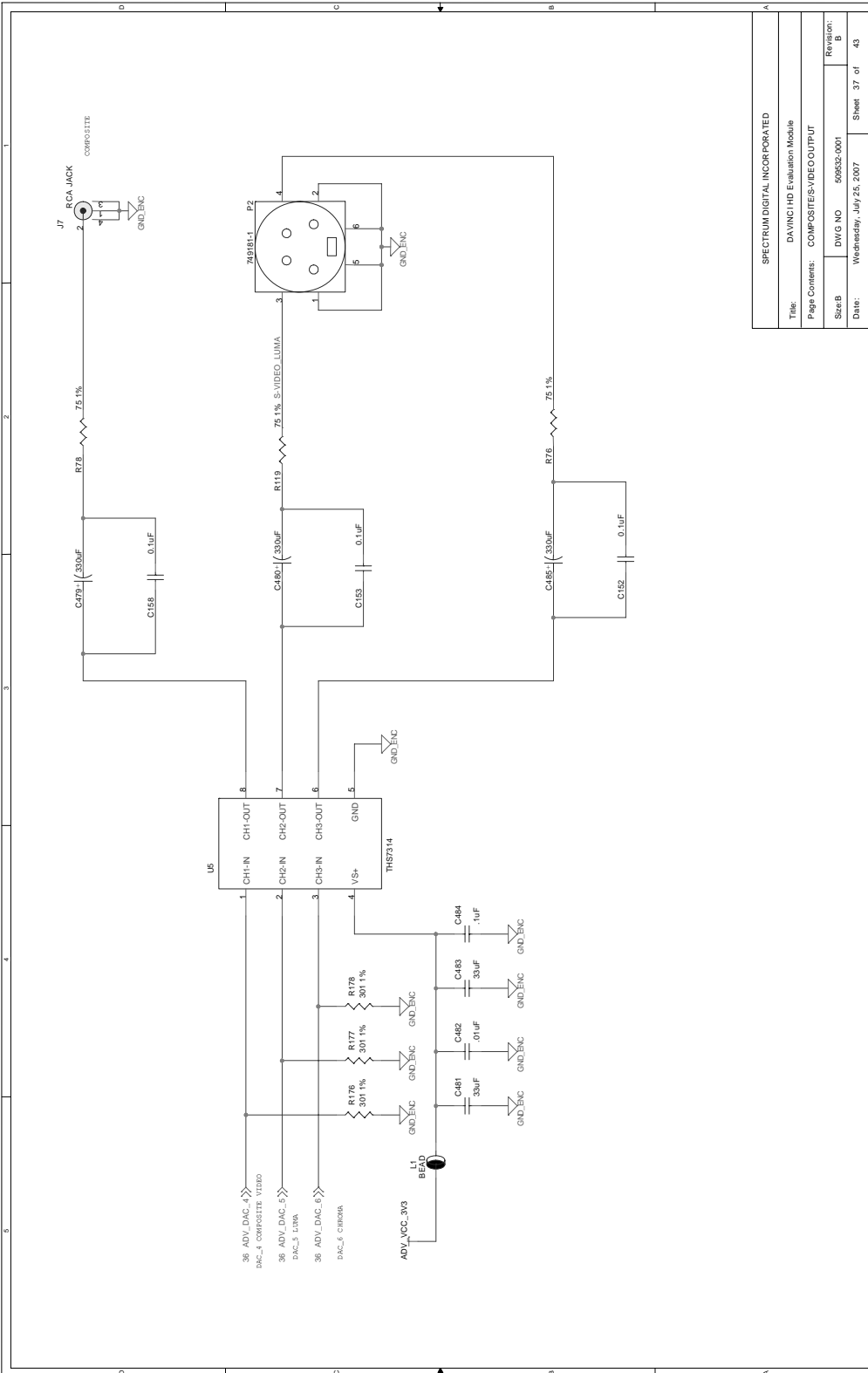




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0	1	0	B2
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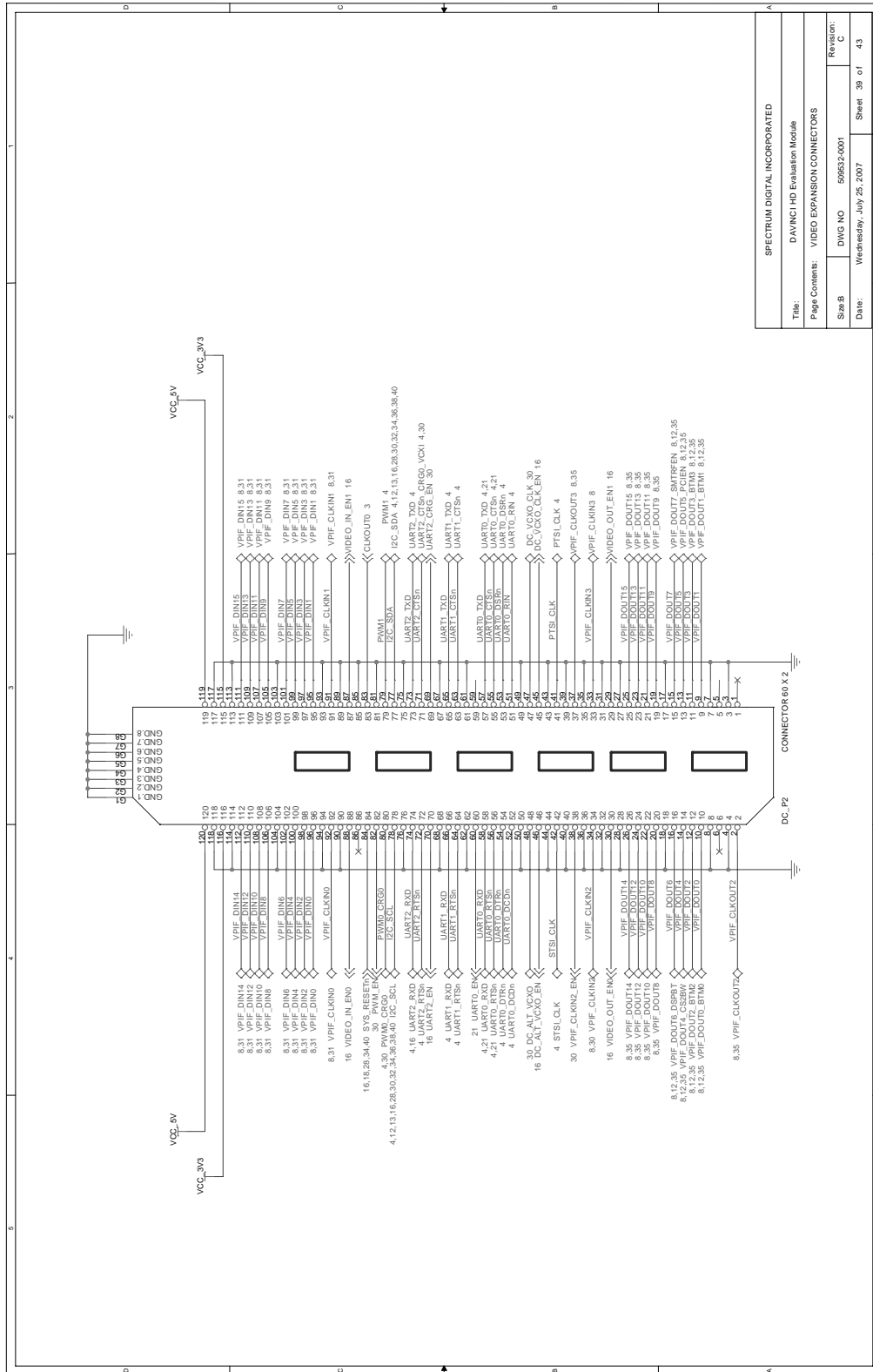
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Date:	Wednesday, July 25, 2007		Sheet 35 of 43





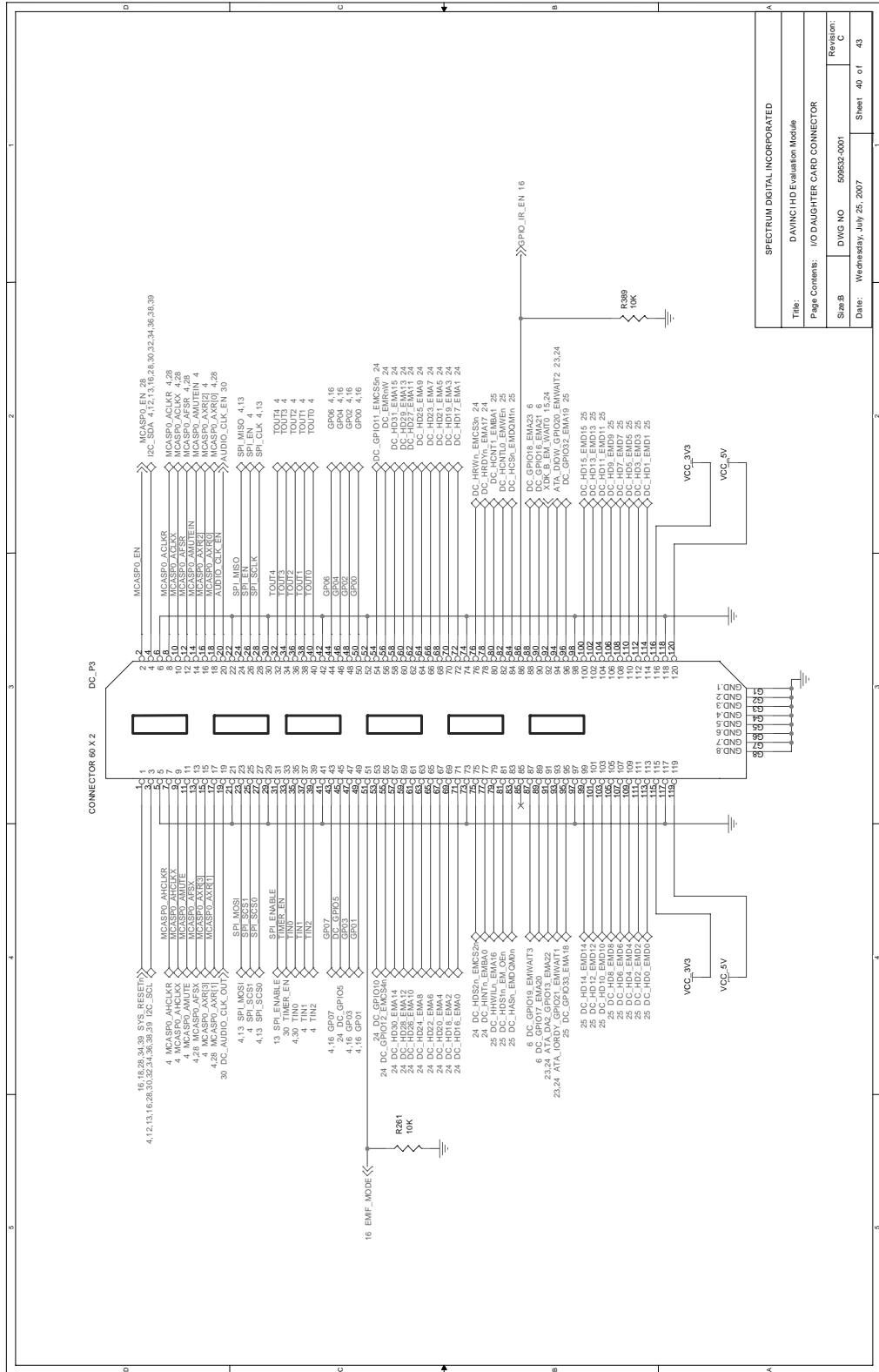
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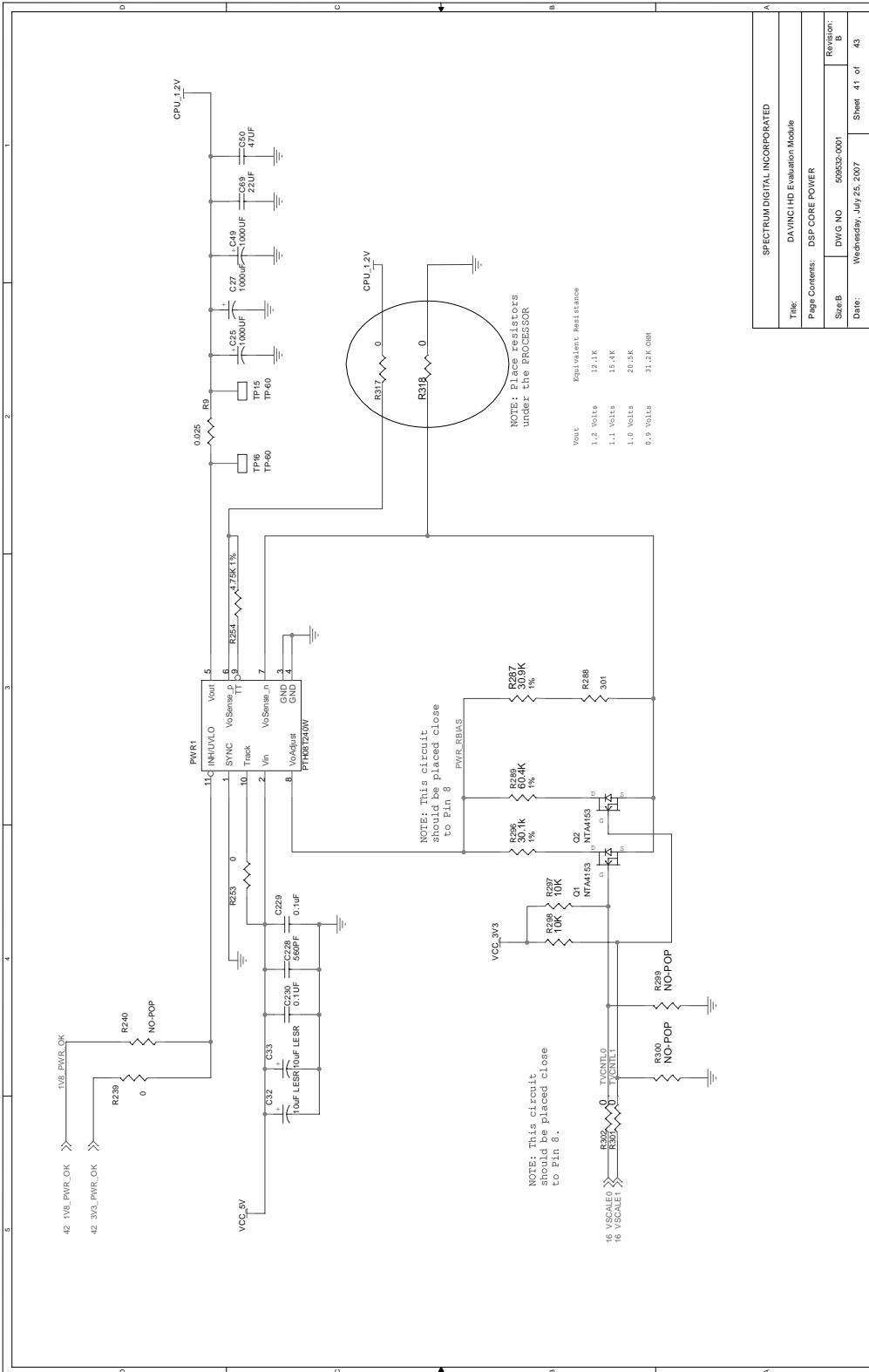


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Revision: C	



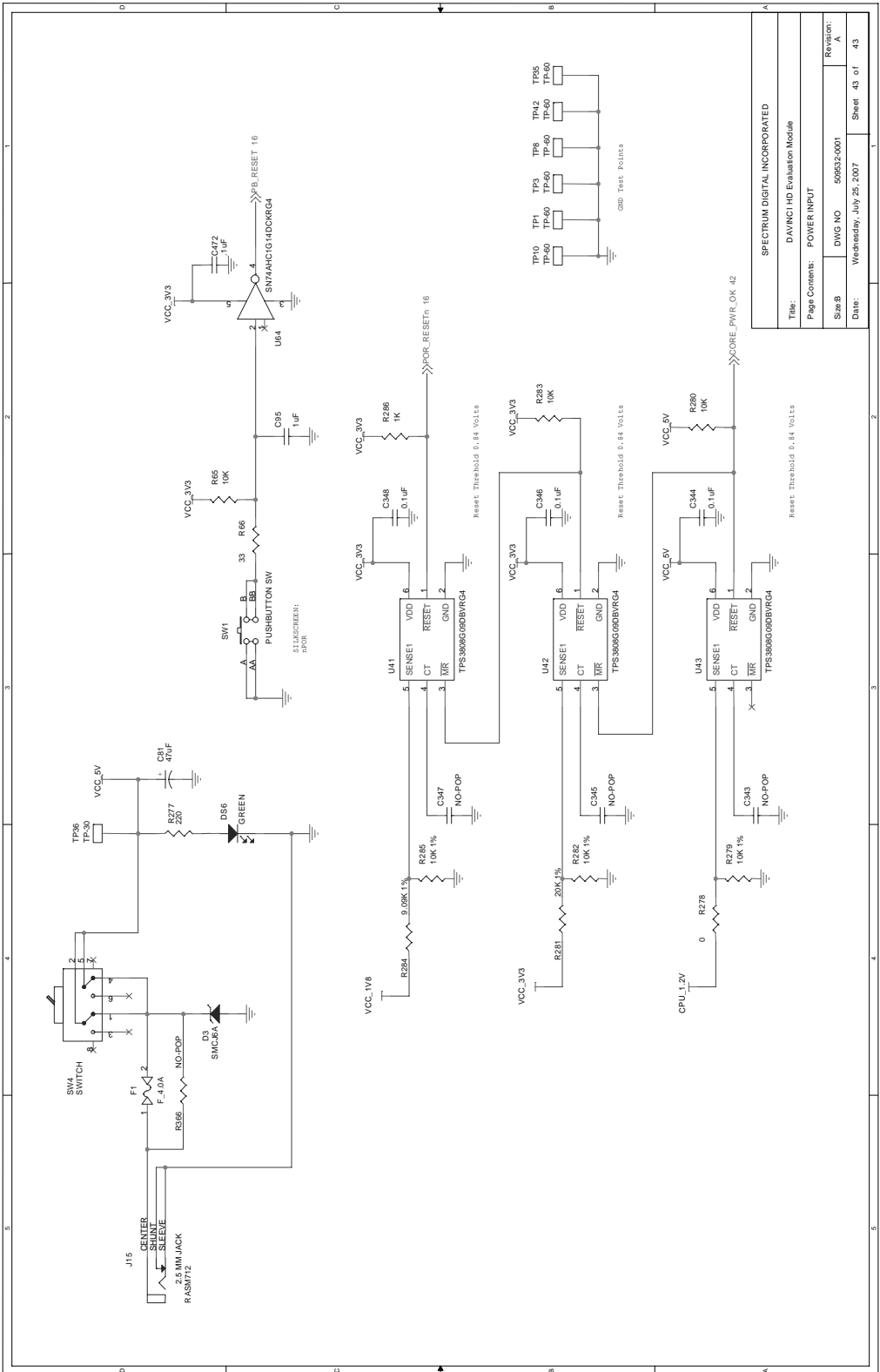


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Size B	DWG NO 50552-0001
Date: Wednesday, July 25, 2007	Sheet 40 of 43
Revision: C	



SPECTRUM DIGITAL INCORPORATED	
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Page Contents:	DSP CORE POWER
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Rev:	Rev: 1.0
Date:	Wednesday, July 25, 2007
Sheet	41 of 43





# Appendix B

## Mechanical Information

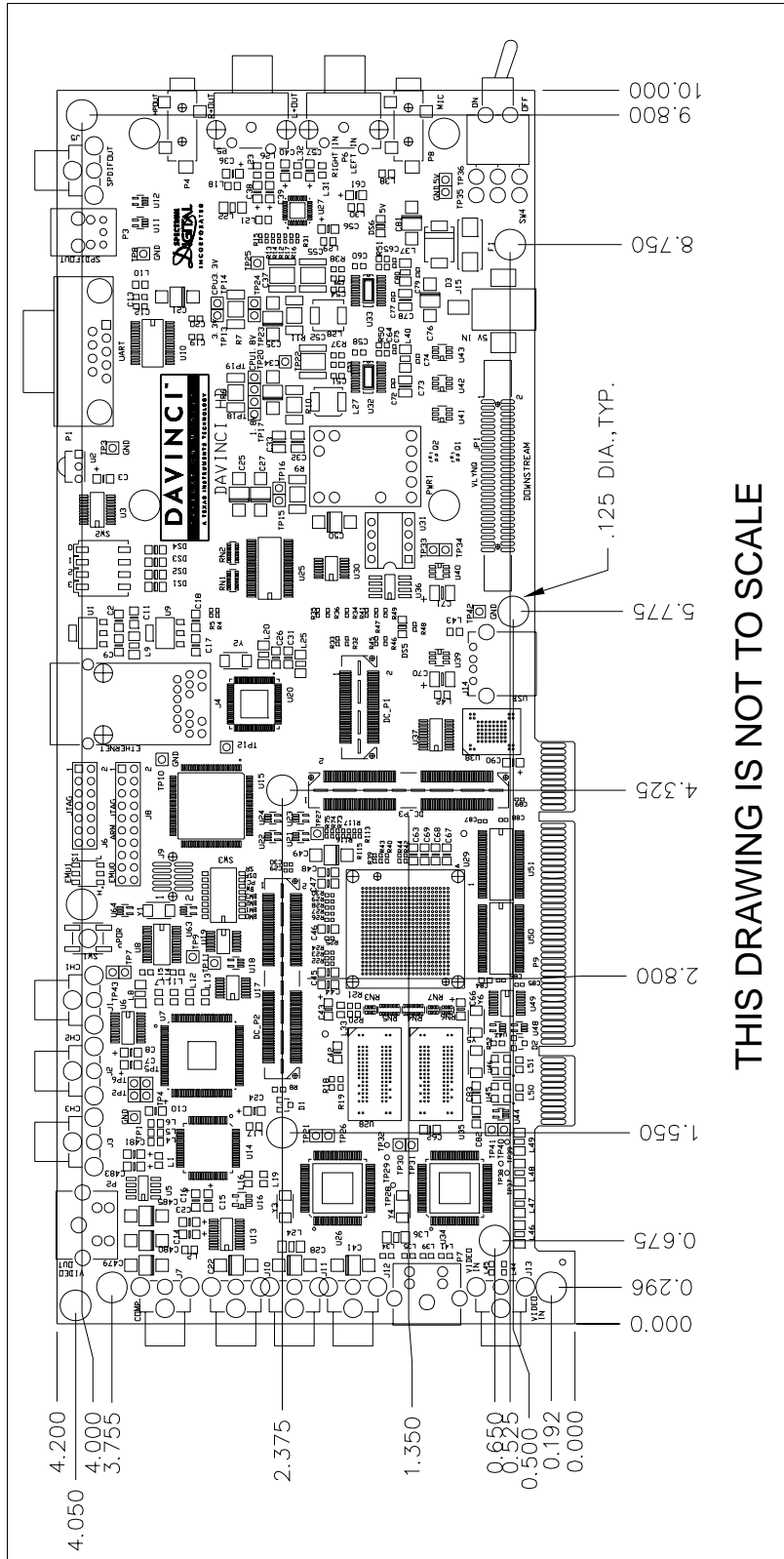
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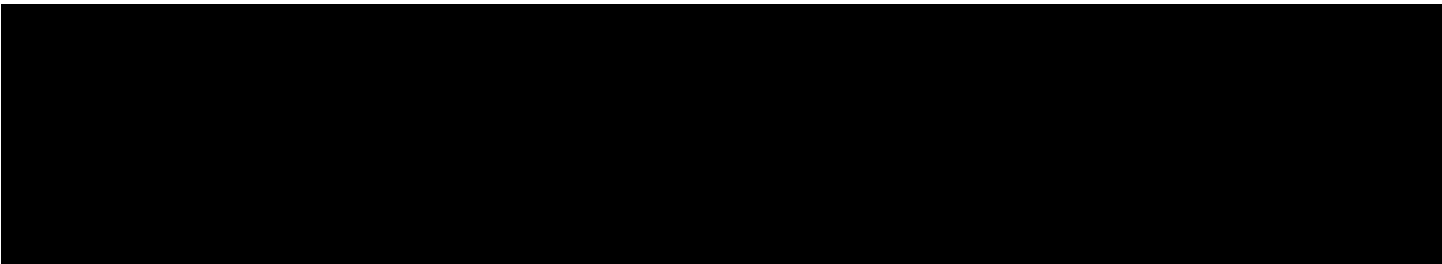
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This appendix contains the mechanical information about the TMS320DM6467 EVM produced by Spectrum Digital.



THIS DRAWING IS NOT TO SCALE





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Printed in U.S.A., July 2007  
509535-0001 Rev A