

FDD6N25 / FDU6N25

250V N-Channel MOSFET

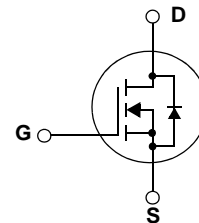
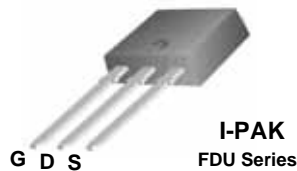
Features

- 4.4A, 250V, $R_{DS(on)} = 1.1\Omega @ V_{GS} = 10V$
- Low gate charge (typical 4.5 nC)
- Low C_{rss} (typical 5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



Absolute Maximum Ratings

Symbol	Parameter	FDD6N25 / FDU6N25	Unit
V_{DSS}	Drain-Source Voltage	250	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	4.4 2.6	A A
I_{DM}	Drain Current - Pulsed (Note 1)	18	A
V_{GSS}	Gate-Source voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	45	mJ
I_{AR}	Avalanche Current (Note 1)	4.4	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	50 0.4	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD6N25	FDD6N25TM	D-PAK	380mm	16mm	2500
FDD6N25	FDD6N25TF	D-PAK	380mm	16mm	2000
FDU6N25	FDU6N25TU	I-PAK	-	-	70

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	250	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	--	0.25	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 250V, V _{GS} = 0V V _{DS} = 200V, T _C = 125°C	--	--	1 10	μA μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30V, V _{DS} = 0V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30V, V _{DS} = 0V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3.0	--	5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10V, I _D = 2.2A	--	0.9	1.1	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40V, I _D = 2.2A (Note 4)	--	5.5	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	--	194	250	pF
C _{oss}	Output Capacitance		--	38	50	pF
C _{rss}	Reverse Transfer Capacitance		--	5	8	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 125V, I _D = 6A R _G = 25Ω (Note 4, 5)	--	10	30	ns
t _r	Turn-On Rise Time		--	25	60	ns
t _{d(off)}	Turn-Off Delay Time		--	7	24	ns
t _f	Turn-Off Fall Time		--	12	34	ns
Q _g	Total Gate Charge	V _{DS} = 200V, I _D = 6A V _{GS} = 10V (Note 4, 5)	--	4.5	6	nC
Q _{gs}	Gate-Source Charge		--	1.5	--	nC
Q _{gd}	Gate-Drain Charge		--	1.8	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	4.4	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	18	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0V, I _S = 4.4A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _S = 6A di _F /dt = 100A/μs (Note 4)	--	145	--	ns
Q _{rr}	Reverse Recovery Charge		--	0.55	--	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 3.7mH, I_{AS} = 4.4A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 4.4A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

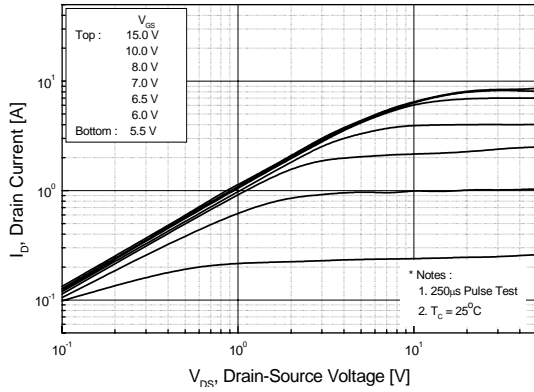


Figure 2. Transfer Characteristics

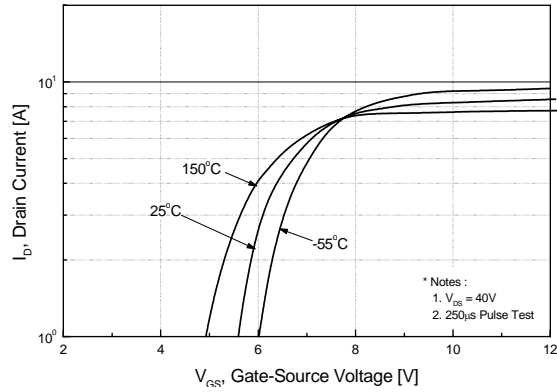


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

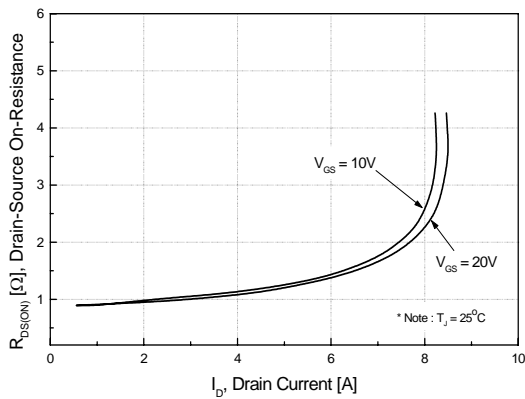


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

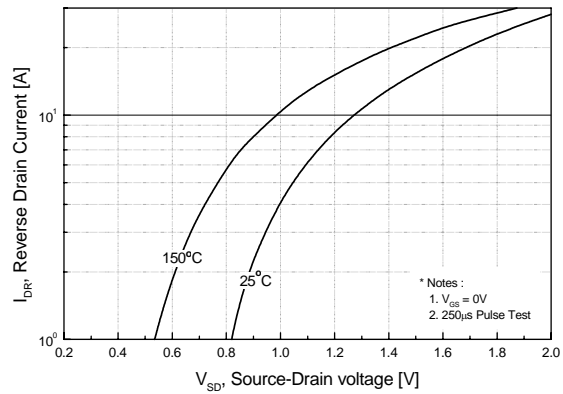


Figure 5. Capacitance Characteristics

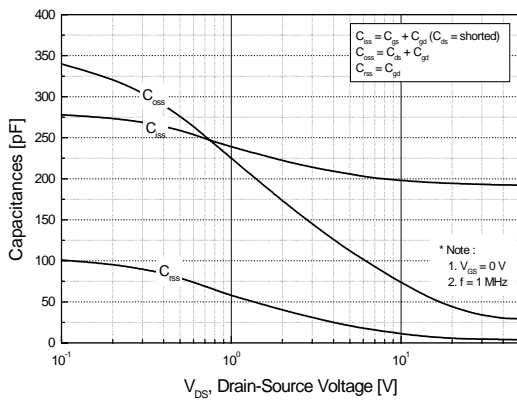
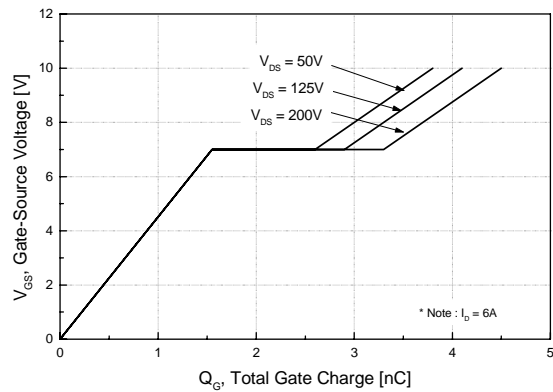


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

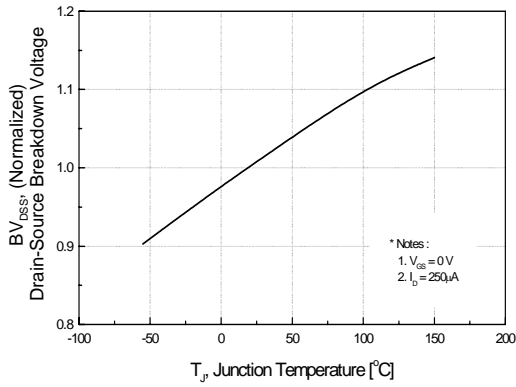


Figure 8. On-Resistance Variation vs. Temperature

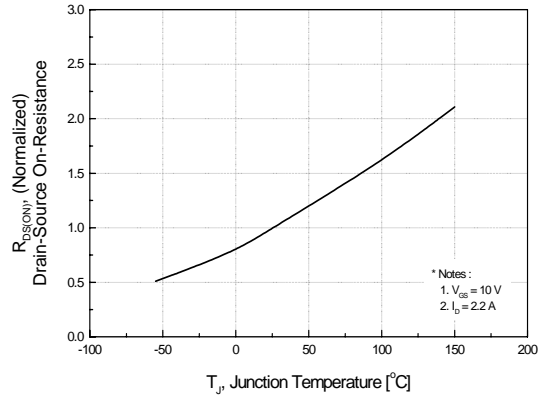


Figure 9. Maximum Safe Operating Area

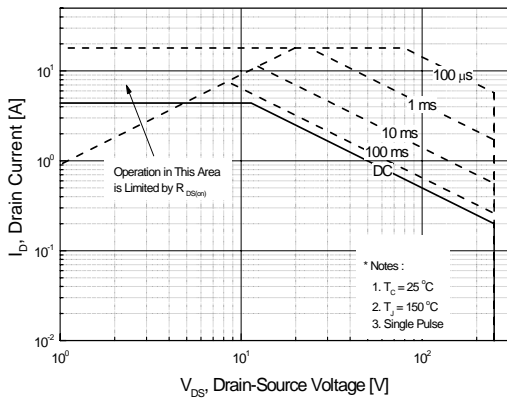


Figure 10. Maximum Drain Current vs. Case Temperature

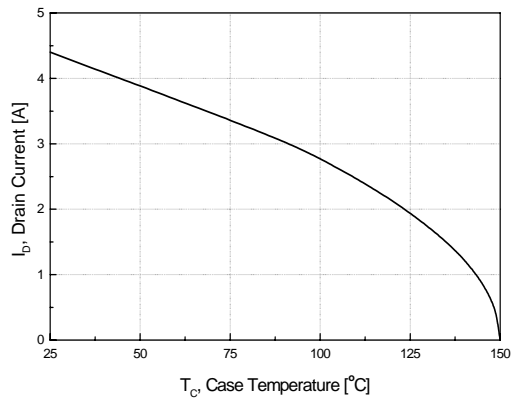
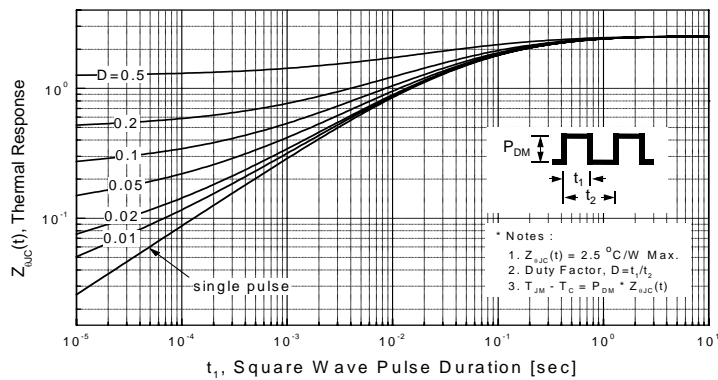


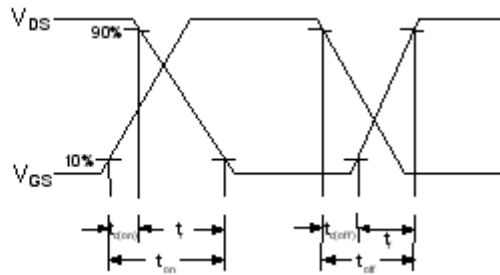
Figure 11. Transient Thermal Response Curve



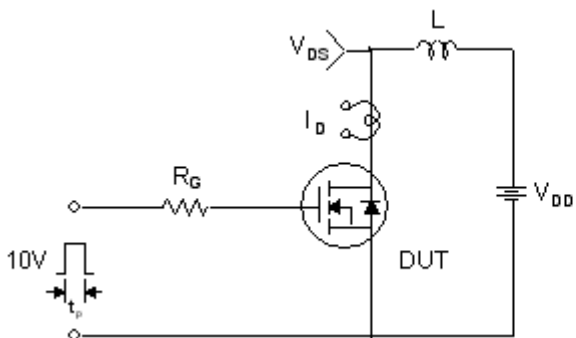
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

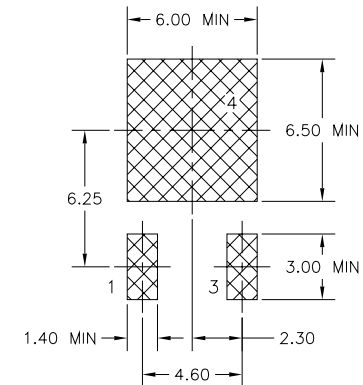
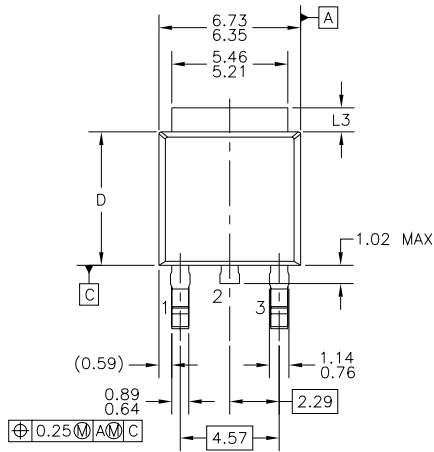


Peak Diode Recovery dv/dt Test Circuit & Waveforms

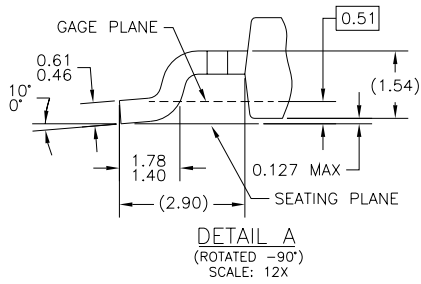
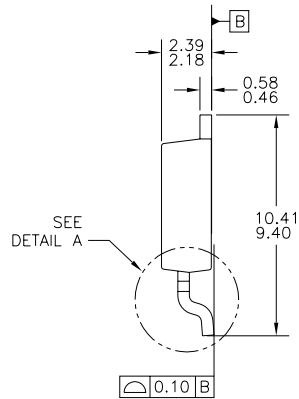
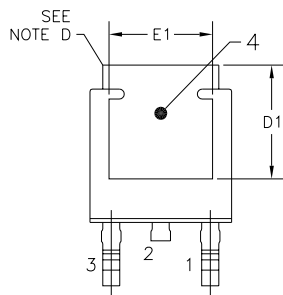


Mechanical Dimensions

D-PAK



LAND PATTERN RECOMMENDATION

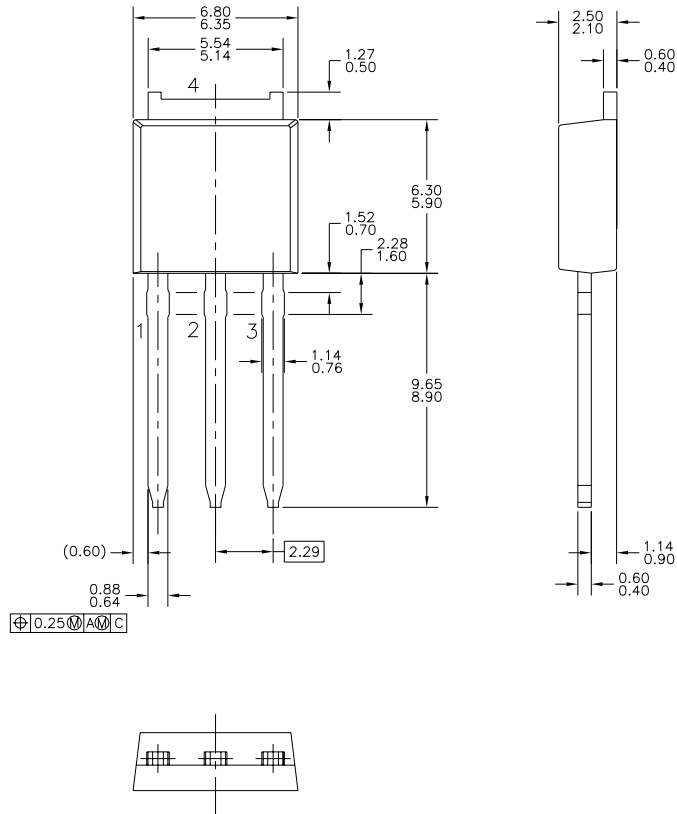


NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3,D,E1&D1 TABLE:
- | | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN | 3.81 MIN |
| D1 | 5.21 MIN | 4.57 MIN |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Mechanical Dimensions


I-PAK





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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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