AK1110AEU

2ch Output, Ultra High PSRR, Ultra Low Noise LDO Regulator

1. General Description

The AK1110AEU is a dual output low dropout linear regulator with ON/OFF control. Each output can supply 100mA and 200mA load current. The AK1110AEU is an integrated circuit achieving excellent ripple rejection and low output noise characteristics with silicon monolithic bipolar structure. In addition, over current and thermal protections are integrated. It is especially well suited for noise sensitive applications. The AK1110AEU is housed in a small and thin type PLP10-2725 package with an exposed pad. It is designed for space saving requiring systems.

2. Feature

- Operating Voltage Range 6V to 14V
- Maximum Output Current LDO1 200mA
  LDO2 100mA
- High Precision output voltage LDO1 5.0V
  LDO2 5.0V
- Dropout Voltage LDO1 600mV at Io=200mA
  LDO2 600mV at Io=100mA
- Output Noise LDO1 2μ V_{RMS} at 10Hz to 100kHz
  LDO2 1μ V_{RMS} at 10Hz to 100kHz
- Ripple Rejection Ratio LDO1 83dB at f=1kHz
  LDO2 100dB at f=1kHz
- NP terminal to reduce output noise
- On/Off Control Function
- Over Current Protection, Thermal Protection
- Ceramic Capacitor Available
- Small Package PLP10-2725 (2.7mm×2.5mm×0.6mm)

3. Application

- High precision DAC applications, RF, PLL, etc.

4. Table of Contents

5. Block Diagram

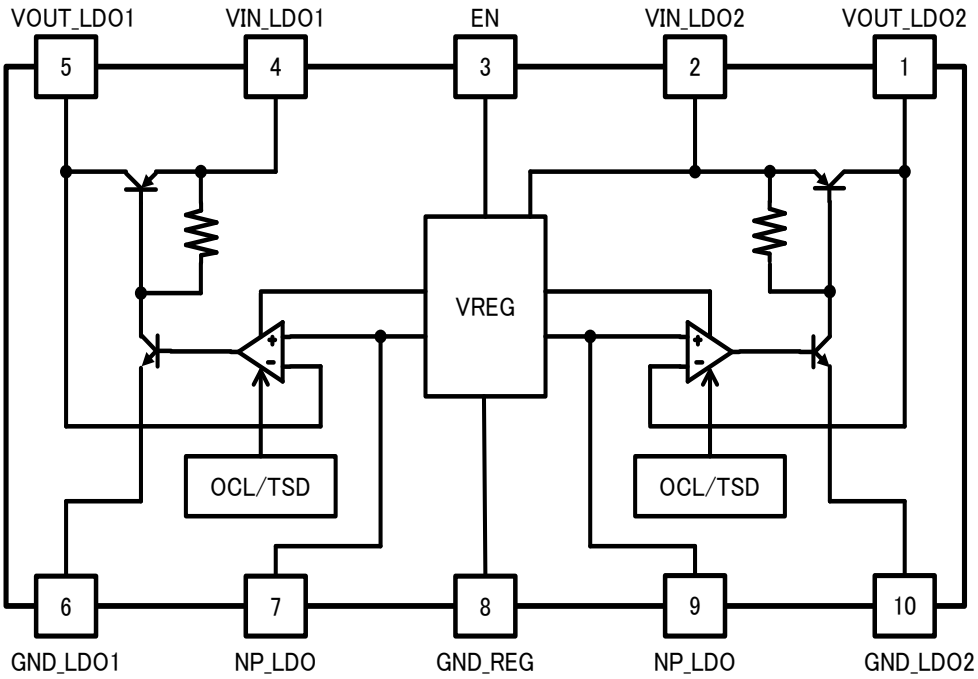


Figure 1. Block Diagram

6. Pin Configurations and Functions

■ Pin Configurations

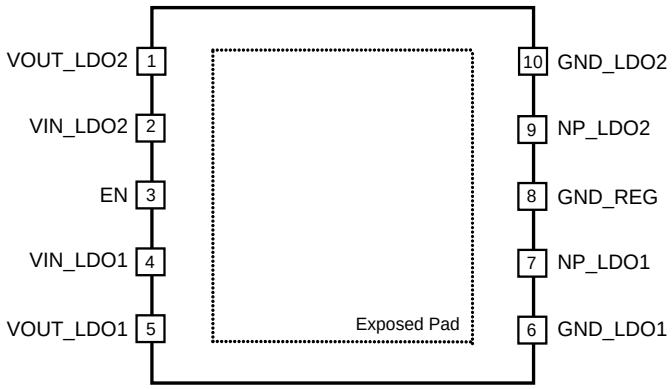


Figure 2. Pin Configurations (Top View)

■ Pin Functions

No.	Name	I/O	Internal Equivalent Circuit	Description
1	VOUT_LDO2	O	Figure 3	LOD2 Output
2	VIN_LDO2	P	Figure 3	LOD2 Input
3	EN	I	Figure 4	On/Off Control Terminal of the LDO1 and LDO2 (High active) The pull-down resister (300kΩ) is built-in.
4	VIN_LDO1	P	Figure 3	LDO1 Input
5	VOUT_LDO1	O	Figure 3	LDO1 Output
6	GND_LDO1	-	-	LDO1 Ground
7	NP_LDO1	O	Figure 5	Noise Bypass Terminal of the LDO1 Connect a bypass capacitor between NP_LDO1 and GND.
8	GND_REG	-	-	GND terminal of the internal 5V regulator
9	NP_LDO2	O	Figure 5	Noise Bypass Terminal of the LDO2 Connect a bypass capacitor between NP_LDO2 and GND.
10	GND_LDO2	-	-	LDO2 Ground
-	Exposed Pad (Note 2)	-	-	Heat Dissipation Pad It is connected to GND internally.

Note 1. I(Input terminal), O(Output terminal), P(Power terminal)
Note 2. The exposed pad should be connected to the GND plane.

Equivalent Circuits

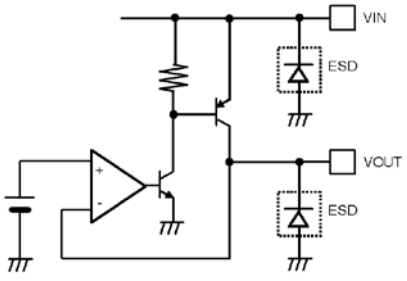


Figure 3

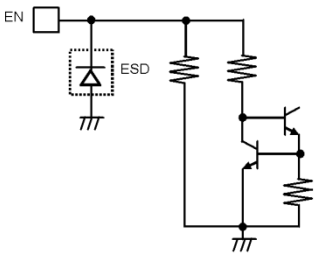


Figure 4

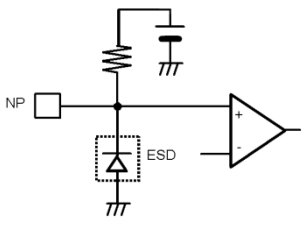


Figure 5

7. Absolute Maximum Ratings

(GND_LDO1 = GND_LDO2 = GND_REG =0V)

Parameter	Symbol	Min.	Max.	Unit	Condition
Supply Voltage (VIN_LDO1, VIN_LDO2)	V_{IN}	-0.3	16	V	
Reverse Bias (VOUT_LDO1, VOUT_LDO2)	V_{REV}	-0.3	6	V	
Np Terminal Voltage (NP_LDO1, NP_LDO2)	V_{NP}	-0.3	16	V	
EN Terminal Voltage (EN)	V_{EN}	-0.3	16	V	
GND_LDO1- GND_LDO2 GND_LDO1- GND_REG GND_LDO2- GND_REG	VGND	-0.3	0.3	V	
Junction Temperature	T_j	-	150	°C	
Storage Temperature Range	T_{STG}	-55	150	°C	
Power Dissipation	P_D	-	1800	mW	(Note 5)

Note 3. All voltages are with respect to GND. GND=0V

Note 4. The exposed pad should be connected to the GND plane.

Note 5. When the temperature is more than 25°C, derating by -18mW is needed. Thermal resistance θ_{JA}= 55.4 °C /W (Mounted on the four-layer board that conforms to the JEDEC51)

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

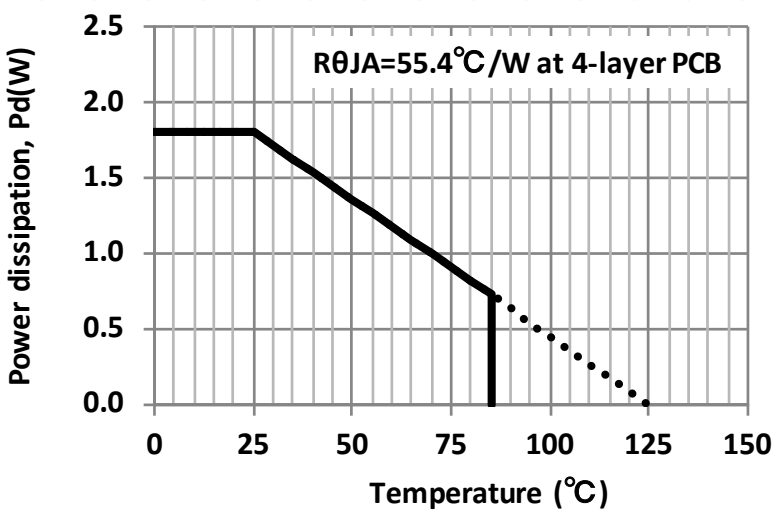


Figure 6. Thermal Derating Curve

8. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comments
Operating Temperature Range	T_a	-40	-	85	°C	
Operating junction temperature	T_j	-40		125	°C	
Operating Voltage Range	V_{IN}	6	-	14	V	

Note 6. All voltages are with respect to GND. GND=0V

9. Electrical Characteristics

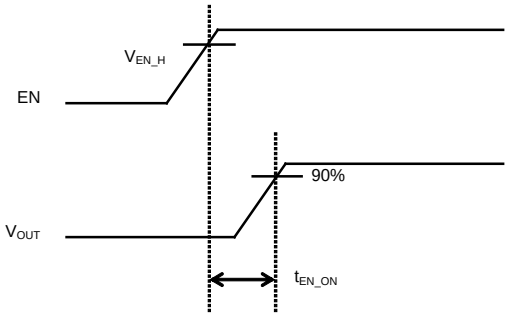
(Ta= −40°C ~ +85°C, V_{IN}=V_{EN}=6.0V, C_{IN}=1.0uF, C_{NP1}=C_{NP2}=10uF, C_{OUT1}=C_{OUT2}=10uF)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Common items of LDO1 and LDO2						
Quiescent Current	I_Q	I_{OUT} = 0mA	-	3.0	5.0	mA
Ground Terminal Current	I_{GND}	I_{OUT1}+I_{OUT2} =32mA	-	5.0	7.0	mA
Standby Current	$I_{STANDBY}$	V_{EN}=0V	-	0.01	2.0	μA
EN terminal high level	V_{ENH}		1.8	-	-	V
EN terminal Low level	V_{ENL}		-	-	0.35	V
EN Terminal Current	I_{ENLKG}	V_{EN}=1.8V	-	50	150	μA
EN terminal on time (Note 10)	t_{ENON}		-	55	100	ms
Thermal protection Shutdown Temperature	T_{TSD}		135	-	155	°C
LDO1						
Output Voltage	V_{OUT1}	I_{OUT1}= 1mA to 200mA	4.90	5.0	5.10	V
Line Regulation	$LinReg_1$	ΔV_{IN1} = 5V		6	20	mV
Load Regulation	$LoaReg_1$	I_{OUT1}= 1mA to 200mA			50	mV
Dropout Voltage	V_{DROP1}	I_{OUT1} = 200mA			600	mV
Maximum Output Current (Note 9)	$I_{OUTMAX1}$	V_{OUT1} = V_{OUT1}(typ)×0.9	220			mA
Output noise(Note 8)	V_{noise1}	I_{OUT1}=100mA, f=10Hz to100kHz		2.0		μV_{RMS}
Ripple rejection (Note 8)	$PSRR_1$	I_{OUT1} = 100mA, f=1kHz		83		dB
		I_{OUT1} = 100mA, f=100kHz		80		dB
		I_{OUT1} = 100mA, f=1MHz		70		dB
LDO2						
Output Voltage	V_{OUT2}	I_{OUT2}= 1mA to 100mA	4.90	5.0	5.10	V
Line Regulation	$LinReg_2$	ΔV_{IN2} = 5V		5	15	mV
Load Regulation	$LoaReg_2$	I_{OUT2} = 1mA to 100mA			25	mV
Dropout Voltage	V_{DROP2}	I_{OUT2} = 100mA			600	mV
Maximum Output Current (Note 9)	$I_{OUTMAX2}$	V_{OUT2} = V_{OUT2}(typ)×0.9	120			mA

(Ta= −40°C ~ +85°C, V_{IN}= V_{EN} =6.0V, C_{IN}=1.0uF, C_{NP1}= C_{NP2}=10uF, C_{OUT1}= C_{OUT2}=10uF)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output Noise (Note 8)	V_{noise2}	I_{OUT2} = 1mA, f=10Hz to100kHz		1.0		μV_{RMS}
Ripple Rejection (Note 8)	$PSRR_2$	I_{OUT2} = 1mA, f=1kHz		100		dB
		I_{OUT2} = 1mA, f=100kHz		83		dB
		I_{OUT2} = 1mA, f=1MHz		76		dB

Note 7. All voltages are with respect to GND. GND=0V
Note 8. Guaranteed by design. This value is not tested.
Note 9. The maximum output current is limited by Ta and power dissipation.
Note 10. Definition of rise time is shown below.



10. Functional Descriptions

■ Output Capacitor and Stability

To ensure loop stability, select output capacitors that have more than 3.3uF effective capacitance and 0.1Ω or less ESR. If the capacity of the output capacitor is increased, peak voltage fluctuation caused by load current variation is reduced. Therefore, the transient response characteristics are improved. DC bias and temperature characteristics must be considered when using ceramic capacitors.

■ Noise Bypass Capacitor

It is recommended that the effective capacitance of the capacitor connected to the NP pin is 3.3 μF or higher. Increase the capacitance of a capacitor at the NP pin to prioritize the output noise and ripple rejection characteristics in the system design. The NP pin capacitance does not affect output stability.

■ Output Enable Control

Output ON/OFF control is available by the EN pin. When output is turned OFF, IC current consumption can be minimized.

EN terminal voltage (V_{EN})	Operating state
V_{EN} > 1.8V	ON
V_{EN} < 0.35V	OFF

■ Over Current Protection

The AK1110 limits the output current for IC protection when the output current exceeds the maximum rating such as when it is shorted to ground. The AK1110 automatically returns to normal operation when the output current decreases.

■ Thermal Protection

If the junction temperature exceeds the maximum rating as power loss of the AK1110 is large, the output of the AK1110 is turned off by the thermal protection function. The AK1110 automatically returns to normal operation when the junction temperature decreases.

■ Attention to PCB Layout

Package: PLP10-2725

Board Material: 4-layer glass epoxy substrate, (x=25mm, y=25mm, t=1.6mm, Copper pattern thickness 18um)

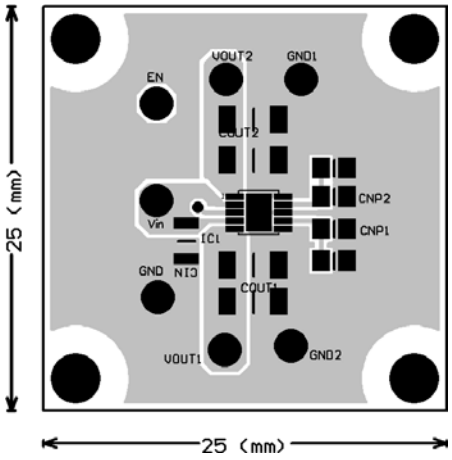


Figure 7. Recommended Layout

1. CIN should be located as close as possible to the VIN1, VIN2 pin and GND.
2. COUT1, COUT2 should be located as close as possible to the VOUT1, VOUT2 pin and GND.
3. CNP1, CNP2 should be located as close as possible to the NP1, NP2 pin and GND.
4. GND plane should be large as much as possible.
5. The exposed pad is a common ground of the IC. It must be connected to the PCB GND.
6. Via halls are effective for heat dissipation to each layer of PCB.

■ Characteristic Examples

C_{IN}=1.0uF, C_{NP1}= C_{NP2}=10uF, C_{OUT1}= C_{OUT2}=10uF

Noise Characteristics

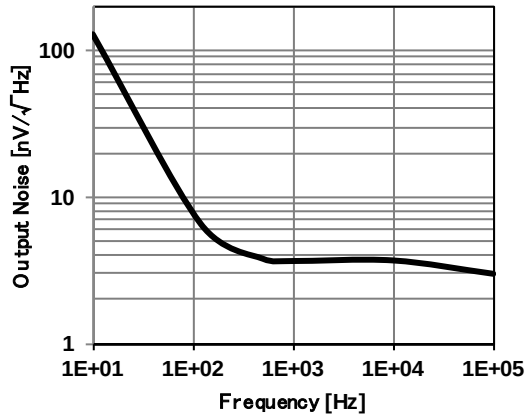
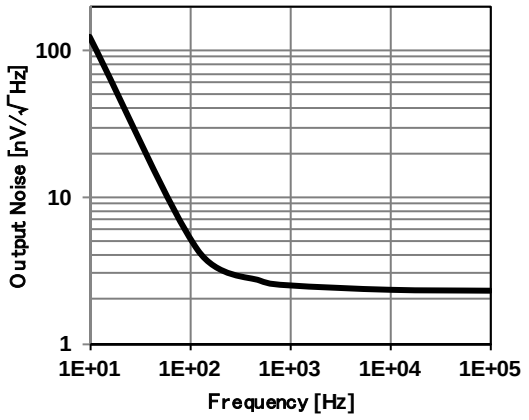
LDO1	LDO2
	

Figure 8. Output Noise Level (1/f)

To reduce the output noise, increase capacitance of the NP capacitors. A 3.3 uF or higher NP capacitor is recommended.

Ripple Rejection Characteristics

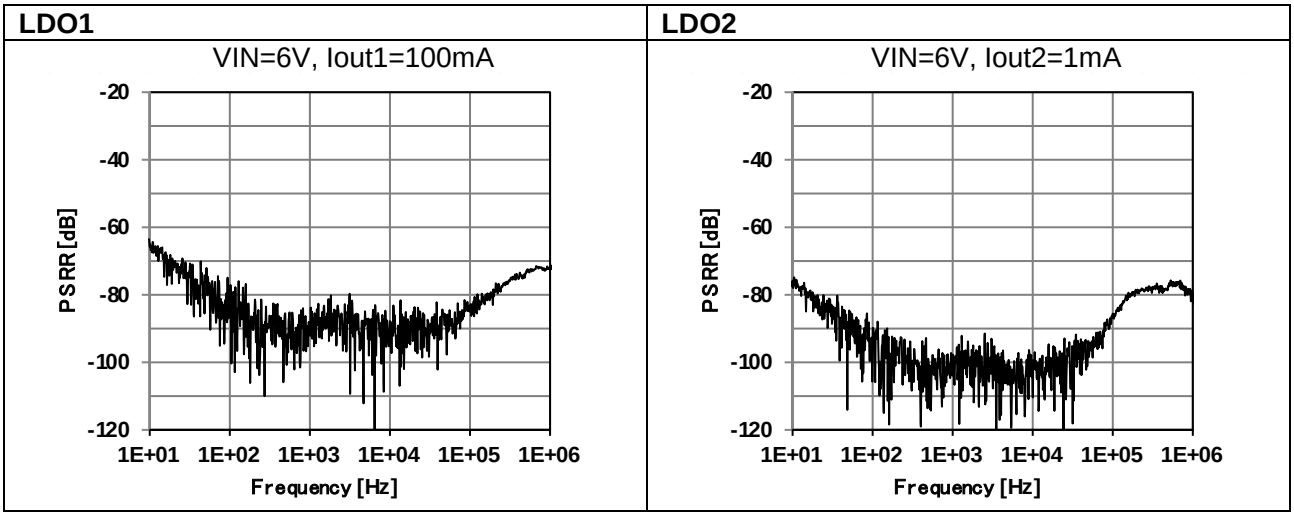


Figure 98. Ripple Rejection

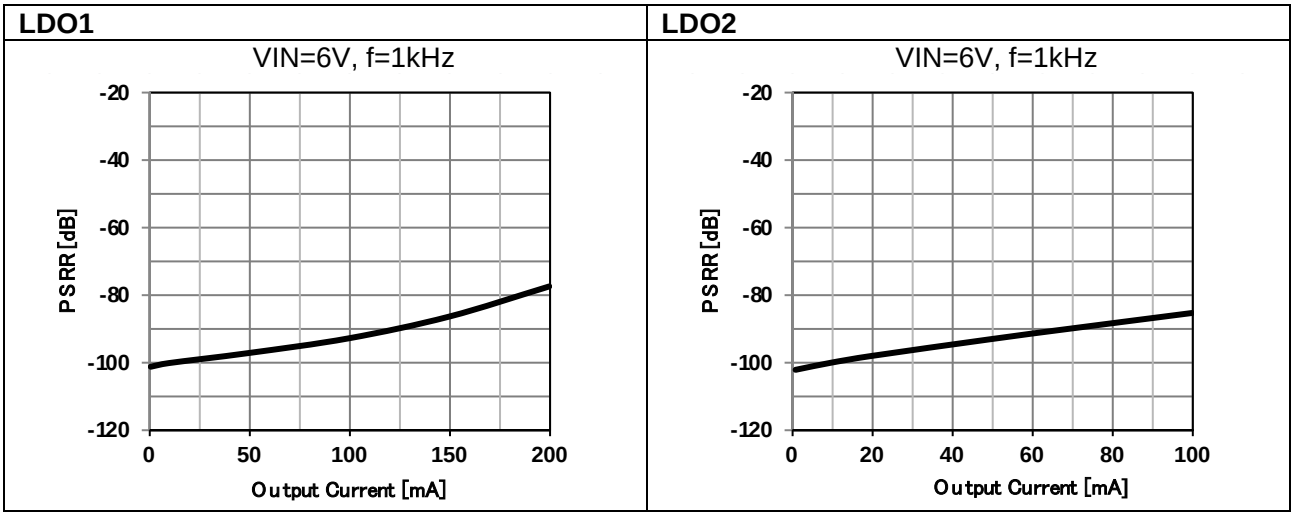


Figure 90. Ripple Rejection vs. Iout

The ripple rejection characteristic depends on the capacity and characteristics of the output capacitor. Ripple rejection characteristics over 50 kHz are greatly affected by the output capacitor capacitance and PCB pattern.

DC Characteristics

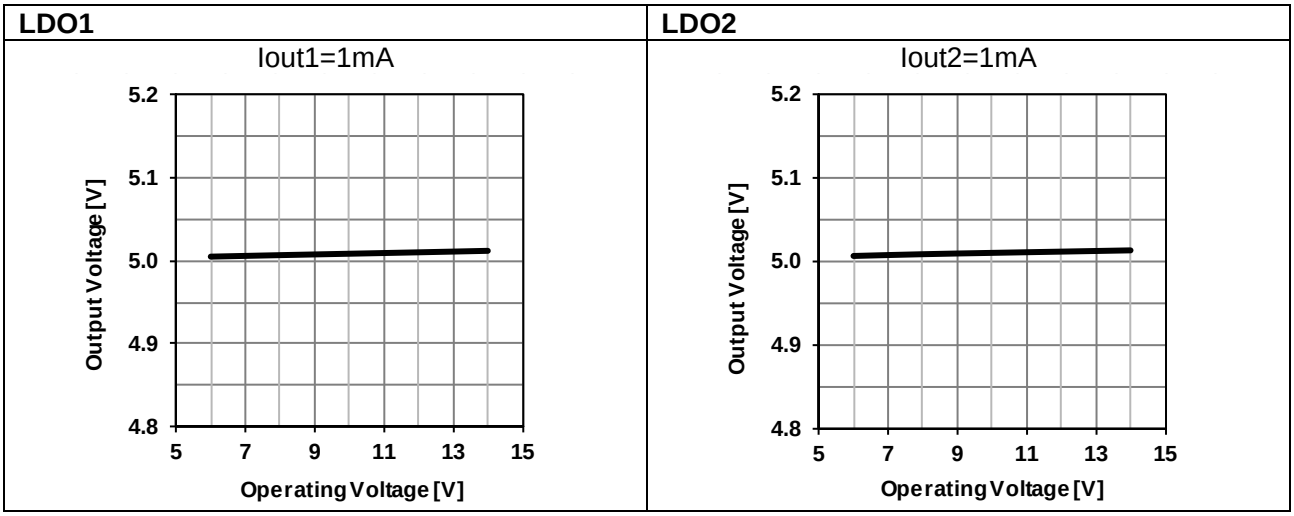


Figure 101. Input voltage fluctuation

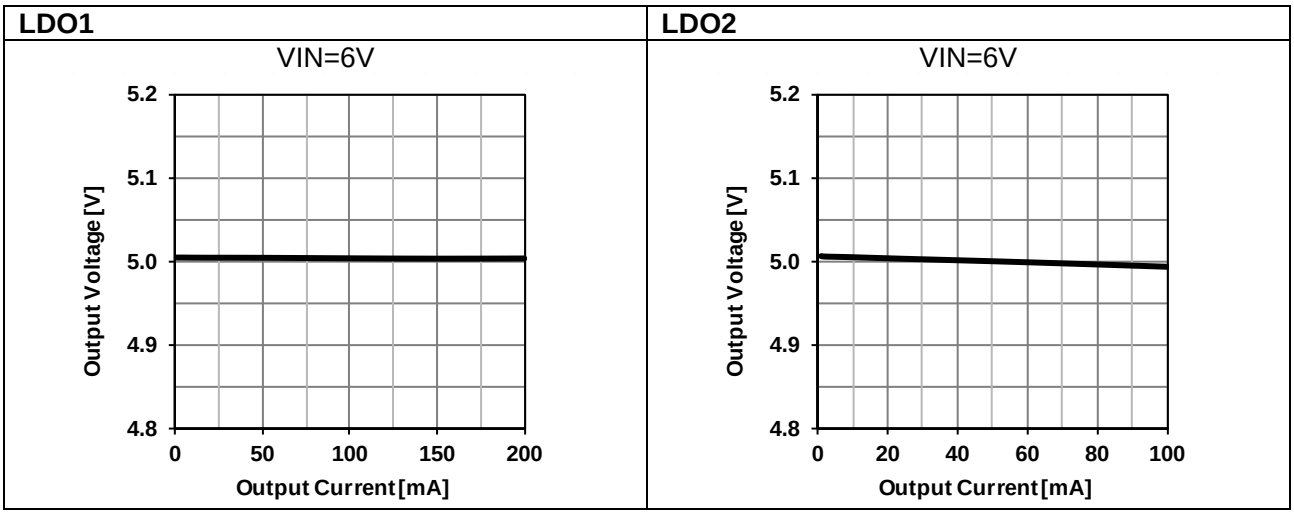


Figure 112. Load fluctuation

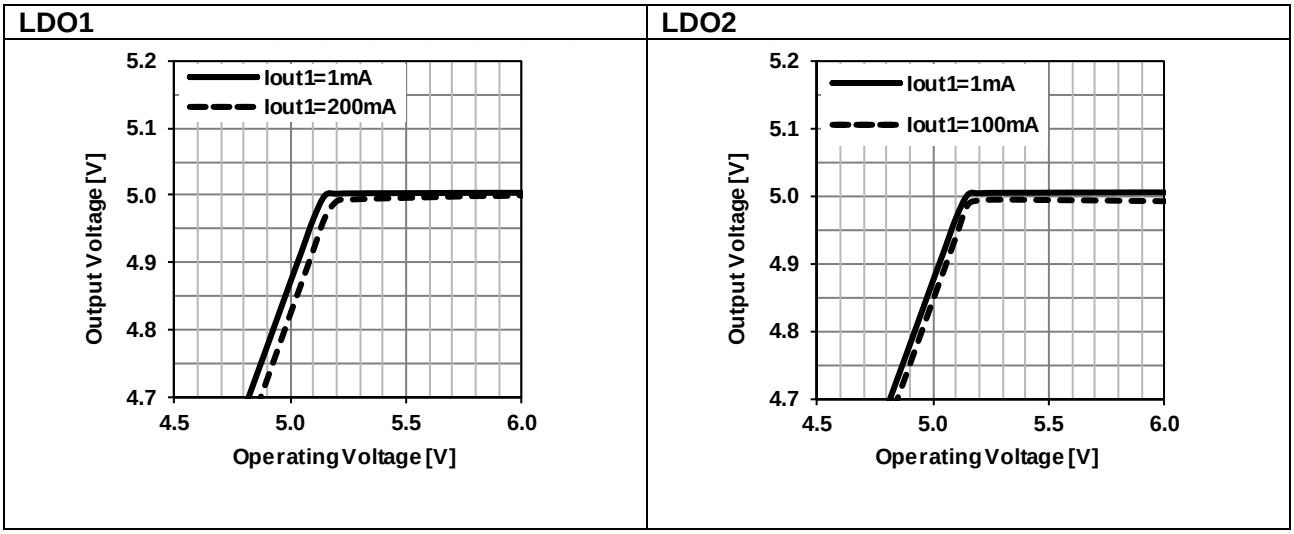


Figure 123. Input vs Output Voltage

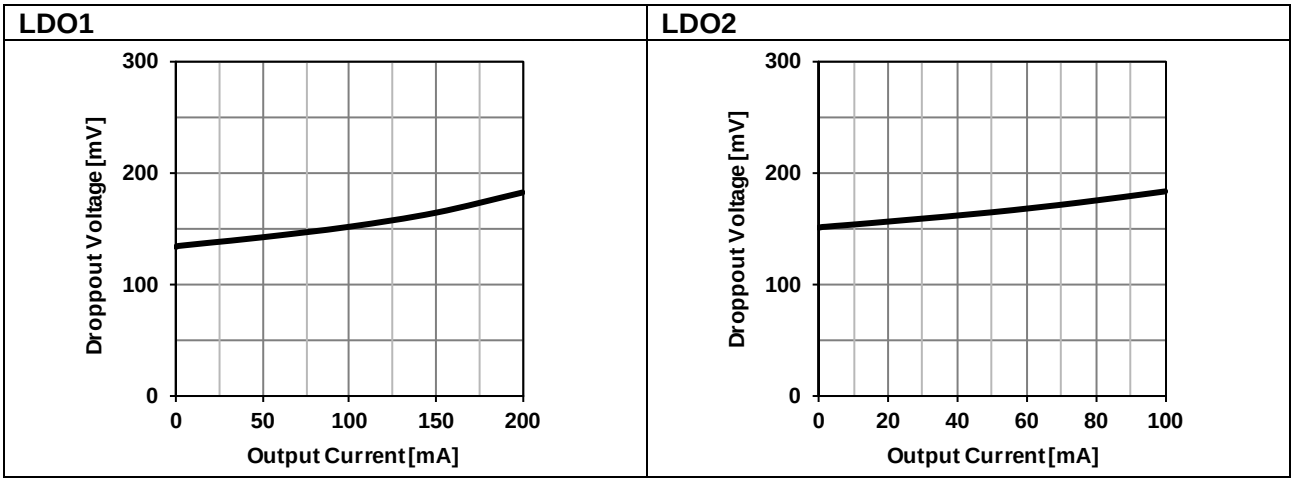


Figure 134. Dropout Voltage

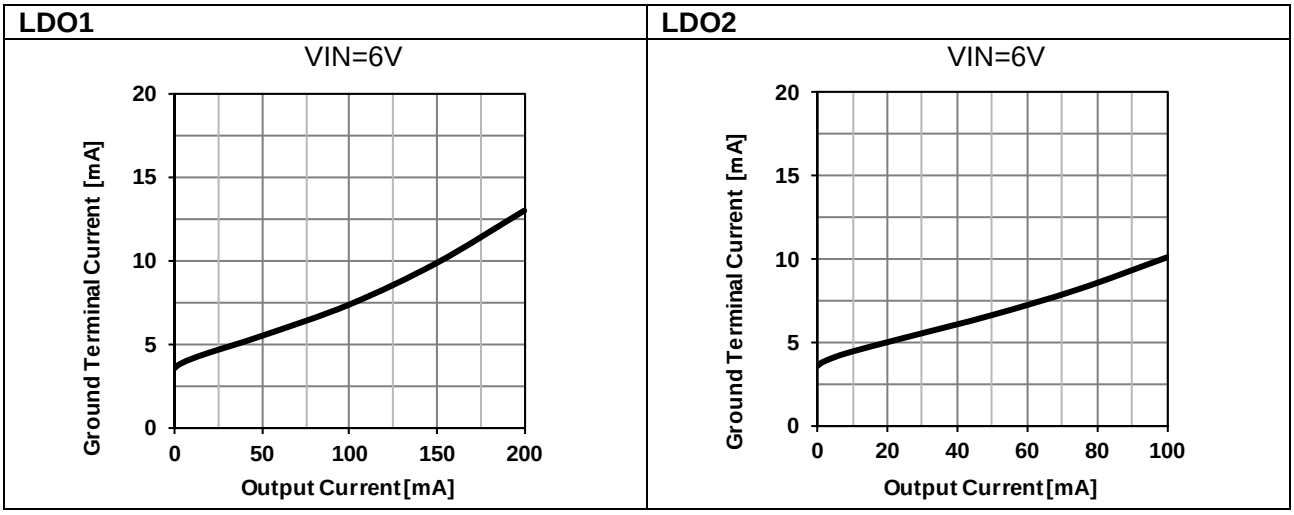


Figure 145. Ground Terminal Current

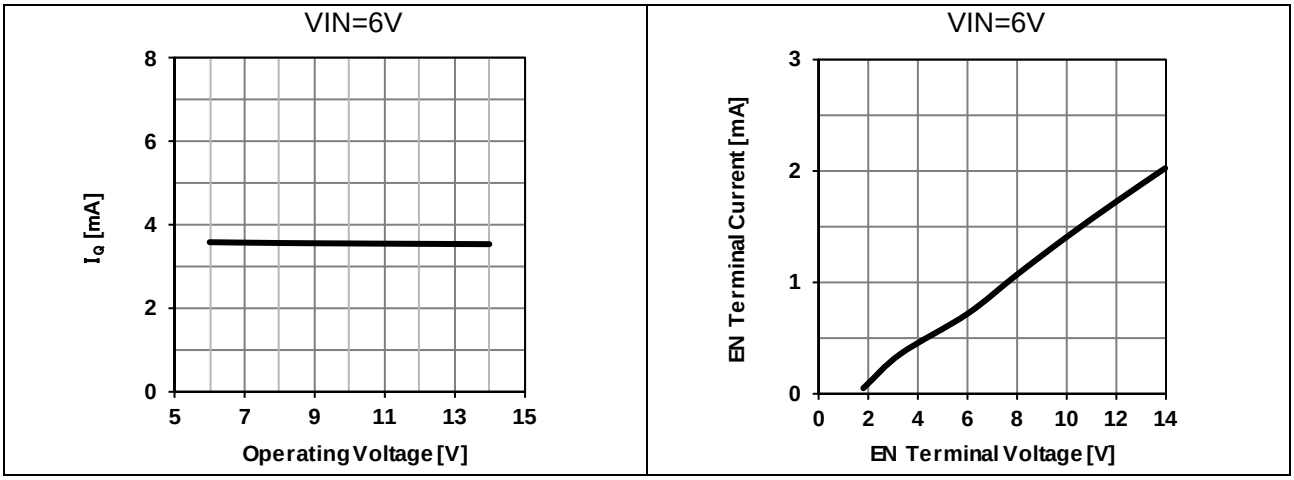


Figure 156. Quiescent Current

Figure 167. V_{EN} vs. I_{EN}

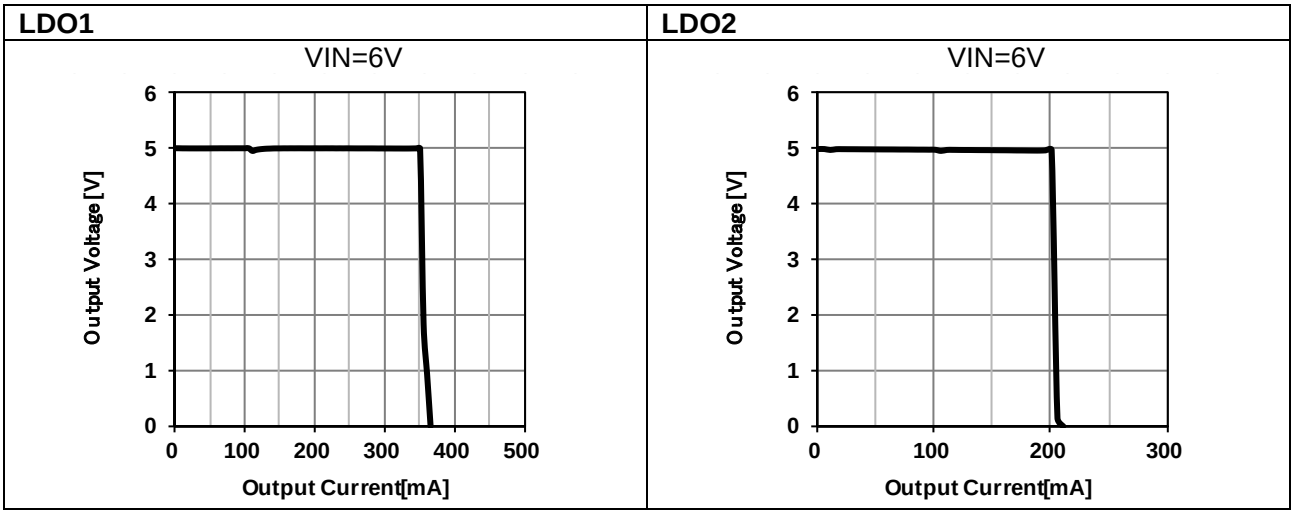


Figure 178. Overcurrent protection characteristics

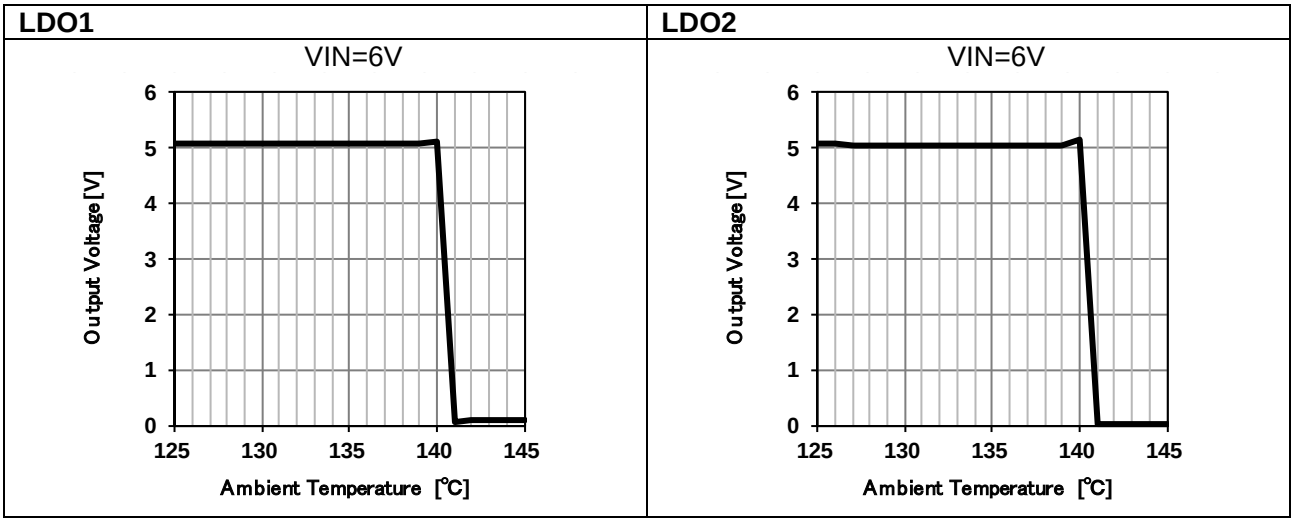


Figure19. Thermal Protection

Temperature Characteristic

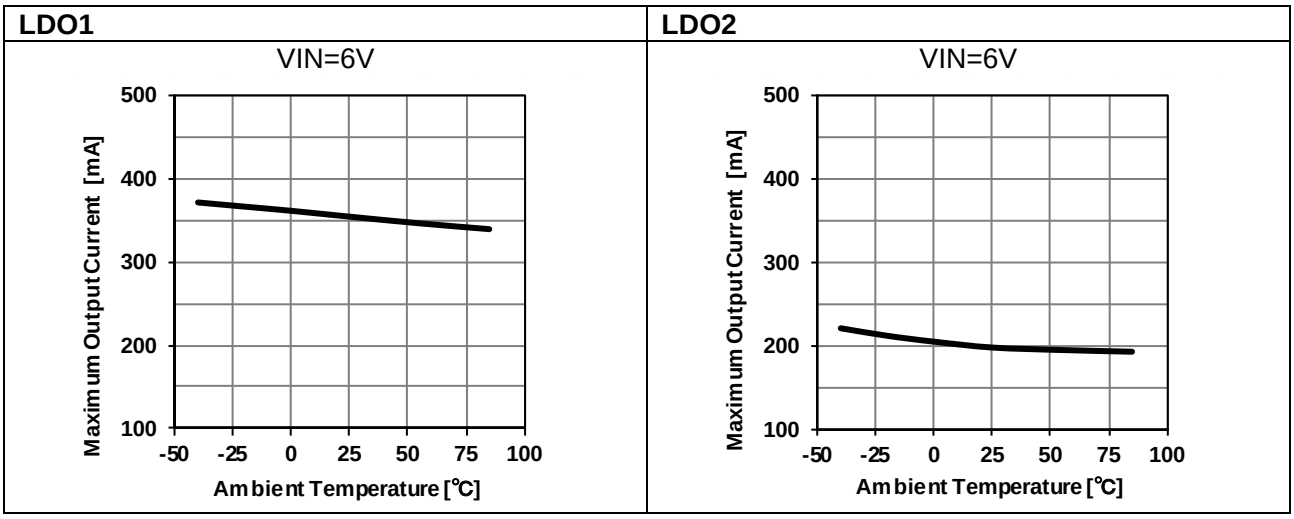


Figure 180. Maximum Output Current

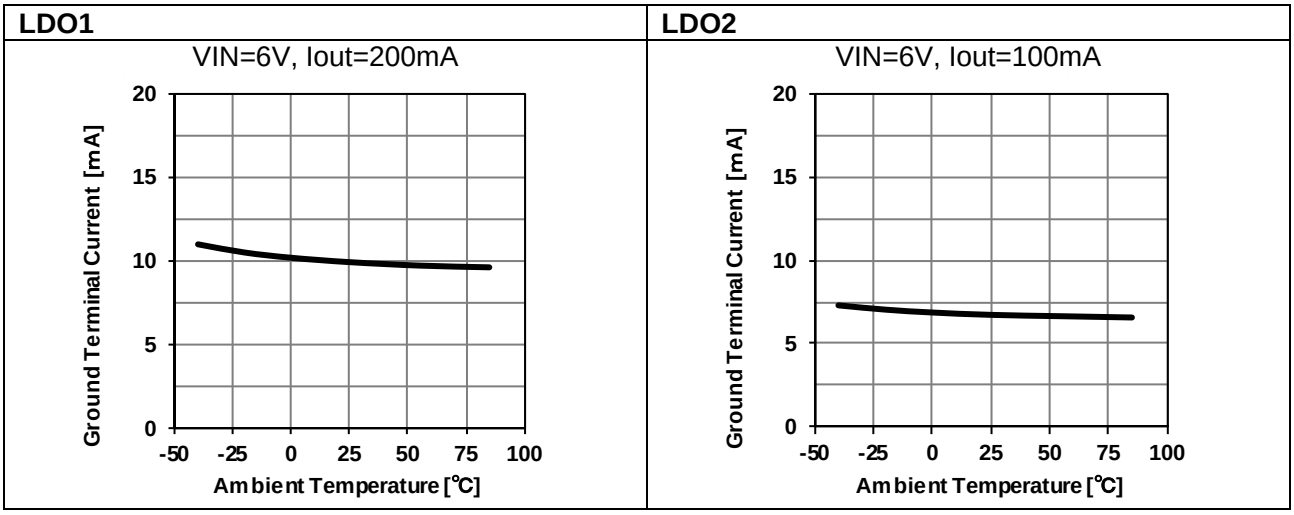


Figure 191. Ground Terminal Current

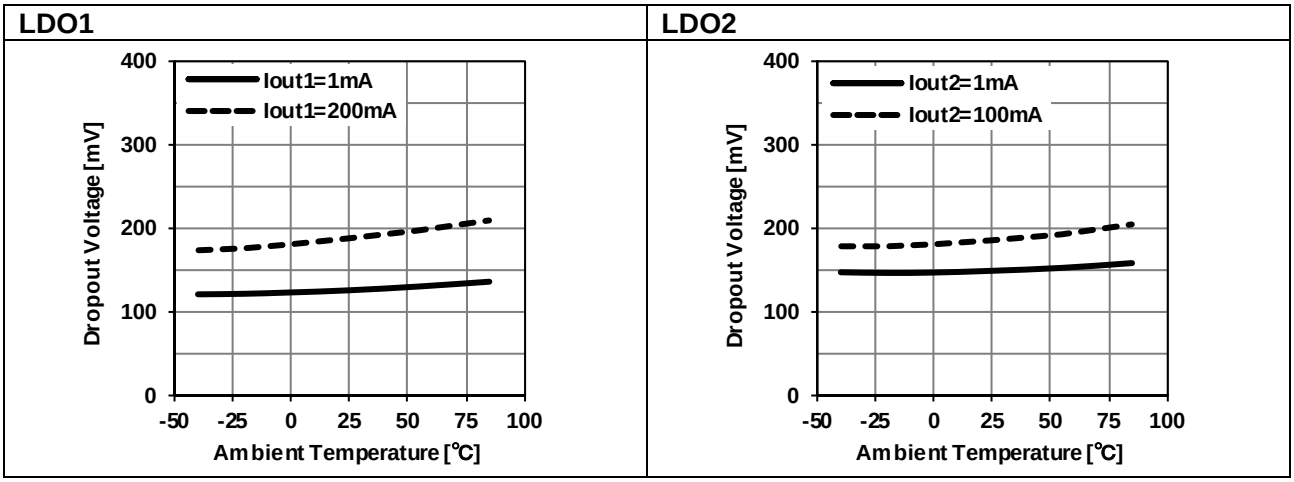


Figure 202. Dropout Voltage

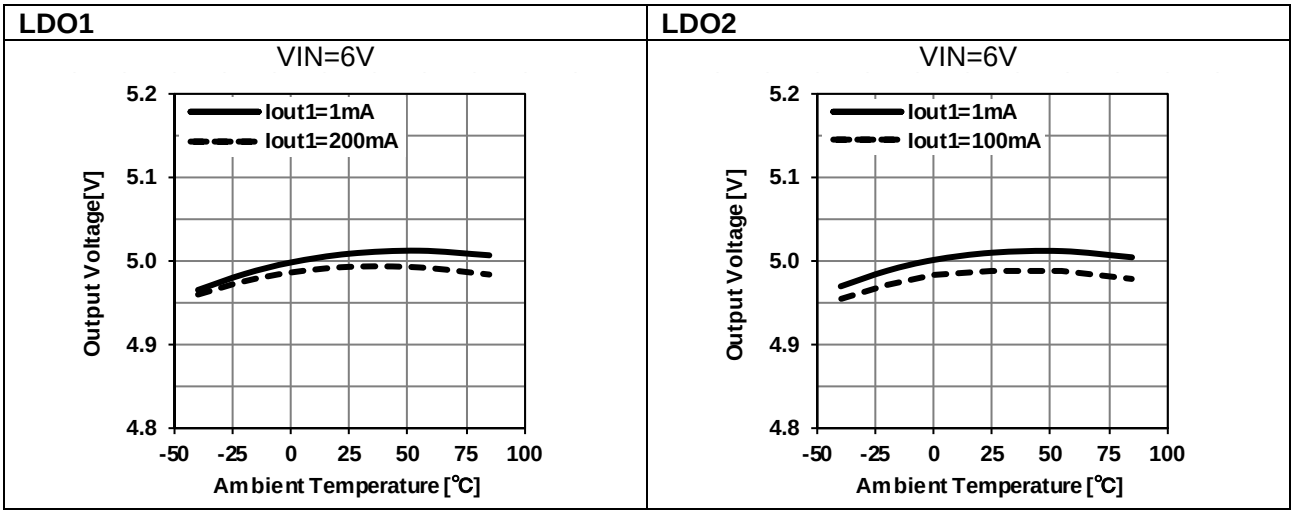


Figure 213. Output Voltage Temperature Characteristic

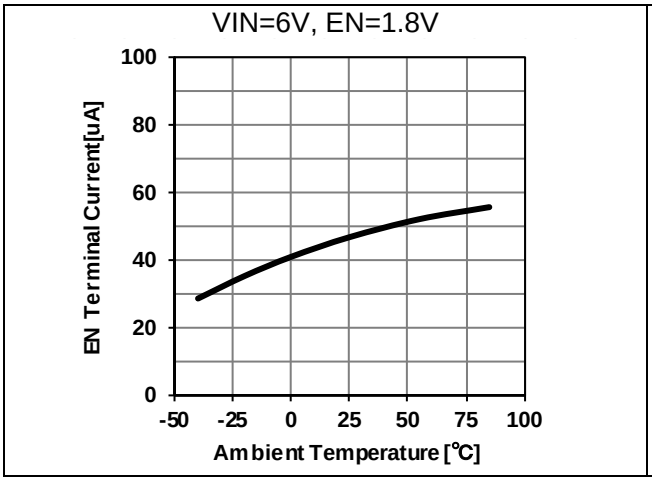


Figure 224. EN Terminal Current

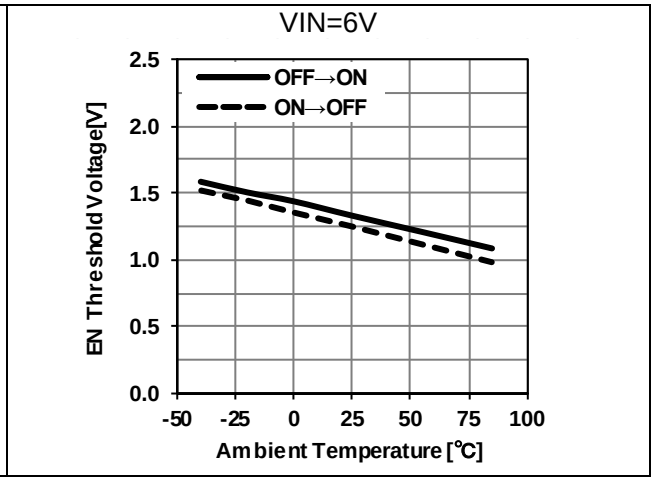


Figure 235. EN Threshold Voltage

Transient Characteristic

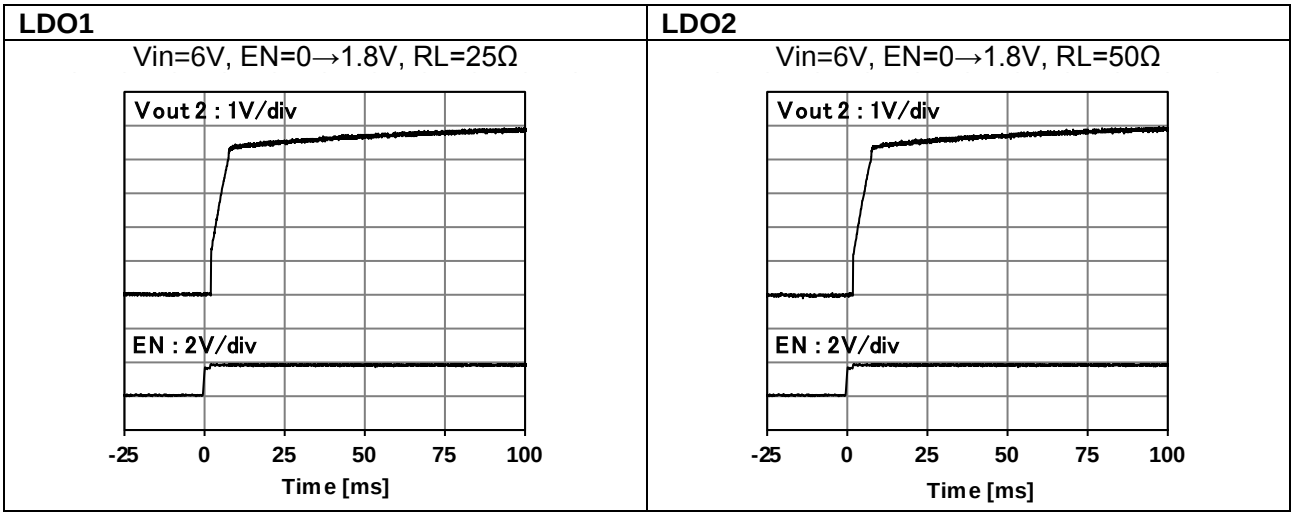


Figure 246. Starting Characteristic

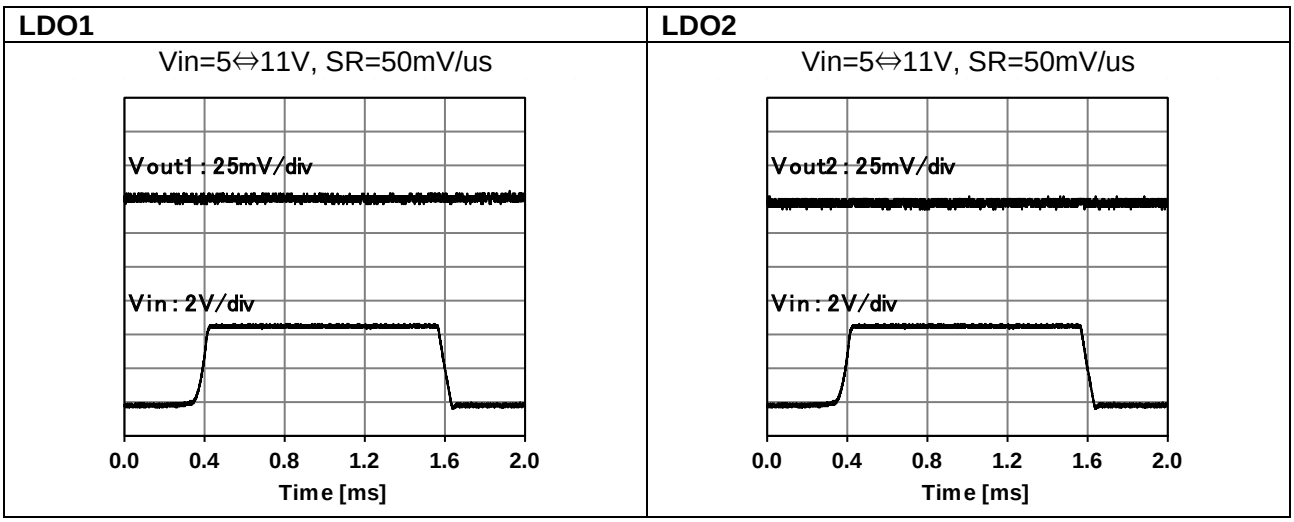
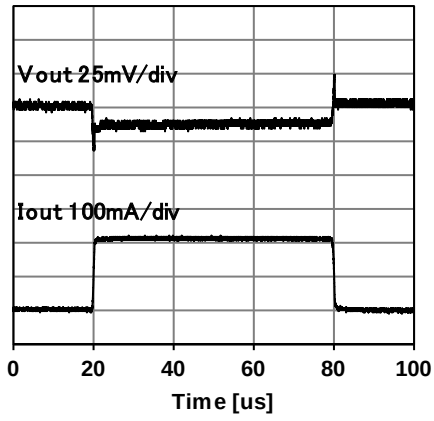


Figure 25. Line Transient

LDO1	LDO2
Iout = 1⇔200mA, SR = 100mA/us	Iout = 1⇔100mA, SR = 100mA/us



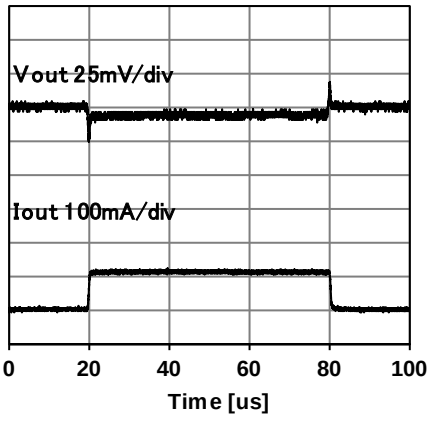


Figure 268. Load Transient

11. Definition of Terms

- **Maximum Output Current (I_{OUT_MAX})**
  It is defined as the output current that the output voltage with 1mA load current becomes 90%.

- **Dropout Voltage (V_{DROP})**
  It is a difference between the input voltage and the output voltage when the output voltage drops 100mV from its nominal value by decreasing the input voltage gradually.

- **Line Regulation (LinReg)**
  It is the fluctuation of the output voltage caused by input voltage variation.

- **Load Regulation (LoaReg)**
  It is the fluctuation of the output voltage with load current variation when assuming the input voltage is 6V.

- **Ripple Rejection (PSRR)**
  It is a voltage ratio between the input and the output waveforms when 200 mVp-p AC input is superimposed to the 6.5V input voltage.

- **Standby Current ($I_{STANDBY}$)**
  It is the input current that flows when the output voltage is turned OFF by setting the EN pin.

12. Recommended External Circuits

External Circuit

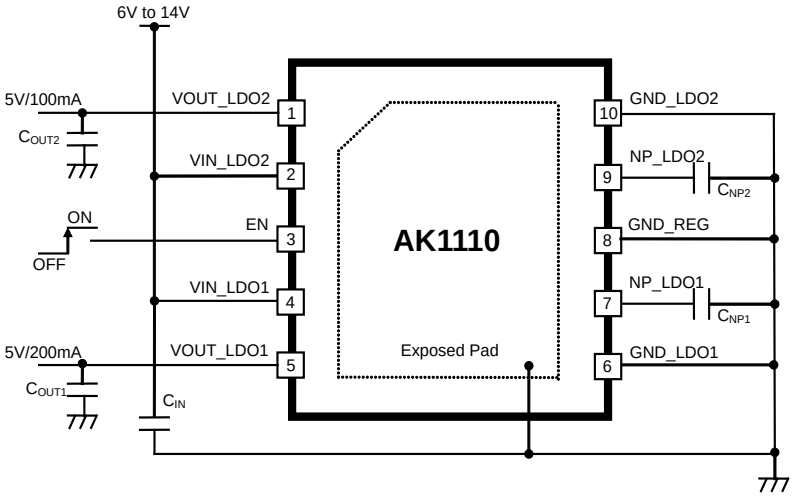


Figure 2927. External Circuit (Top View)

Table 1. Recommended External Parts List

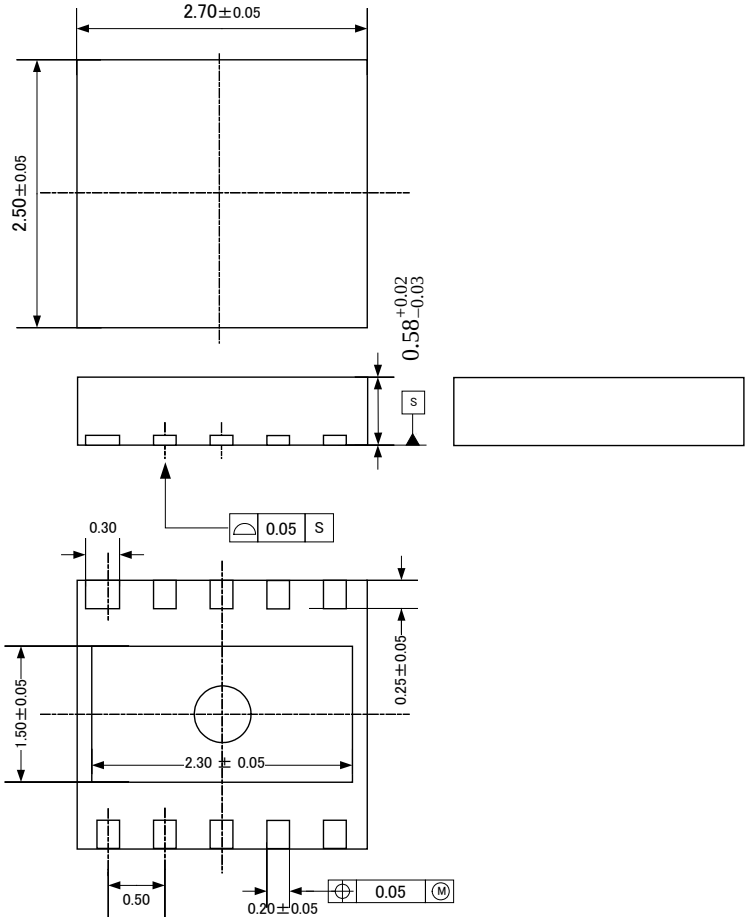
	Symbol	Effective Value	Remarks
Input Capacitor	C_{IN}	1.0μF or higher	
LDO1 Output Capacitor	C_{OUT1}	3.3μF or higher	ESR ≤ 0.1Ω
LDO2 Output Capacitor	C_{OUT2}	3.3μF or higher	ESR ≤ 0.1Ω
LDO1 NP Capacitor	C_{NP1}	3.3μF or higher	
LDO2 NP Capacitor	C_{NP2}	3.3μF or higher	

Note 11. The table above is recommended examples. Please confirm and select optimal values with your system board.

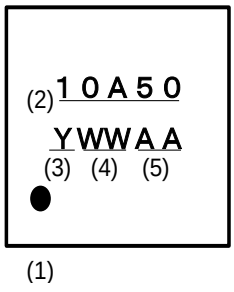
13. Package

■ Outline Dimensions

・PLP10-2725 (Unit: mm)



■ Marking



(1) 1pin Indication
(2) Market No.
(3) Year code (last1digit)
(4) Week code
(5) Management code

14. Ordering Guide

AK1110AEU50	Ta = −40 to 85°C	PLP10-2725

15. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
16/12/26	00	First Edition		

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