# Triple, 200 mA, Low Noise, High PSRR Voltage Regulator

Data Sheet

# ADP322/ADP323

## FEATURES

- Fixed (ADP322) and adjustable output (ADP323) options
- Bias voltage range (VBIAS): 2.5 V to 5.5 V
- LDO input voltage range (VIN1/VIN2, VIN3): 1.8 V to 5.5 V
- Three 200 mA low dropout voltage regulators (LDOs)
- 16-lead, 3 mm × 3 mm LFCSP
- Initial accuracy: ±1%
- Stable with 1 µF ceramic output capacitors
- No noise bypass capacitor required
- 3 independent logic controlled enables
- Overcurrent and thermal protection
- Key specifications
  - High PSRR
    - 76 dB PSRR up to 1 kHz
    - 70 dB PSRR at 10 kHz
    - 60 dB PSRR at 100 kHz
    - 40 dB PSRR at 1 MHz
  - Low output noise
    - 24 µV rms typical output noise at $V_{OUT}$ = 1.2 V
    - 43 µV rms typical output noise at $V_{OUT}$ = 2.8 V
- Excellent transient response
- Low dropout voltage: 110 mV at 200 mA load
- 85 µA typical ground current at no load, all LDOs enabled
- 100 µs fast turn on circuit
- Guaranteed 200 mA output current per regulator
- −40°C to +125°C junction temperature

## APPLICATIONS

- Mobile phones
- Digital cameras and audio devices
- Portable and battery-powered equipment
- Portable medical devices
- Post dc-to-dc regulation

## TYPICAL APPLICATION CIRCUITS

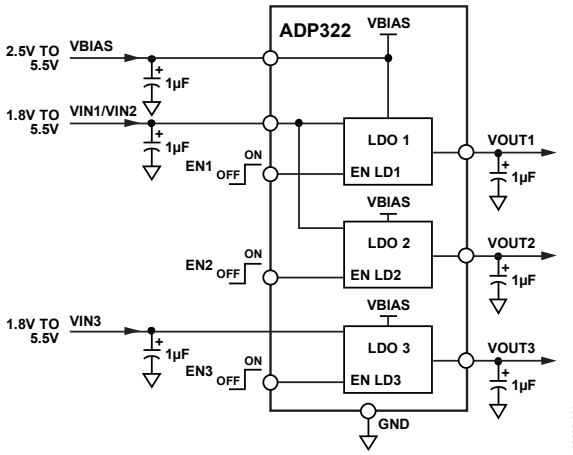


*Figure 1. Typical Application Circuit for ADP322*

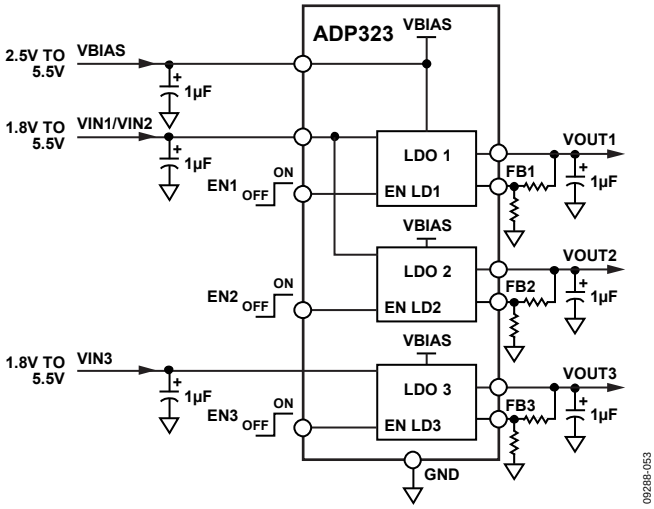


*Figure 2. Typical Application Circuit for ADP323*

## GENERAL DESCRIPTION

The ADP322/ADP323 200 mA triple output LDOs combine high PSRR, low noise, low quiescent current, and low dropout voltage to extend the battery life of portable devices and are ideally suited for wireless applications with demanding performance and board space requirements.

The ADP322/ADP323 PSRR is greater than 60 dB for frequencies as high as 100 kHz while operating with a low headroom voltage. The ADP322/ADP323 offer much lower noise performance than competing LDOs without the need for a noise bypass capacitor.

The ADP322/ADP323 are available in a miniature 16-lead, 3 mm × 3 mm LFCSP package and are stable with tiny 1 µF ±30% ceramic output capacitors providing the smallest possible board area for a wide variety of portable power needs.

The ADP322 is available in output voltage combinations ranging from 0.8 V to 3.3 V and offers overcurrent and thermal protection to prevent damage in adverse conditions. The ADP323 adjustable triple LDO can be configured for any output voltage between 0.5 V and 5 V with two resistors for each output.

Rev. D
Document Feedback


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**9/2010—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{IN1}/V_{IN2} = V_{IN3} = (V_{OUT} + 0.5\ V)$ or 1.8 V (whichever is greater), $V_{BIAS}$ = 2.5 V, EN1, EN2, EN3 = $V_{BIAS}$, $I_{OUT1} = I_{OUT2} = I_{OUT3}$ = 10 mA, $C_{IN} = C_{OUT1} = C_{OUT2} = C_{OUT3}$ = 1 µF, and $T_A$ = 25°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VOLTAGE RANGE | | | | | | |
| Input Bias Voltage Range | $V_{BIAS}$ | $T_J$ = −40°C to +125°C | 2.5 | | 5.5 | V |
| Input LDO Voltage Range | $V_{IN1}/V_{IN2}/V_{IN3}$ | $T_J$ = −40°C to +125°C | 1.8 | | 5.5 | V |
| CURRENT | | | | | | |
| Ground Current with All Regulators On | $I_{GND}$ | $I_{OUT}$ = 0 µA | | 85 | | µA |
| | | $I_{OUT}$ = 0 µA, $T_J$ = −40°C to +125°C | | | 160 | µA |
| | | $I_{OUT}$ = 10 mA | | 120 | | µA |
| | | $I_{OUT}$ = 10 mA, $T_J$ = −40°C to +125°C | | | 220 | µA |
| | | $I_{OUT}$ = 200 mA | | 250 | | µA |
| | | $I_{OUT}$ = 200 mA, $T_J$ = −40°C to +125°C | | | 380 | µA |
| Bias Voltage Input Current | $I_{BIAS}$ | | | 66 | | µA |
| | | $T_J$ = −40°C to +125°C | | | 140 | µA |
| Shutdown Current | $I_{GND-SD}$ | EN1 = EN2 = EN3 = GND | | 0.1 | | µA |
| | | EN1 = EN2 = EN3 = GND, $T_J$ = −40°C to +125°C | | | 2.5 | µA |
| FEEDBACK INPUT CURRENT | $FB_{IN}$ | | | 0.01 | | µA |
| VOLTAGE ACCURACY | | | | | | |
| Output Voltage Accuracy (ADP322) | $V_{OUT}$ | | −1 | | +1 | % |
| | | 100 µA < $I_{OUT}$ < 200 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.5 V, $T_J$ = −40°C to +125°C | −2 | | +2 | % |
| Feedback Voltage Accuracy (ADP323)[1] | $V_{FB}$ | | 0.495 | 0.5 | 0.505 | V |
| | | 100 µA < $I_{OUT}$ < 200 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.5 V, $T_J$ = −40°C to +125°C | 0.490 | | 0.510 | V |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.5 V | | 0.01 | | %/V |
| | | $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.5 V, $T_J$ = −40°C to +125°C | −0.03 | | +0.03 | %/V |
| LOAD REGULATION[2] | $\Delta V_{OUT}/\Delta I_{OUT}$ | $I_{OUT}$ = 1 mA to 200 mA | | 0.001 | | %/mA |
| | | $I_{OUT}$ = 1 mA to 200 mA, $T_J$ = −40°C to +125°C | | | 0.005 | %/mA |
| DROPOUT VOLTAGE[3] | $V_{DROPOUT}$ | $V_{OUT}$ = 3.3 V | | | | mV |
| | | $I_{OUT}$ = 10 mA | | 6 | | mV |
| | | $I_{OUT}$ = 10 mA, $T_J$ = −40°C to +125°C | | | 9 | mV |
| | | $I_{OUT}$ = 200 mA | | 110 | | mV |
| | | $I_{OUT}$ = 200 mA, $T_J$ = −40°C to +125°C | | | 170 | mV |
| START-UP TIME[4] | $T_{START-UP}$ | $V_{OUT}$ = 3.3 V, all $V_{OUT}$ initially off, enable any LDO | | 240 | | µs |
| | | $V_{OUT}$ = 0.8 V | | 100 | | µs |
| | | $V_{OUT}$ = 3.3 V, one $V_{OUT}$ initially on, enable second or third LDO | | 160 | | µs |
| | | $V_{OUT}$ = 0.8 V | | 20 | | µs |
| CURRENT LIMIT THRESHOLD[5] | $I_{LIMIT}$ | | 250 | 360 | 600 | mA |
| THERMAL SHUTDOWN | | | | | | |
| Thermal Shutdown Threshold | $TS_{SD}$ | $T_J$ rising | | 155 | | °C |
| Thermal Shutdown Hysteresis | $TS_{SD-HYS}$ | | | 15 | | °C |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| EN INPUT | | | | | | |
| EN Input Logic High | $V_{IH}$ | 2.5 V ≤ $V_{BIAS}$ ≤ 5.5 V | 1.2 | | | V |
| EN Input Logic Low | $V_{IL}$ | 2.5 V ≤ $V_{BIAS}$ ≤ 5.5 V | | | 0.4 | V |
| EN Input Leakage Current | $V_{I-LEAKAGE}$ | EN1 = EN2 = EN3 = $V_{IN}$ or GND | | 0.1 | | µA |
| | | EN1 = EN2 = EN3 = $V_{IN}$ or GND, $T_J$ = −40°C to +125°C | | | 1 | µA |
| UNDERVOLTAGE LOCKOUT | UVLO | | | | | |
| Input Bias Voltage (VBIAS) Rising | $UVLO_{RISE}$ | | | | 2.45 | V |
| Input Bias Voltage (VBIAS) Falling | $UVLO_{FALL}$ | | 2.0 | | | V |
| Hysteresis | $UVLO_{HYS}$ | | | 180 | | mV |
| OUTPUT NOISE | $OUT_{NOISE}$ | 10 Hz to 100 kHz, $V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V | | 50 | | µV rms |
| | | 10 Hz to 100 kHz, $V_{IN}$ = 5 V, $V_{OUT}$ = 2.8 V | | 43 | | µV rms |
| | | 10 Hz to 100 kHz, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 2.5 V | | 40 | | µV rms |
| | | 10 Hz to 100 kHz, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.2 V | | 24 | | µV rms |
| | | 10 Hz to 100 kHz, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.5 V | | 14 | | µV rms |
| POWER SUPPLY REJECTION RATIO | PSRR | $V_{IN}$ = 1.8 V, $V_{OUT}$ = 0.8 V, $I_{OUT}$ = 100 mA | | | | |
| | | 100 Hz | | 70 | | dB |
| | | 1 kHz | | 70 | | dB |
| | | 10 kHz | | 70 | | dB |
| | | 100 kHz | | 60 | | dB |
| | | 1 MHz | | 40 | | dB |
| | | $V_{IN}$ = 3.3 V, $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 100 mA | | | | |
| | | 100 Hz | | 68 | | dB |
| | | 1 kHz | | 62 | | dB |
| | | 10 kHz | | 68 | | dB |
| | | 100 kHz | | 60 | | dB |
| | | 1 MHz | | 40 | | dB |

[1] Accuracy when VOUTx is connected directly to FBx. When the VOUTx voltage is set by external feedback resistors, the absolute accuracy in adjust mode depends on the tolerances of the resistors used.
[2] Based on an end point calculation using 1 mA and 200 mA loads.
[3] The dropout voltage specification applies only to output voltages greater than 1.8 V. Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage.
[4] Start-up time is defined as the time between the rising edge of ENx to VOUTx being at 90% of its nominal value.
[5] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, that is, 2.7 V.

## INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

**Table 2.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MINIMUM INPUT AND OUTPUT CAPACITANCE[1] | $C_{MIN}$ | $T_A$ = −40°C to +125°C | 0.70 | | | µF |
| CAPACITOR ESR | $R_{ESR}$ | $T_A$ = −40°C to +125°C | 0.001 | | 1 | Ω |

[1] The minimum input and output capacitance must be greater than 0.70 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with LDOs.

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| VIN1/VIN2, VIN3, VBIAS to GND | −0.3 V to +6.5 V |
| VOUT1, VOUT2, FB1, FB2 to GND | −0.3 V to VIN1/VIN2 |
| VOUT3, FB3 to GND | −0.3 V to VIN3 |
| EN1, EN2, EN3 to GND | −0.3 V to +6.5 V |
| Storage Temperature Range | −65°C to +150°C |
| Operating Junction Temperature Range | −40°C to +125°C |
| Soldering Conditions | JEDEC J-STD-020 |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL DATA

Absolute maximum ratings apply individually only, not in combination.

The ADP322/ADP323 triple LDO can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that the junction temperature ($T_J$) is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated. In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits.

The junction temperature ($T_J$) of the device is dependent on the ambient temperature ($T_A$), the power dissipation of the device ($P_D$), and the junction to ambient thermal resistance of the package ($\theta_{JA}$). Maximum junction temperature ($T_J$) is calculated from the ambient temperature ($T_A$) and power dissipation ($P_D$) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction to ambient thermal resistance ($\theta_{JA}$) of the package is based on modeling and calculation using a 4-layer board. The junction to ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of $\theta_{JA}$ can vary, depending on PCB material, layout, and environmental conditions. The specified values of $\theta_{JA}$ are based on a 4-layer, 4 inch × 3 inch circuit board. See JEDEC JESD 51-9 for detailed information on the board construction. For additional information, see the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*.

$\Psi_{JB}$ is the junction to board thermal characterization parameter with units of °C/W. $\Psi_{JB}$ of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. $\Psi_{JB}$ measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, $\theta_{JB}$. Therefore, $\Psi_{JB}$ thermal paths include convection from the top of the package as well as radiation from the package, factors that make $\Psi_{JB}$ more useful in real-world applications. Maximum junction temperature ($T_J$) is calculated from the board temperature ($T_B$) and power dissipation ($P_D$) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JEDEC JESD51-8 and JESD51-12 for more detailed information about $\Psi_{JB}$.

## THERMAL RESISTANCE

$\theta_{JA}$ and $\Psi_{JB}$ are specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 4.**

| Package Type | $\theta_{JA}$ | $\Psi_{JB}$ | Unit |
|---|---|---|---|
| 16-Lead, 3 mm × 3 mm LFCSP | 49.5 | 25.2 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

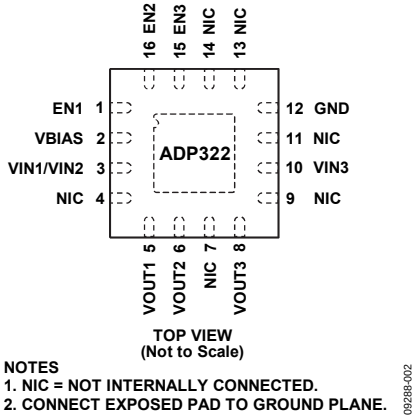


*Figure 3. ADP322 Pin Configuration*

**Table 5. ADP322 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | EN1 | Enable Input for Regulator 1. Drive EN1 high to turn on Regulator 1; drive it low to turn off Regulator 1. For automatic startup, connect EN1 to VBIAS. |
| 2 | VBIAS | Input Voltage Bias Supply. Bypass VBIAS to GND with a 1 µF or greater capacitor. |
| 3 | VIN1/VIN2 | Regulator Input Supply for Output Voltage 1 and Output Voltage 2. Bypass VIN1/VIN2 to GND with a 1 µF or greater capacitor. |
| 4 | NIC | Not Internally Connected. This pin is not connected internally. |
| 5 | VOUT1 | Regulated Output Voltage 1. Connect a 1 µF or greater output capacitor between VOUT1 and GND. |
| 6 | VOUT2 | Regulated Output Voltage 2. Connect a 1 µF or greater output capacitor between VOUT2 and GND. |
| 7 | NIC | Not Internally Connected. This pin is not connected internally. |
| 8 | VOUT3 | Regulated Output Voltage 3. Connect a 1 µF or greater output capacitor between VOUT3 and GND. |
| 9 | NIC | Not Internally Connected. This pin is not connected internally. |
| 10 | VIN3 | Regulator Input Supply for Output Voltage 3. Bypass VIN3 to GND with a 1 µF or greater capacitor. |
| 11 | NIC | Not Internally Connected. This pin is not connected internally. |
| 12 | GND | Ground Pin. |
| 13 | NIC | Not Internally Connected. This pin is not connected internally. |
| 14 | NIC | Not Internally Connected. This pin is not connected internally. |
| 15 | EN3 | Enable Input for Regulator 3. Drive EN3 high to turn on Regulator 3; drive it low to turn off Regulator 3. For automatic startup, connect EN3 to VBIAS. |
| 16 | EN2 | Enable Input for Regulator 2. Drive EN3 high to turn on Regulator 2; drive it low to turn off Regulator 2. For automatic startup, connect EN2 to VBIAS. |
| | EP | Exposed pad for enhanced thermal performance. Connect to copper ground plane. |

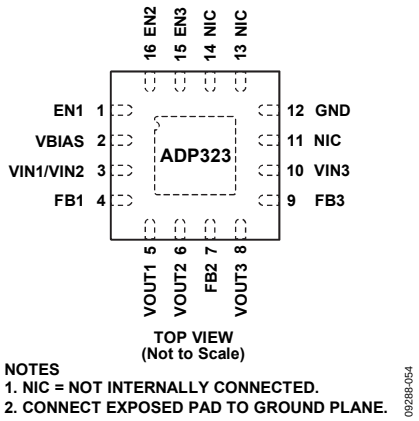


*Figure 4. ADP323 Pin Configuration*

**Table 6. ADP323 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | EN1 | Enable Input for Regulator 1. Drive EN1 high to turn on Regulator 1; drive it low to turn off Regulator 1. For automatic startup, connect EN1 to VBIAS. |
| 2 | VBIAS | Input Voltage Bias Supply. Bypass VBIAS to GND with a 1 µF or greater capacitor. |
| 3 | VIN1/VIN2 | Regulator Input Supply for Output Voltage 1 and Output Voltage 2. Bypass VIN1/VIN2 to GND with a 1 µF or greater capacitor. |
| 4 | FB1 | Connect the midpoint of the voltage divider from VOUT1 to GND to set VOUT1. |
| 5 | VOUT1 | Regulated Output Voltage 1. Connect a 1 µF or greater output capacitor between VOUT1 and GND. |
| 6 | VOUT2 | Regulated Output Voltage 2. Connect a 1 µF or greater output capacitor between VOUT2 and GND. |
| 7 | FB2 | Connect the midpoint of the voltage divider from VOUT2 to GND to set VOUT2. |
| 8 | VOUT3 | Regulated Output Voltage 3. Connect a 1 µF or greater output capacitor between VOUT3 and GND. |
| 9 | FB3 | Connect the midpoint of the voltage divider from VOUT3 to GND to set VOUT3. |
| 10 | VIN3 | Regulator Input Supply for Output Voltage 3. Bypass VIN3 to GND with a 1 µF or greater capacitor. |
| 11 | NIC | Not Internally Connected. This pin is not connected internally. |
| 12 | GND | Ground Pin. |
| 13 | NIC | Not Internally Connected. This pin is not connected internally. |
| 14 | NIC | Not Internally Connected. This pin is not connected internally. |
| 15 | EN3 | Enable Input for Regulator 3. Drive EN3 high to turn on Regulator 3; drive it low to turn off Regulator 3. For automatic startup, connect EN3 to VBIAS. |
| 16 | EN2 | Enable Input for Regulator 2. Drive EN3 high to turn on Regulator 2; drive it low to turn off Regulator 2. For automatic startup, connect EN2 to VBIAS. |
| | EP | Exposed pad for enhanced thermal performance. Connect to copper ground plane. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN1}/V_{IN2} = V_{IN3} = V_{BIAS} = 4$ V, $V_{OUT1} = 3.3$ V, $V_{OUT2} = 1.8$ V, $V_{OUT3} = 1.5$ V, $I_{OUT} = 10$ mA, $C_{IN} = C_{OUT1} = C_{OUT2} = C_{OUT3} = 1$ µF, $V_{ENX}$ is the enable voltage, $T_A = 25°C$, unless otherwise noted.

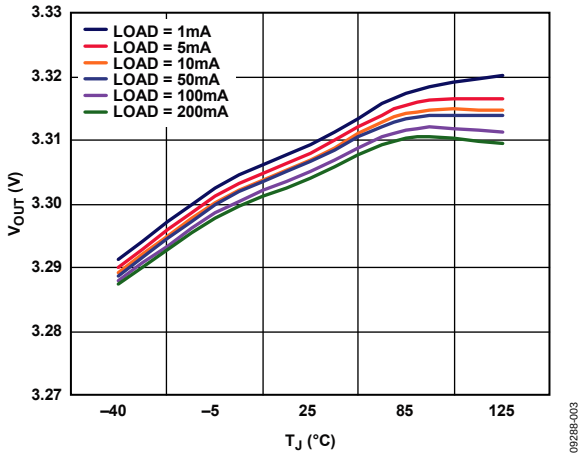


Figure 5. Output Voltage vs. Junction Temperature, $V_{RIPPLE} = 50$ mV, $C_{OUT} = 1$ µF

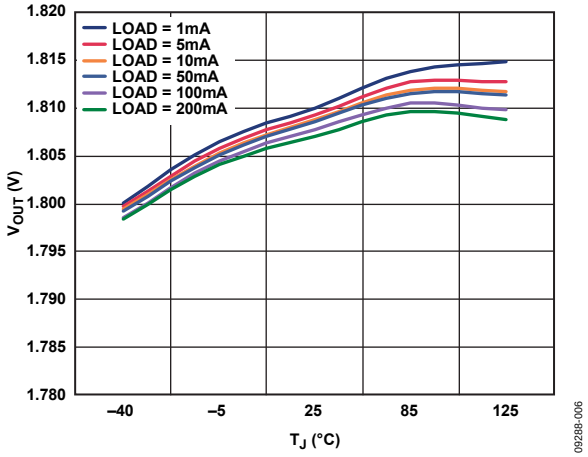


Figure 8. Output Voltage vs. Junction Temperature, $V_{RIPPLE} = 50$ mV, $C_{OUT} = 1$ µF

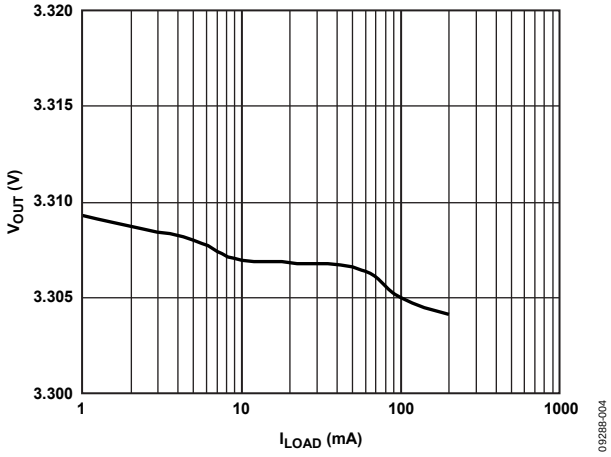


Figure 6. Output Voltage vs. Load Current, $V_{RIPPLE} = 50$ mV, $C_{OUT} = 1$ µF

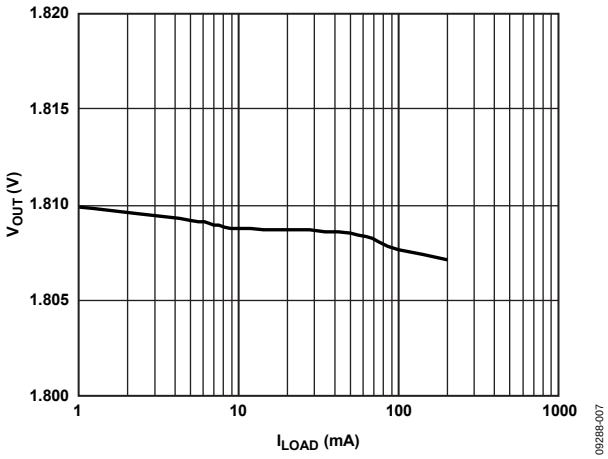


Figure 9. Output Voltage vs. Load Current, $V_{RIPPLE} = 50$ mV, $C_{OUT} = 1$ µF

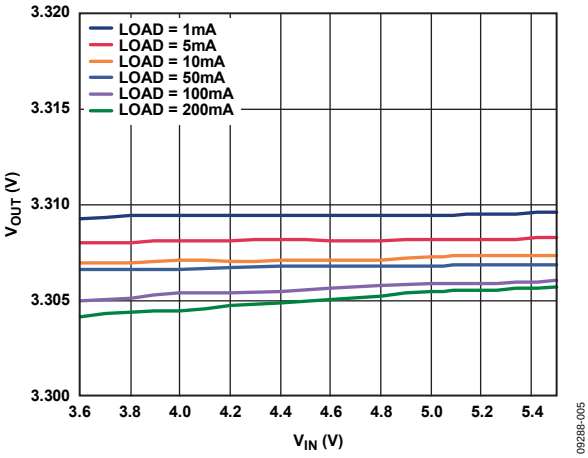


Figure 7. Output Voltage vs. Input Voltage, $V_{RIPPLE} = 50$ mV, $C_{OUT} = 1$ µF

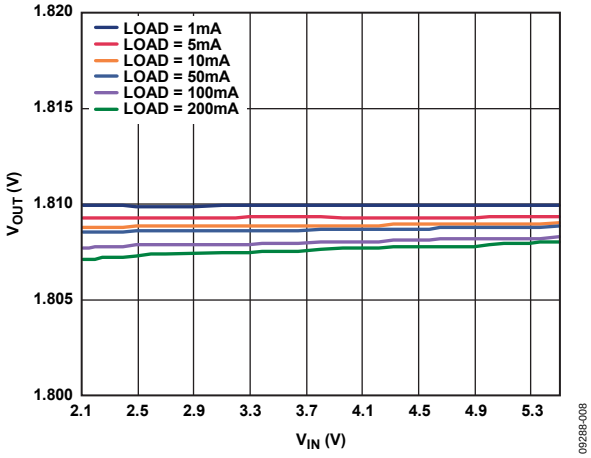


Figure 10. Output Voltage vs. Input Voltage, $V_{RIPPLE} = 50$ mV, $C_{OUT} = 1$ µF

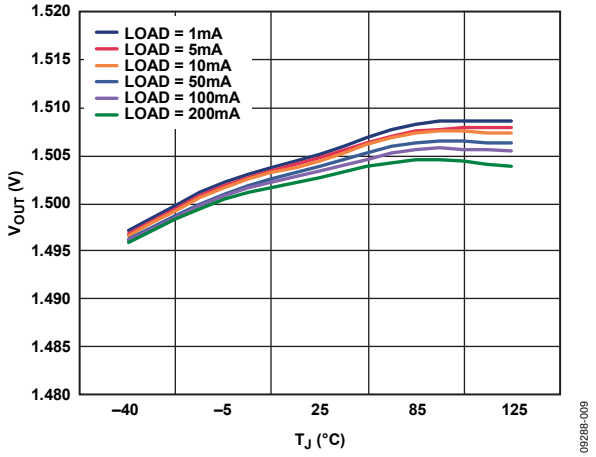


Figure 11. Output Voltage vs. Junction Temperature, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

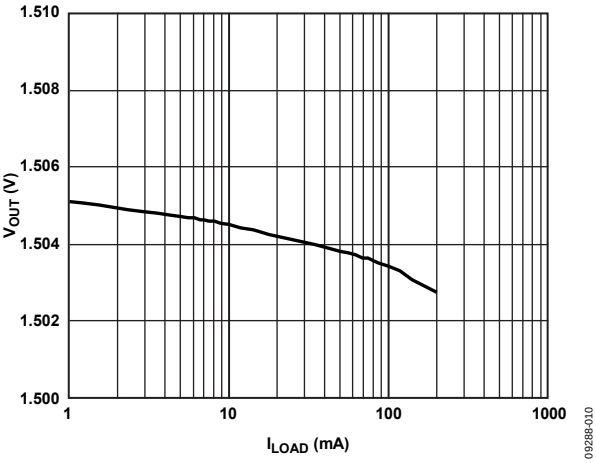


Figure 12. Output Voltage vs. Load Current, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

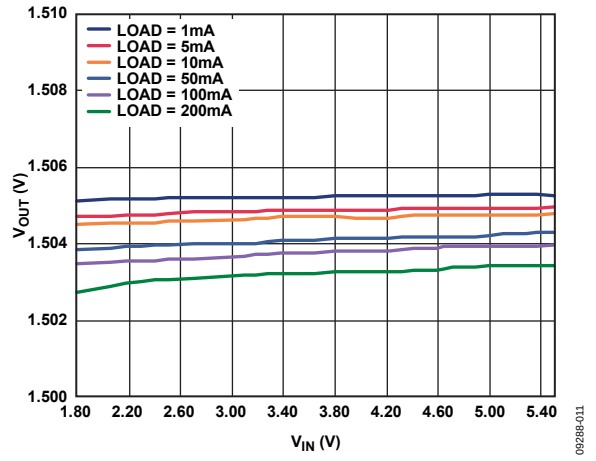


Figure 13. Output Voltage vs. Input Voltage, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

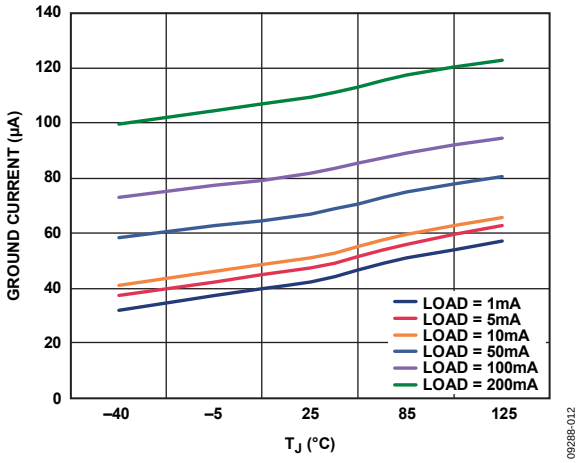


Figure 14. Ground Current vs. Junction Temperature, Single Output Loaded, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

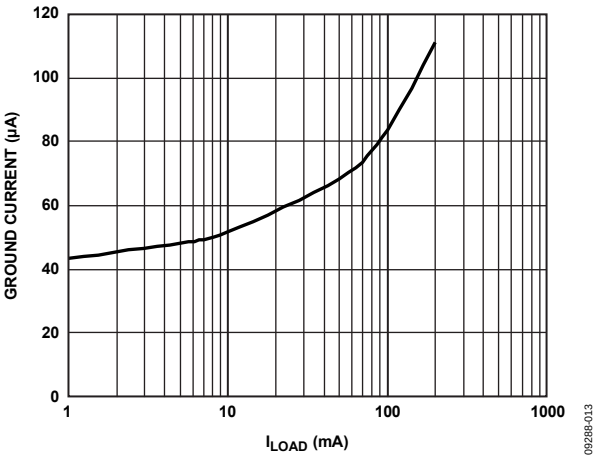


Figure 15. Ground Current vs. Load Current, Single Output Loaded, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

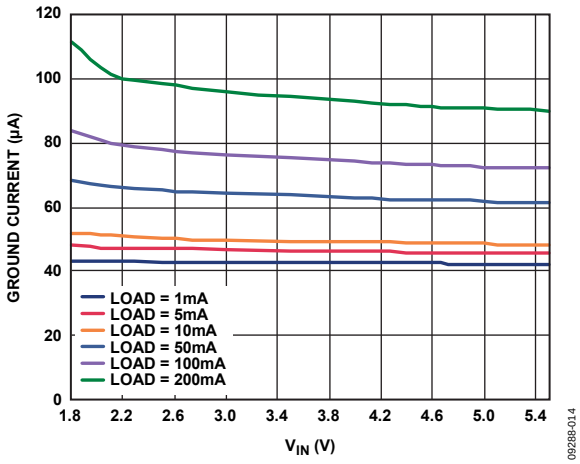


Figure 16. Ground Current vs. Input Voltage, Single Output Loaded, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

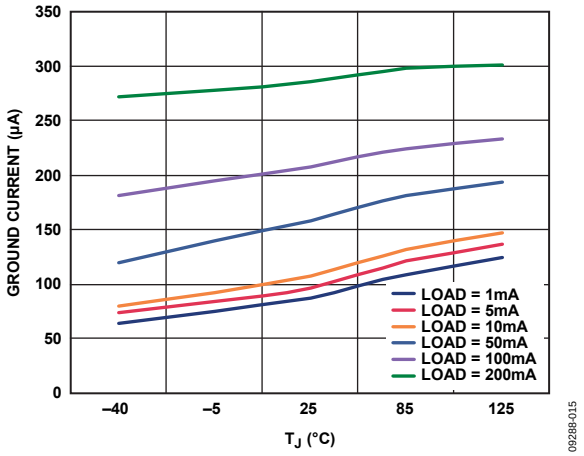


*Figure 17. Ground Current vs. Junction Temperature, All Outputs Loaded Equally, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

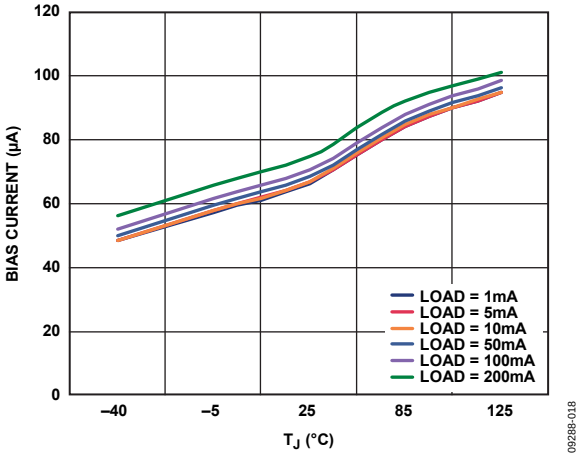


*Figure 20. Bias Current vs. Junction Temperature, Single Output Loaded, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

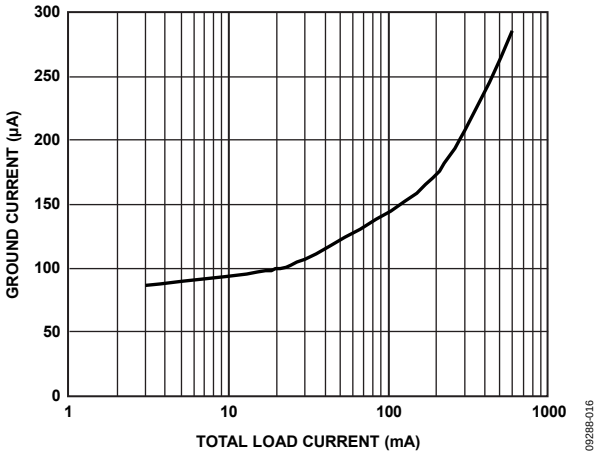


*Figure 18. Ground Current vs. Load Current, All Outputs Loaded Equally, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

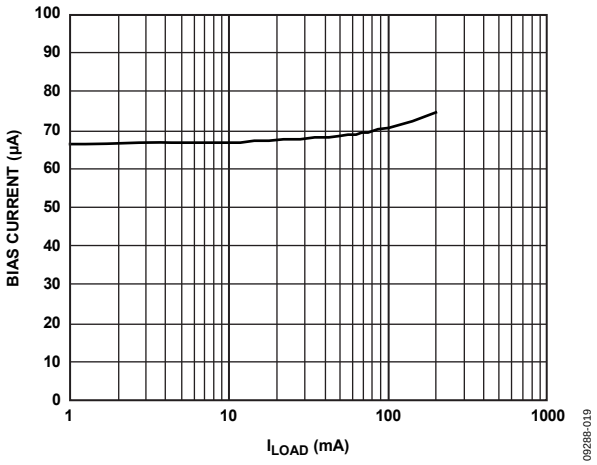


*Figure 21. Bias Current vs. Load Current, Single Output Loaded, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

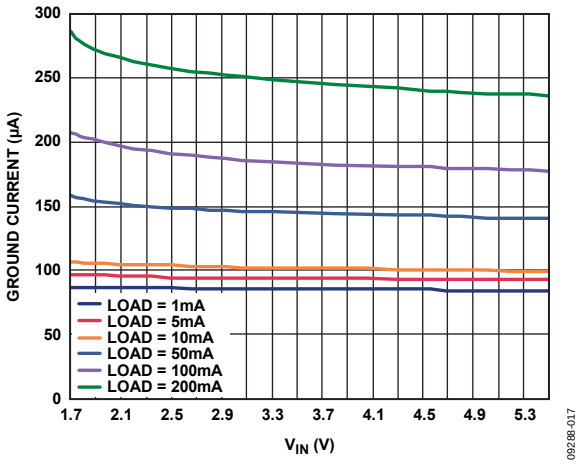


*Figure 19. Ground Current vs. Input Voltage, All Outputs Loaded Equally, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

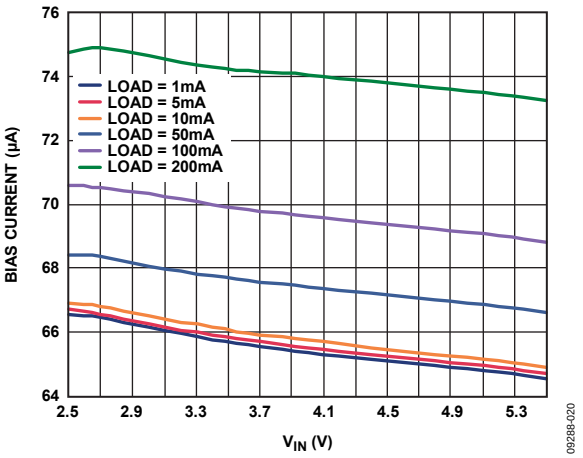


*Figure 22. Bias Current vs. Input Voltage, Single Output Loaded, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

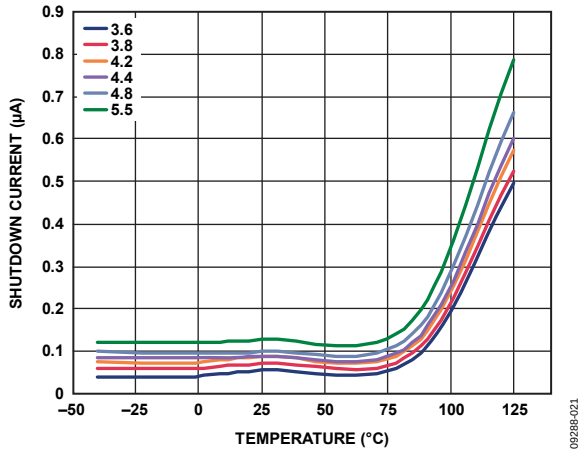


Figure 23. Shutdown Current vs. Temperature at Various Input Voltages, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

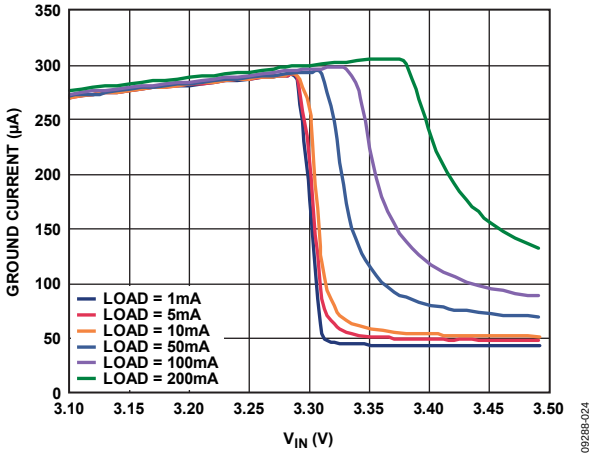


Figure 26. Ground Current vs. Input Voltage (in Dropout), $V_{OUT1}$ = 3.3 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

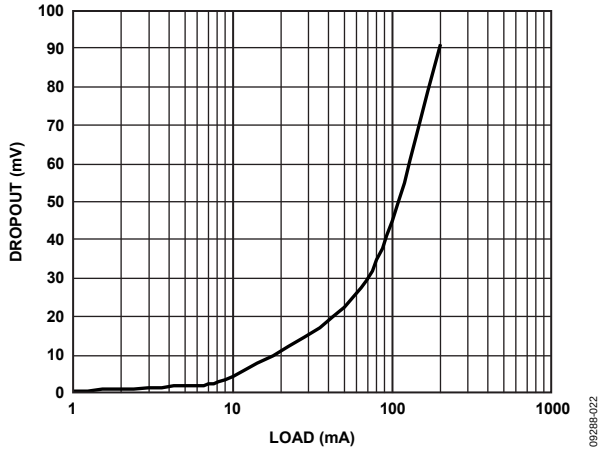


Figure 24. Dropout Voltage vs. Load Current and Output Voltage, $V_{OUT1}$ = 3.3 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

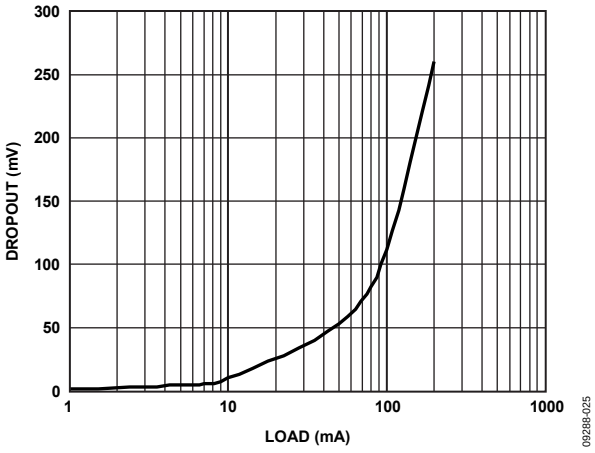


Figure 27. Dropout Voltage vs. Load Current and Output Voltage, $V_{OUT2}$ = 1.8 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

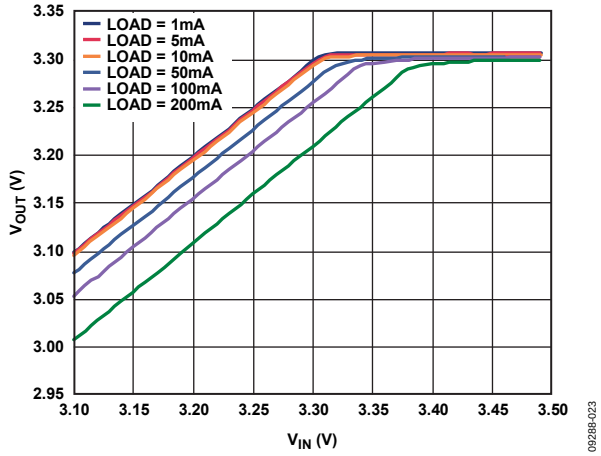


Figure 25. Output Voltage vs. Input Voltage (in Dropout), $V_{OUT1}$ = 3.3 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

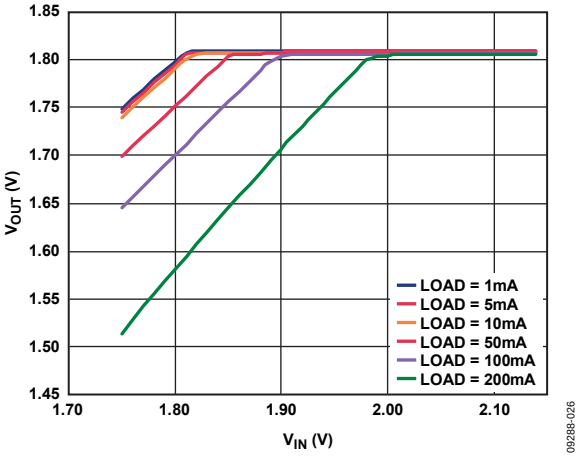


Figure 28. Output Voltage vs. Input Voltage (in Dropout), $V_{OUT2}$ = 1.8 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

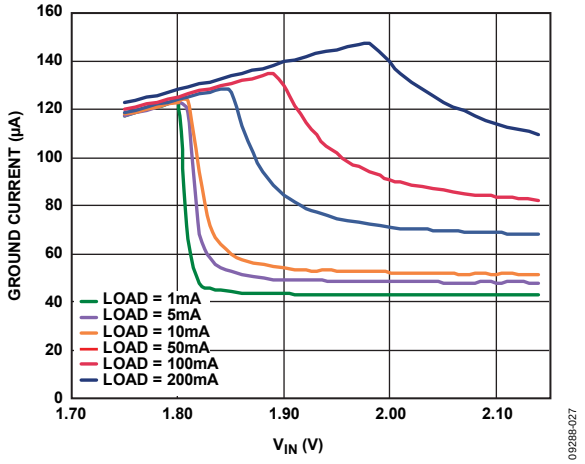


Figure 29. Ground Current vs. Input Voltage (in Dropout), $V_{OUT2}$ = 1.8 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

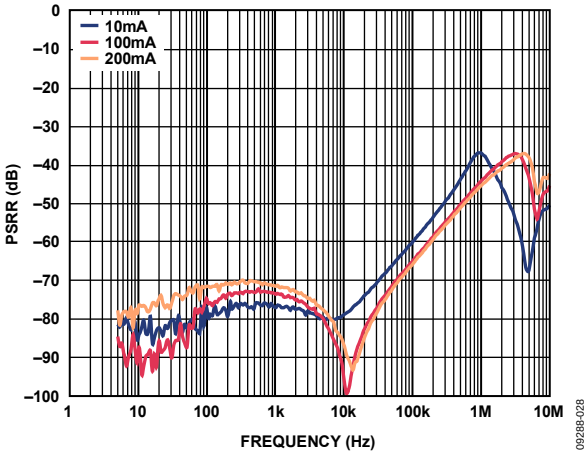


Figure 30. Power Supply Rejection Ratio vs. Frequency, $V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.8 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

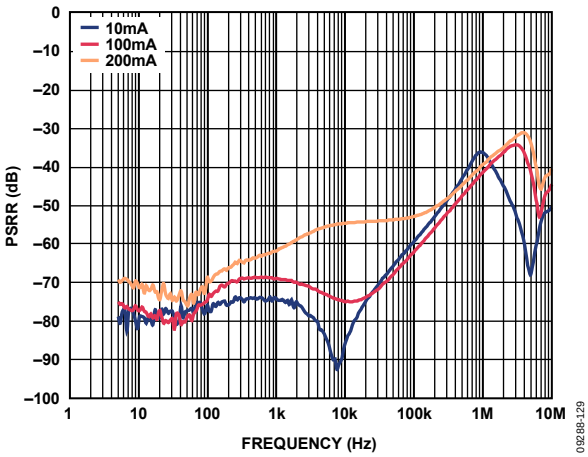


Figure 31. Power Supply Rejection Ratio vs. Frequency, $V_{OUT}$ = 1.8 V, $V_{IN}$ = 2.3 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

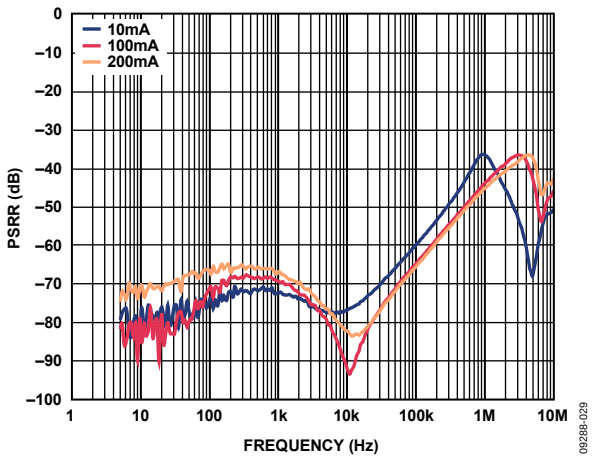


Figure 32. Power Supply Rejection Ratio vs. Frequency, $V_{OUT}$ = 3.3 V, $V_{IN}$ = 4.3 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

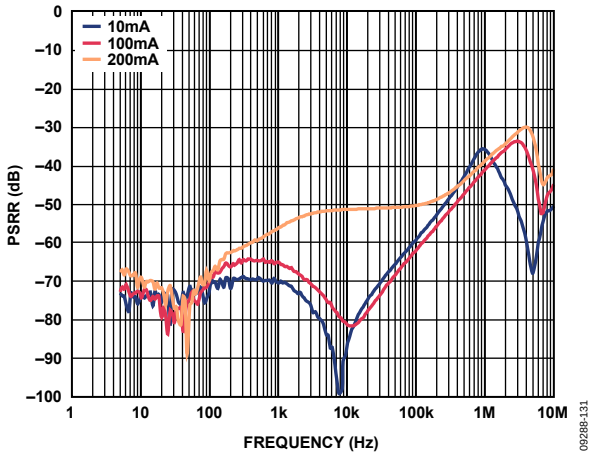


Figure 33. Power Supply Rejection Ratio vs. Frequency, $V_{OUT}$ = 3.3 V, $V_{IN}$ = 3.8 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

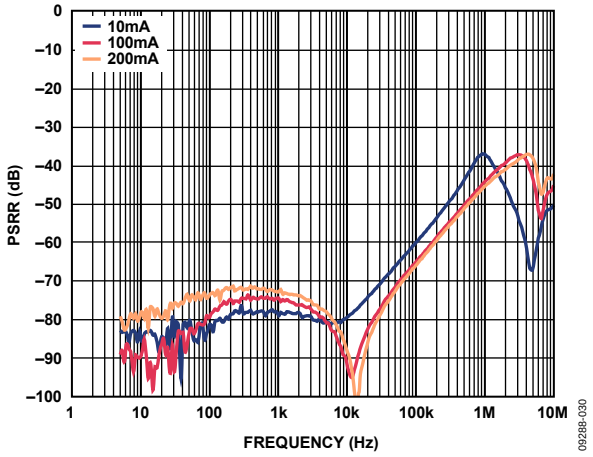


Figure 34. Power Supply Rejection Ratio vs. Frequency, $V_{OUT}$ = 1.5 V, $V_{IN}$ = 2.5 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

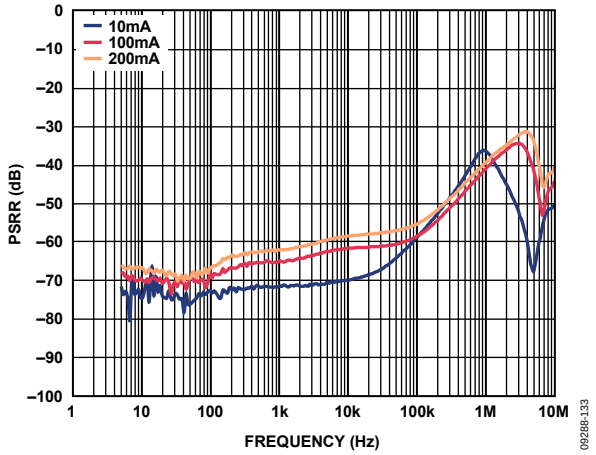


Figure 35. Power Supply Rejection Ratio vs. Frequency, $V_{OUT}$ = 1.5 V, $V_{IN}$ = 2.0 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

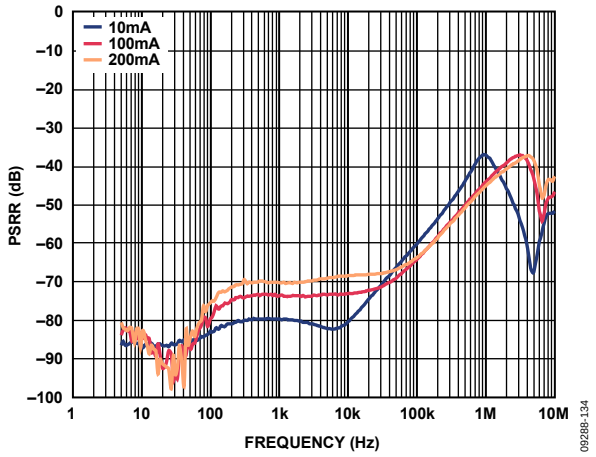


Figure 36. Power Supply Rejection Ratio vs. Frequency, $V_{OUT}$ = 1.2 V, $V_{IN}$ = 2.2 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

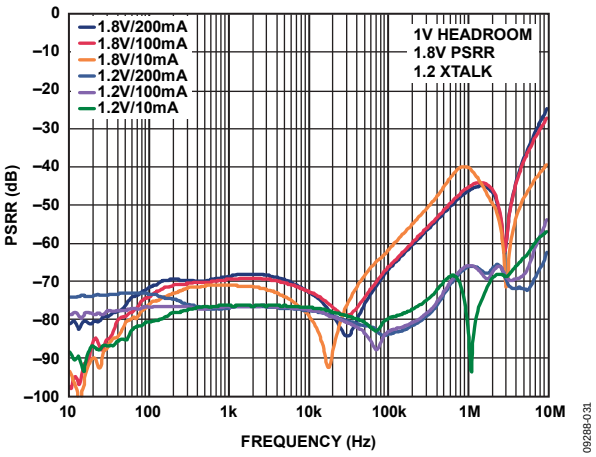


Figure 37. Power Supply Rejection Ratio vs. Frequency, Channel to Channel Crosstalk, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

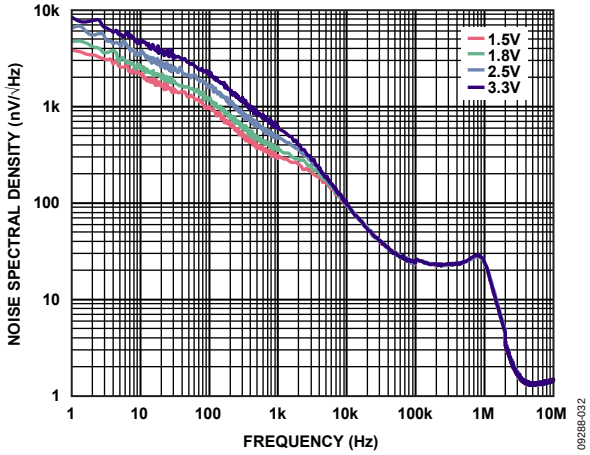


Figure 38. Output Noise Spectral Density, $V_{IN}$ = 5 V, $I_{LOAD}$ = 10 mA, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

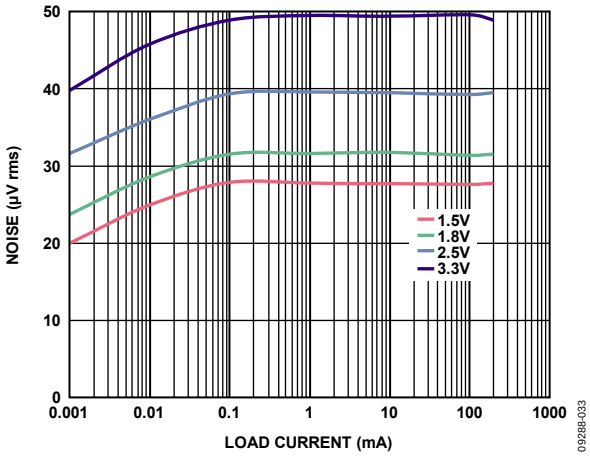


Figure 39. 10 Hz to 100 kHz Output Noise vs. Load Current and Output Voltage, $V_{IN}$ = 5 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

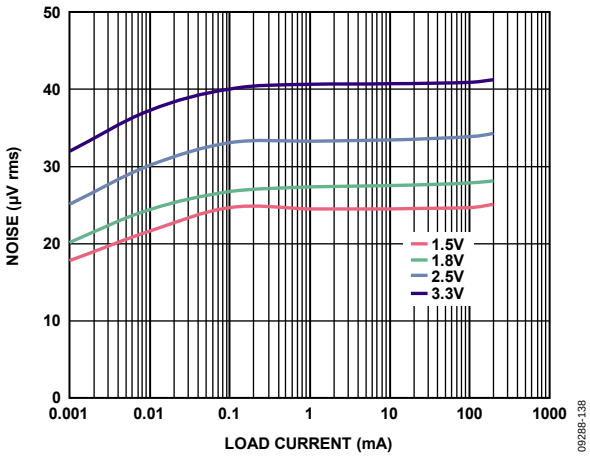


Figure 40. 100 Hz to 100 kHz Output Noise vs. Load Current and Output Voltage, $V_{IN}$ = 5 V, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF

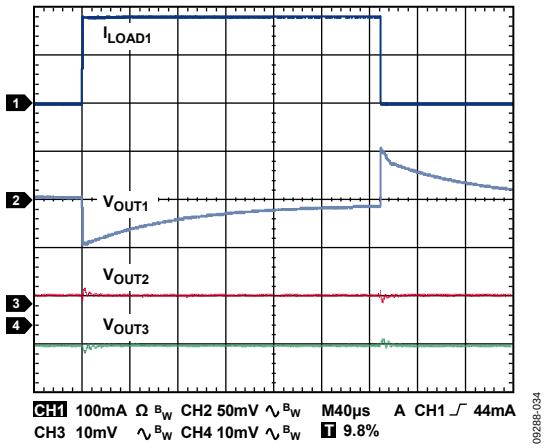


*Figure 41. Load Transient Response, $I_{LOAD1}$ = 1 mA to 200 mA, $I_{LOAD2} = I_{LOAD3}$ = 1 mA, CH1 = $I_{LOAD1}$, CH2 = $V_{OUT1}$, CH3 = $V_{OUT2}$, CH4 = $V_{OUT3}$, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

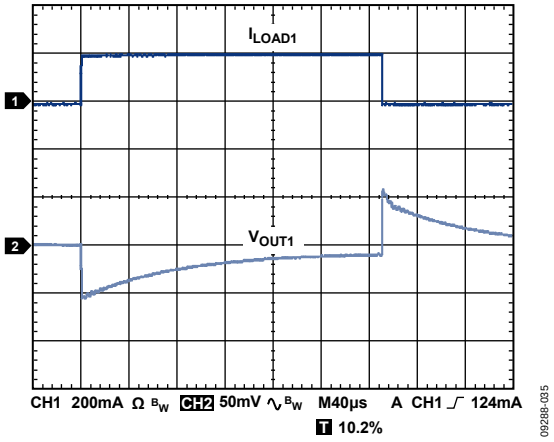


*Figure 42. Load Transient Response, $I_{LOAD1}$ = 1 mA to 200 mA, $C_{OUT1}$ = 1 µF, CH1 = $I_{LOAD1}$, CH2 = $V_{OUT1}$, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

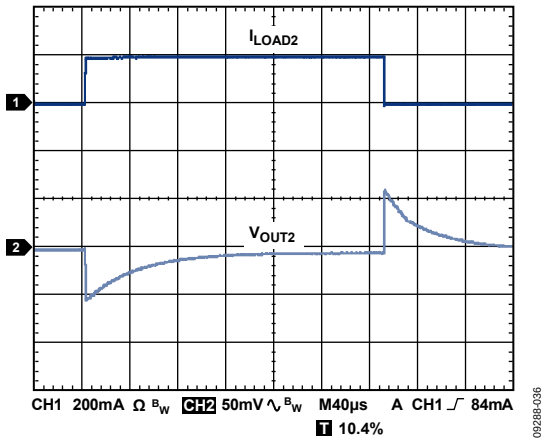


*Figure 43. Load Transient Response, $I_{LOAD2}$ = 1 mA to 200 mA, $C_{OUT2}$ = 1 µF, CH1 = $I_{LOAD2}$, CH2 = $V_{OUT2}$, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

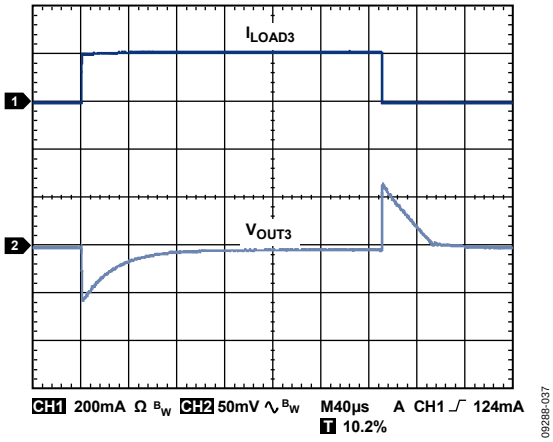


*Figure 44. Load Transient Response, $I_{LOAD3}$ = 1 mA to 200 mA, $C_{OUT3}$ = 1 µF, CH1 = $I_{LOAD3}$, CH2 = $V_{OUT3}$, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

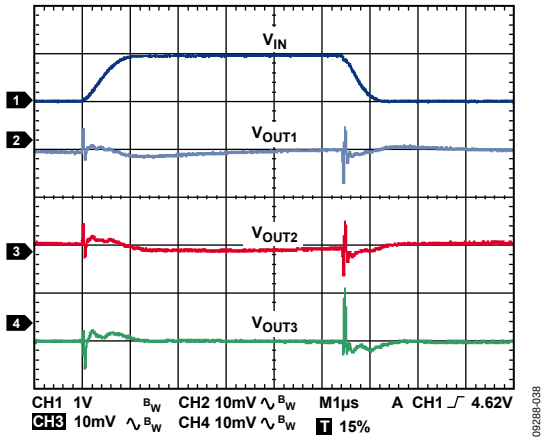


*Figure 45. Line Transient Response, $V_{IN}$ = 4 V to 5 V, $I_{LOAD1} = I_{LOAD2} = I_{LOAD3}$ =100 mA, CH1 = $V_{IN}$, CH2 = $V_{OUT1}$, CH3 = $V_{OUT2}$, CH4 = $V_{OUT3}$, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

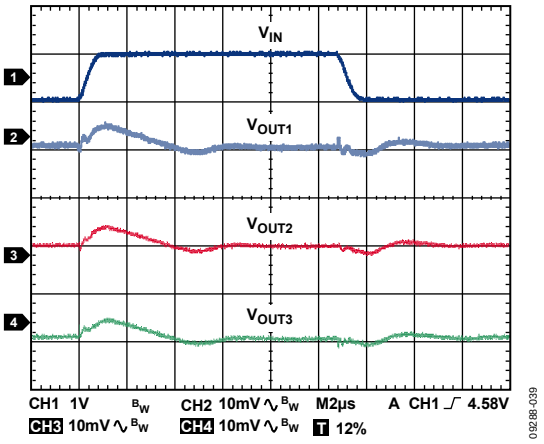


*Figure 46. Line Transient Response, $V_{IN}$ = 4 V to 5 V, $I_{LOAD1} = I_{LOAD2} = I_{LOAD3}$ =1 mA, CH1 = $V_{IN}$, CH2 = $V_{OUT1}$, CH3 = $V_{OUT2}$, CH4 = $V_{OUT3}$, $V_{RIPPLE}$ = 50 mV, $C_{OUT}$ = 1 µF*

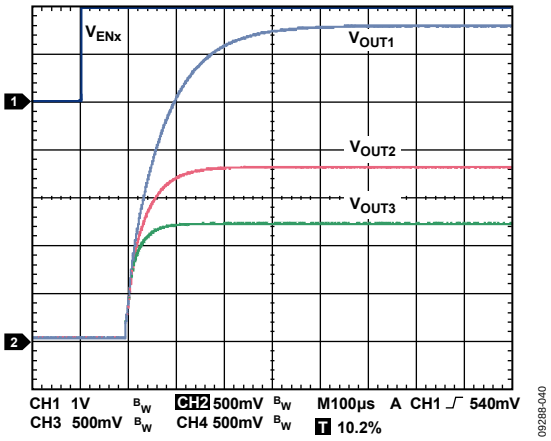


*Figure 47. Turn On Response, $I_{LOAD1} = I_{LOAD2} = I_{LOAD3} = 100$ mA, CH1 = $V_{ENx}$ (the Enable Voltage), CH2 = $V_{OUT1}$, CH3 = $V_{OUT2}$, CH4 = $V_{OUT3}$, $V_{RIPPLE} = 50$ mV, $C_{OUT} = 1$ µF*

# THEORY OF OPERATION

The ADP322/ADP323 triple LDO are low quiescent current, LDOs that operate from 1.8 V to 5.5 V on VIN1/VIN2 and VIN3 and provide up to 200 mA of current from each output. Drawing a low 250 µA quiescent current (typical) at full load makes the ADP322/ADP323 ideal for battery operated portable equipment. Shutdown current consumption is typically 100 nA. Optimized for use with small 1 µF ceramic capacitors, the ADP322/ADP323 provide excellent transient performance.

Internally, the ADP322 consists of a reference, three error amplifiers, three feedback voltage dividers, and three PMOS pass transistors. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

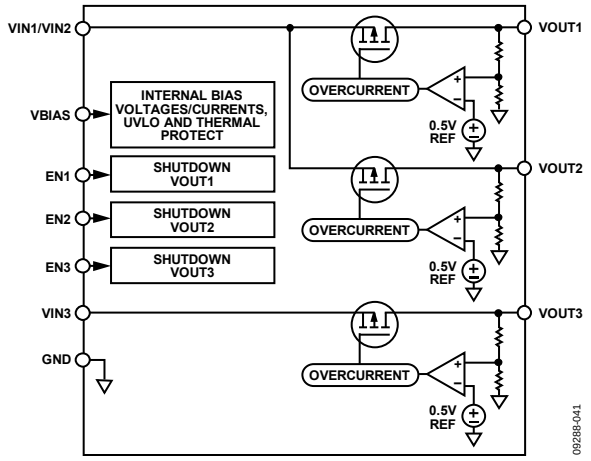


*Figure 48. ADP322 Internal Block Diagram*

The ADP323 differs from the ADP322 except in that the output voltage dividers are internally disconnected and the feedback inputs of the error amplifiers are brought out for each output.

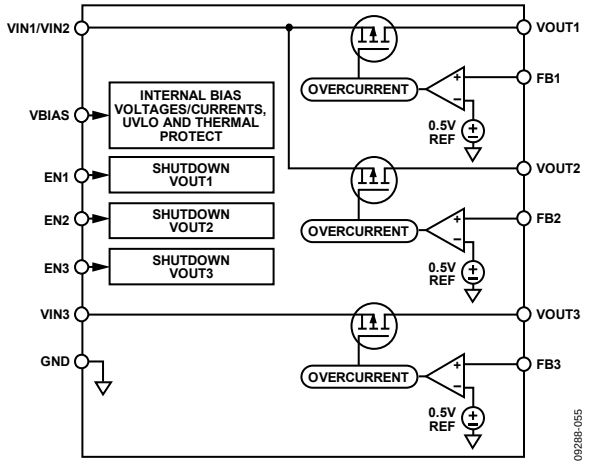


*Figure 49. ADP323 Internal Block Diagram*

The output voltage can be set using the following formulas:

$$V_{OUT} = 0.5\ V(1 + R1/R2) + (FB_{IN})(R1)$$

$$V_{OUT2} = 0.5\ V(1 + R3/R4) + (FB_{IN})(R3)$$

$$V_{OUT3} = 0.5\ V(1 + R5/R6) + (FB_{IN})(R5)$$

The value of R1, R3, R5 must be less than 200 kΩ to minimize errors in the output voltage caused by the FBx pin input current. For example, when R1 and R2 each equal 200 kΩ, the output voltage is 1.0 V. The output voltage error introduced by the FBx pin input current is 2 mV or 0.20%, assuming a typical FBx pin input current of 10 nA at 25°C.

The ADP322 is available in multiple output voltage options ranging from 0.8 V to 3.3 V.

The ADP322/ADP323 use the EN1/EN2 and EN3 pins to enable and disable the VOUT1/VOUT2/VOUT3 pins under normal operating conditions. When the EN1/EN2 and EN3 pins are high, VOUT1/VOUT2/VOUT3 turn on; when the EN1/EN2 and EN3 pins are low, VOUT1/VOUT2/VOUT3 turn off. For automatic startup, the EN1/EN2 and EN3 pins can be tied to VBIAS.

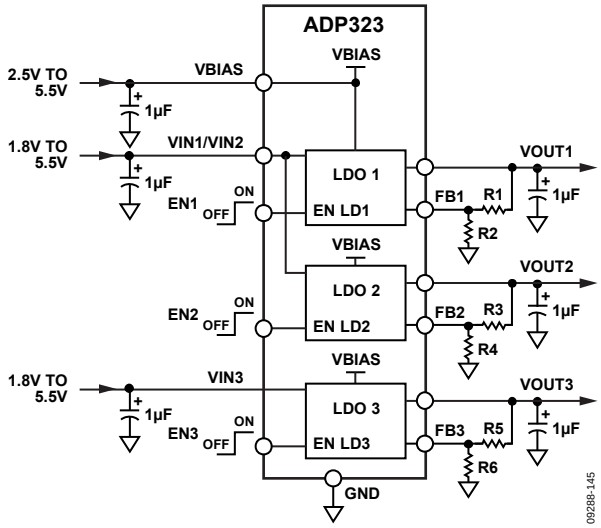


*Figure 50. ADP323 Application Circuit Diagram*

# APPLICATIONS INFORMATION

## ADIsimPOWER DESIGN TOOL

The ADP323 is supported by the ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count, taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about, and to obtain ADIsimPower design tools, visit www.analog.com/ADIsimPower.

## CAPACITOR SELECTION

### *Output Capacitor*

The ADP322/ADP323 are designed for operation with small, space-saving ceramic capacitors, but the devices function with most commonly used capacitors as long as care is taken with the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure the stability of the ADP322/ADP323.

Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP322/ADP323 to large changes in the load current. Figure 51 shows the transient response for an output capacitance value of 1 µF.

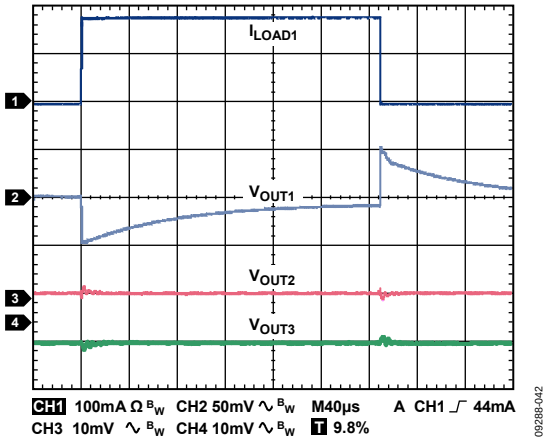


*Figure 51. Output Transient Response, $I_{LOAD1}$ = 1 mA to 200 mA, $I_{LOAD2}$ = 1 mA, $I_{LOAD3}$ = 1 mA, CH1 = $I_{LOAD1}$, CH2 = $V_{OUT1}$, CH3 = $V_{OUT2}$, CH4 = $V_{OUT3}$*

### *Input Bypass Capacitor*

Connecting a 1 µF capacitor from VIN1/VIN2, VIN3, and VBIAS to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance is encountered. If an output capacitance greater than 1 µF is required, the input capacitor can be increased to match it.

### *Input and Output Capacitor Properties*

Any good quality ceramic capacitor can be used with the ADP322/ADP323, as long as the capacitor meets the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have an adequate dielectric to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended due to their poor temperature and dc bias characteristics.

Figure 52 depicts the capacitance vs. voltage bias characteristic of a 0402 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of the package or voltage rating.

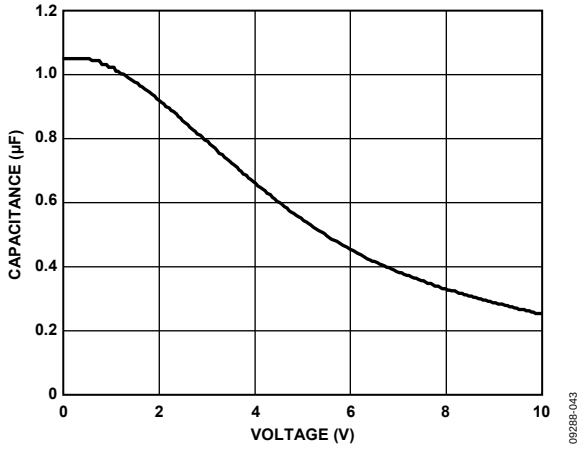


*Figure 52. Capacitance vs. Voltage Bias Characteristic*

Use Equation 1 to determine the worst case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
$C_{BIAS}$ is the effective capacitance at the operating voltage.
*TEMPCO* is the worst case capacitor temperature coefficient.
*TOL* is the worst case component tolerance.

In this example, TEMPCO over −40°C to +85°C is assumed to be 15% for an X5R dielectric. TOL is assumed to be 10%, and $C_{BIAS}$ is 0.94 µF at 1.8 V (from the graph in Figure 52).

Substituting these values into Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP322/ADP323 triple LDO, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

## UNDERVOLTAGE LOCKOUT

The ADP322/ADP323 have an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage bias, VBIAS, is less than approximately 2.2 V. This ensures that the inputs of the ADP322/ADP323 and the output behave in a predictable manner during power-up.

## ENABLE FEATURE

The ADP322/ADP323 use the ENx pins to enable and disable the VOUTx pins under normal operating conditions. Figure 53 shows that, when a rising voltage on ENx crosses the active threshold, VOUTx turns on. When a falling voltage on ENx crosses the inactive threshold, VOUTx turns off.

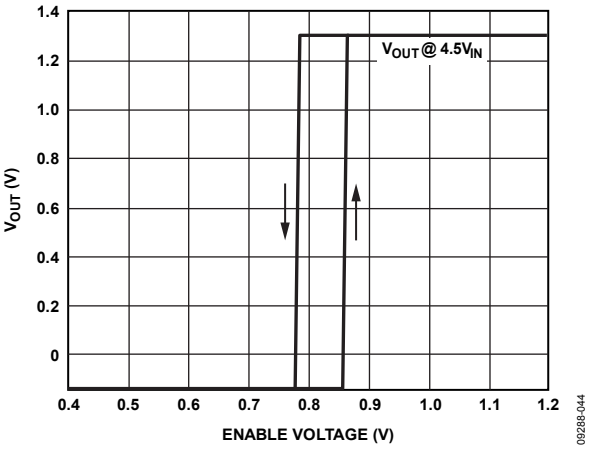


*Figure 53. Typical ENx Pin Operation*

As shown in Figure 53, the ENx pin has built in hysteresis. This prevents on/off oscillations that can occur due to noise on the ENx pin as it passes through the threshold points.

The active/inactive thresholds of the ENx pin are derived from the $V_{BIAS}$ voltage. Therefore, these thresholds vary with changing input voltage. Figure 54 shows typical ENx active/ inactive thresholds when the input voltage varies from 2.5 V to 5.5 V (note that $V_{ENx}$ is the enable voltage).

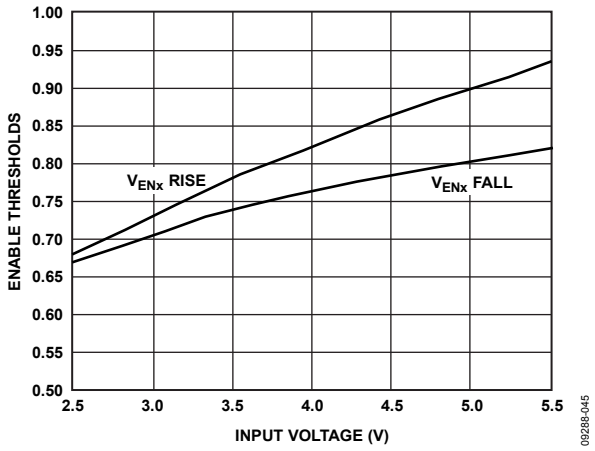


*Figure 54. Typical ENx Pins Thresholds vs. Input Voltage*

The ADP322/ADP323 use an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 2.8 V option is approximately 220 µs from the time the ENx active threshold is crossed to when the output reaches 90% of its final value. The start-up time is somewhat dependent on the output voltage setting and increases slightly as the output voltage increases.

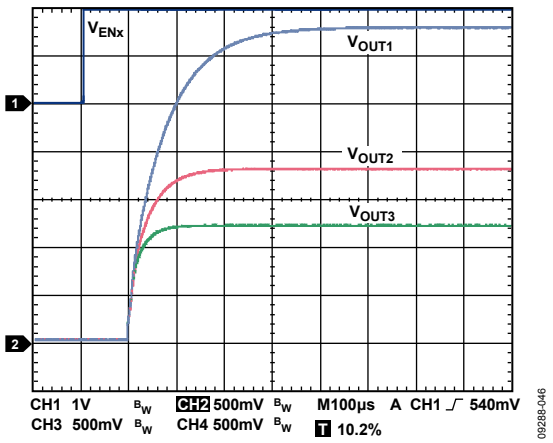


*Figure 55. Typical Start-Up Time, $I_{LOAD1} = I_{LOAD2} = I_{LOAD3} = 100$ mA, CH1 = $V_{ENx}$ (the Enable Voltage), CH2 = $V_{OUT1}$, CH3 = $V_{OUT2}$, CH4 = $V_{OUT3}$*

## NOISE REDUCTION OF THE ADP323 IN ADJUSTABLE MODE

The adjustable LDO circuit can be modified to reduce the output voltage noise to levels close to that of the 500 mV output ADP323. The circuit shown in Figure 56 adds two additional components to the output voltage setting resistor divider. CNR and RNR are added in parallel with R1 to reduce the ac gain of the error amplifier. RNR is chosen to be small with respect to R2. If RNR is 1% to 10% of the value of R2, the minimum ac gain of the error amplifier is approximately 0.1 dB to 0.8 dB. The actual gain is determined by the parallel combination of RNR and R1. This gain ensures that the error amplifier always operates at slightly greater than unity gain.

CNR is chosen by setting the reactance of CNR equal to R1 − RNR at a frequency between 1 Hz and 50 Hz. This setting places the frequency where the ac gain of the error amplifier is 3 dB down from its dc gain.

The noise of the adjustable LDO is found by using the following formula, assuming the noise of the 500 mV output is approximately 14 µV.

$$Noise = 14\ \mu V \times (R_{PAR} + R2)/R2 \quad (1)$$

where $R_{PAR}$ is a parallel combination of *R1* and *RNR*.

Based on the component values shown in Figure 56, the ADP323 has the following characteristics:

- DC gain of 5 (13.98 dB)
- 3 dB roll-off frequency of 0.79 Hz
- High frequency ac gain of 1.02 (0.17 dB)
- Theoretical noise reduction factor of 4.9 (13.8 dB)
- Measured rms noise of the adjustable LDO without noise reduction is 39.5 µV rms
- Measured rms noise of the adjustable LDO with noise reduction is 14.4 µV rms
- Measured noise reduction of approximately 8.8 dB

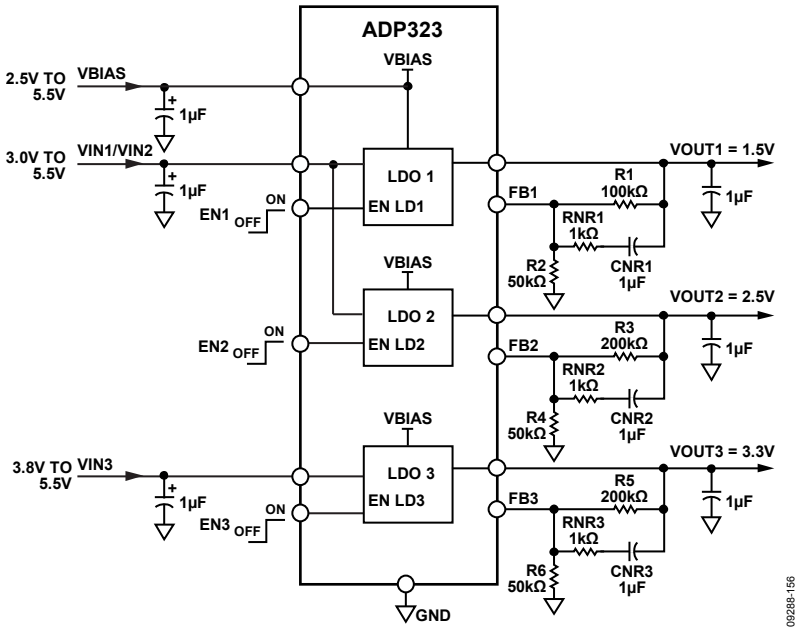


*Figure 56. Noise Reduction Modification*

Note that the measured noise reduction is less than the theoretical noise reduction. Figure 57 shows the noise spectral density of an adjustable ADP323 set to 500 mV and 2.5 V with and without the noise reduction network. The output noise with the noise reduction network is approximately the same for both voltages, especially beyond 10 Hz. The noise of the 500 mV and 2.5 V outputs without the noise reduction network differs by a factor of 5 up to approximately 10 kHz. Above 20 kHz, the closed loop gain of the error amplifier is limited by its open loop gain characteristic. Therefore, the noise contribution from 20 kHz to 100 kHz is less than what it can be if the error amplifier had infinite bandwidth. This is also the reason why the noise is less than what might be expected simply based on the dc gain, that is, 39.5 µV rms vs. 70 µV rms.

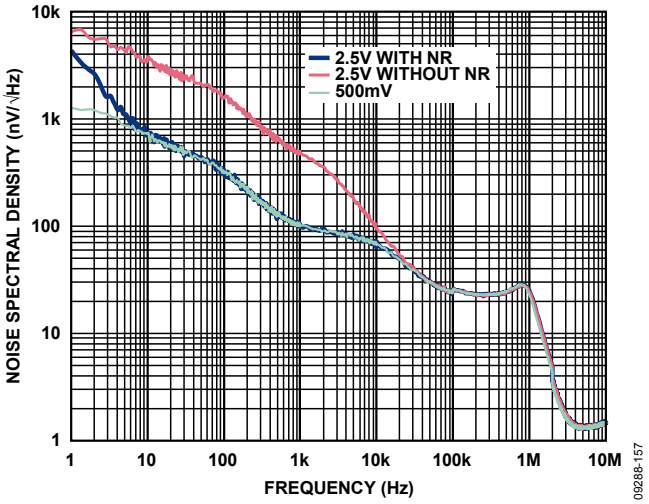


*Figure 57. 500 mV and 2.5 V Output Voltage with and Without Noise Reduction Network*

## CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP322/ADP323 are protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP322/ADP323 are designed to current limit when the output load reaches 300 mA (typical). When the output load exceeds 300 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is built in, which limits the junction temperature to a maximum of 155°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 155°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 140°C, the output is turned on again and the output current is restored to its nominal value.

Consider the case where a hard short from VOUTx to GND occurs. At first, the ADP322/ADP323 limits current so that only 300 mA is conducted into the short. If self heating of the junction is great enough to cause its temperature to rise above 155°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 140°C, the output turns on and conducts 300 mA into the short, again causing the junction temperature to rise above 155°C. This thermal oscillation between 140°C and 155°C causes a current oscillation between 0 mA and 300 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

## THERMAL CONSIDERATIONS

In most applications, the ADP322/ADP323 do not dissipate a lot of heat due to high efficiency. However, in applications with a high ambient temperature and high supply voltage to output voltage differential, the heat dissipated in the package is large enough that it can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 155°C, the converter enters thermal shutdown. It recovers only after the junction temperature decreases below 140°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP322/ADP323 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air ($\theta_{JA}$). The $\theta_{JA}$ number is dependent on the package assembly compounds used and the amount of copper to which the GND pins of the package are soldered on the PCB. Table 7 shows typical $\theta_{JA}$ values for the ADP322/ADP323 for various PCB copper sizes.

**Table 7. Typical $\theta_{JA}$ Values**

| Copper Size (mm²) | ADP322/ADP323 Triple LDO (°C/W) |
|---|---|
| JEDEC[1] | 49.5 |
| 100 | 83.7 |
| 500 | 68.5 |
| 1000 | 64.7 |

[1] Device soldered to JEDEC standard board.

The junction temperature of the ADP322/ADP323 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
$T_A$ is the ambient temperature.
$P_D$ is the power dissipation in the die, given by

$$P_D = \Sigma[(V_{IN} - V_{OUT}) \times I_{LOAD}] + \Sigma(V_{IN} \times I_{GND}) \quad (3)$$

where:
$I_{LOAD}$ is the load current.
$I_{GND}$ is the ground current.
$V_{IN}$ and $V_{OUT}$ are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to

$$T_J = T_A + \{\Sigma[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input to output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 58 to Figure 61 show junction temperature calculations for different ambient temperatures, total power dissipation, and areas of PCB copper.

In cases where the board temperature is known, the thermal characterization parameter, $\Psi_{JB}$, can be used to estimate the junction temperature rise. $T_J$ is calculated from $T_B$ and $P_D$ using the formula

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical $\Psi_{JB}$ value for the 16-lead, 3 mm × 3 mm LFCSP is 25.2°C/W.

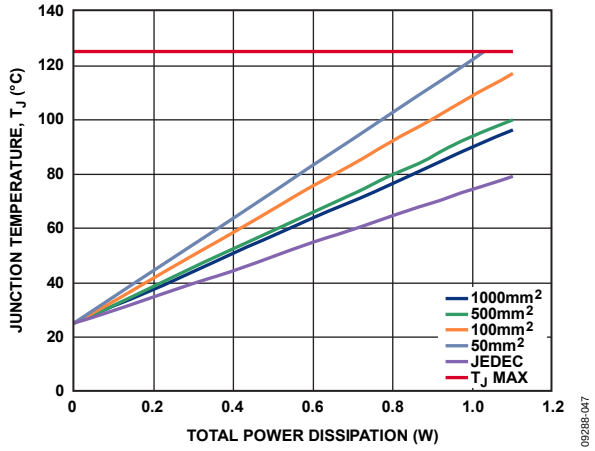


*Figure 58. Junction Temperature vs. Total Power Dissipation, $T_A$ = 25°C*

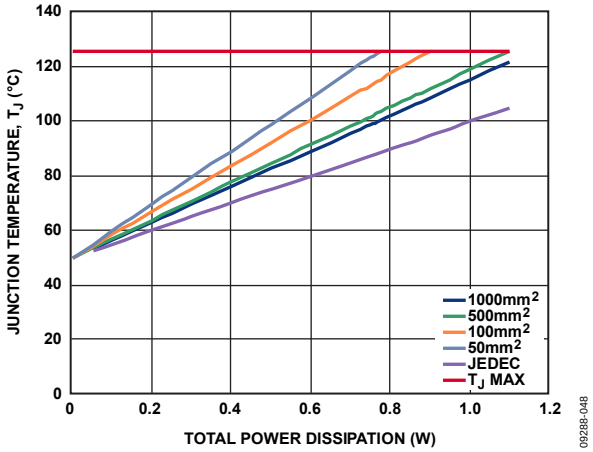


*Figure 59. Junction Temperature vs. Total Power Dissipation, $T_A$ = 50°C*

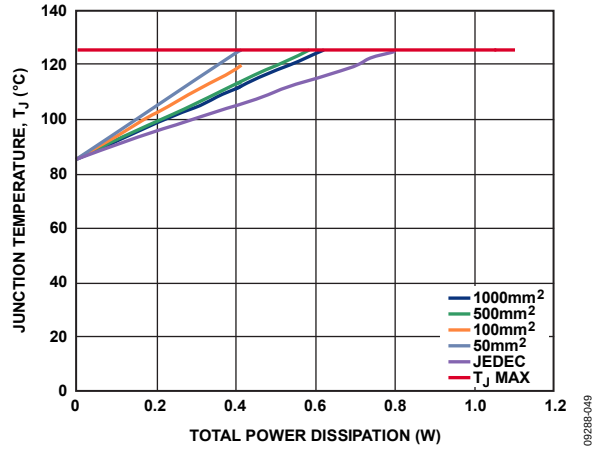


*Figure 60. Junction Temperature vs. Total Power Dissipation, $T_A$ = 85°C*

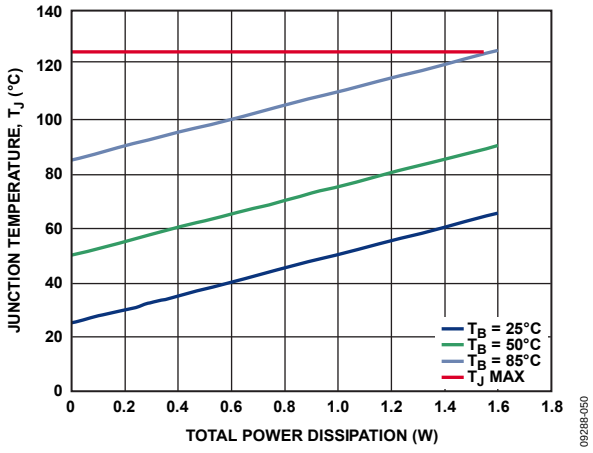


*Figure 61. Junction Temperature vs. Total Power Dissipation and Board Temperature*

## PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP322/ADP323. However, as can be seen from Table 7, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VINx and GND pins. Place the output capacitors as close as possible to the VOUTx and GND pins. Use 0402 or 0603 size capacitors and resistors to achieve the smallest possible footprint solution on boards where area is limited.

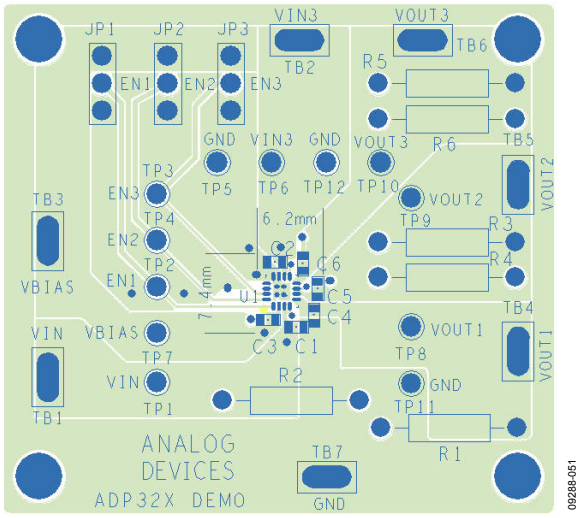


*Figure 62. Example of PCB Layout, Top Side*

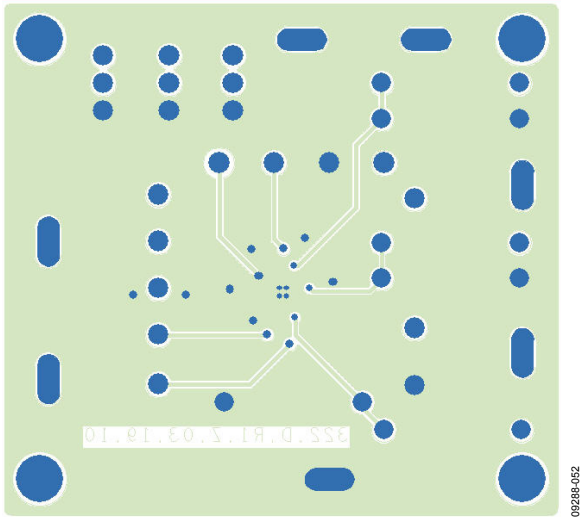


*Figure 63. Example of PCB Layout, Bottom Side*

# OUTLINE DIMENSIONS

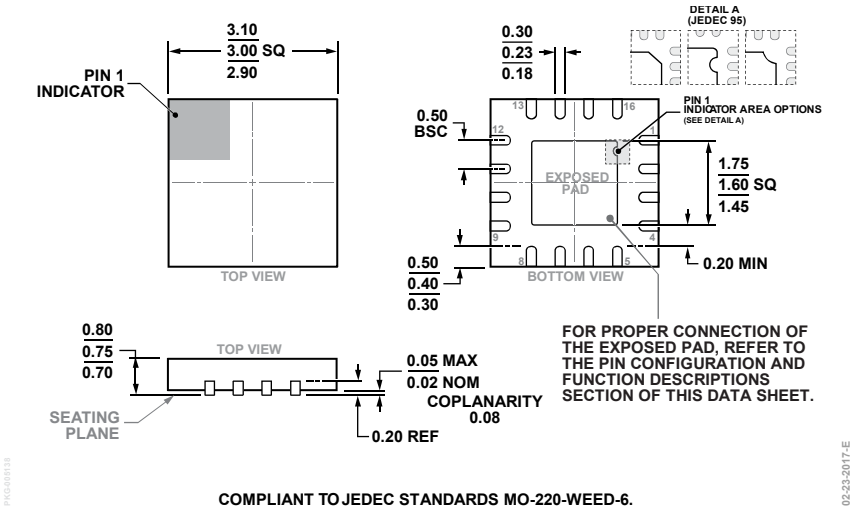


*Figure 64. 16-Lead Lead Frame Chip Scale Package [LFCSP]*
*3 mm × 3 mm Body and 0.75 mm Package Height*
*(CP-16-22)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Output Voltage (V)[2] | | | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|---|
| | | VOUT1 | VOUT2 | VOUT3 | | | |
| ADP322ACPZ-115-R7 | −40°C to +125°C | 3.3 V | 2.8 V | 1.8 V | 16-Lead LFCSP | CP-16-22 | LGU |
| ADP322ACPZ-135-R7 | −40°C to +125°C | 3.3 V | 2.5 V | 1.8 V | 16-Lead LFCSP | CP-16-22 | LGT |
| ADP322ACPZ-145-R7 | −40°C to +125°C | 3.3 V | 2.5 V | 1.2 V | 16-Lead LFCSP | CP-16-22 | LJC |
| ADP322ACPZ-155-R7 | −40°C to +125°C | 3.3 V | 1.8 V | 1.5 V | 16-Lead LFCSP | CP-16-22 | LGS |
| ADP322ACPZ-165-R7 | −40°C to +125°C | 3.3 V | 1.8 V | 1.2V | 16-Lead LFCSP | CP-16-22 | LLX |
| ADP322ACPZ-175-R7 | −40°C to +125°C | 2.8 V | 1.8 V | 1.2 V | 16-Lead LFCSP | CP-16-22 | LGR |
| ADP322ACPZ-189-R7 | −40°C to +125°C | 2.5 V | 1.8 V | 1.2 V | 16-Lead LFCSP | CP-16-22 | LJD |
| ADP323ACPZ-R7 | −40°C to +125°C | Adjustable | Adjustable | Adjustable | 16-Lead LFCSP | CP-16-22 | LGQ |
| ADP323CP-EVALZ | | | | | Evaluation board | | |
| ADP322CPZ-REDYKIT | | | | | Evaluation board kit | | |

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact a local sales or distribution representative.

## NOTES


D09288-0-3/17(D)