38MHz to 320MHz Low Phase Noise VCXO

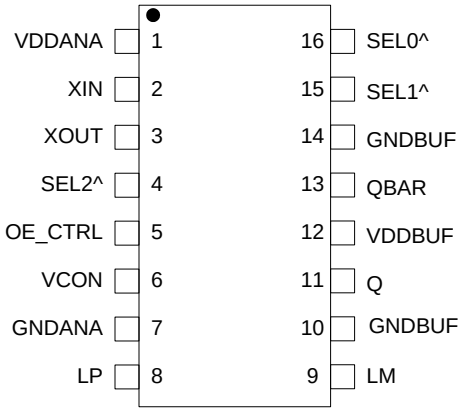
FEATURES

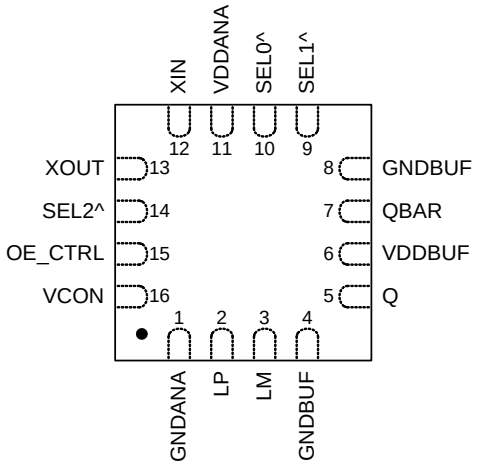
- Typical 0.4ps RMS (12kHz to 20MHz) phase jitter for.
- Typical 25ps (typ.) peak to peak jitter.
- Low phase noise output (@ 1MHz frequency offset
  - o -144dBc/Hz for 155.52MHz
  - o -140dBc/Hz for 311.04MHz
- 19MHz to 40MHz crystal input.
- 38MHz to 320MHz output.
- Available in LVPECL, LVDS, or LVCMOS outputs.
- No external varicap required.
- Output Enable selector.
- Wide pull range (±200ppm).
- 3.3V operation.
- Available in 3x3 QFN or 16-pin TSSOP packages.

DESCRIPTION

The PL580-3X is a monolithic low jitter and low phase noise VCXO, capable of 0.4ps RMS phase jitter and LVCMOS, LVDS, or LVPECL outputs, covering a wide frequency output range up to 320MHz. It allows the control of the output frequency with an input voltage (VCON), using a low cost crystal.
The frequency selector pads of the PL580-3X enable output frequencies of (2, 4, 8, or 16) * F_{XIN}. The PL580-3X is designed to address the demanding requirements of high performance applications such as SONET, GPS, Video, etc.

PACKAGE PIN ASSIGNMENT



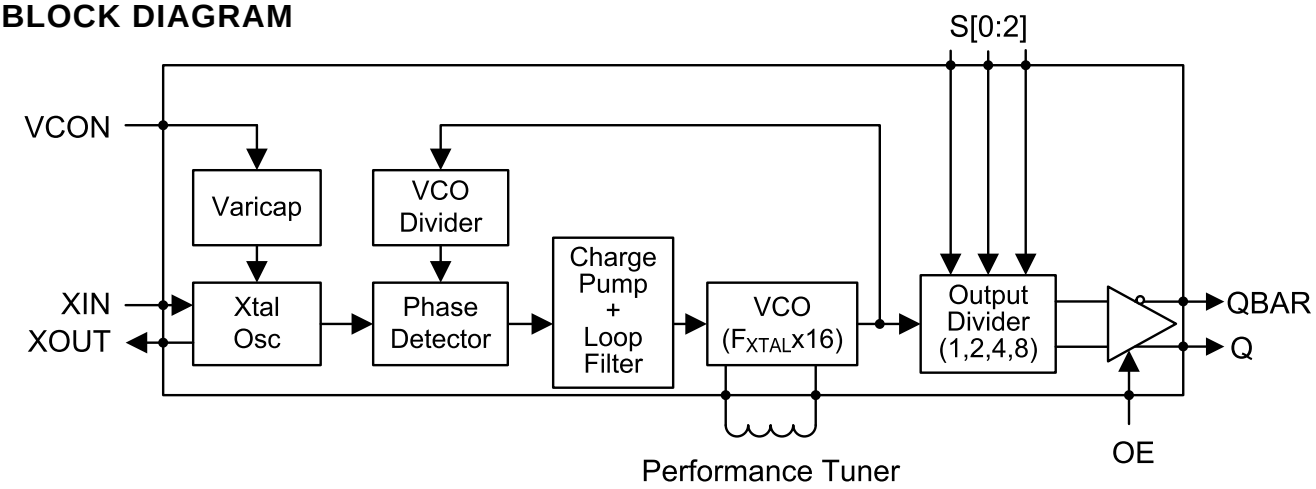


16-pin TSSOP

3x3 QFN

Note1: QBAR is used for single ended LVCMOS output.
Note2: ^ Denotes internal pull up resistor.

BLOCK DIAGRAM



OUTPUT ENABLE LOGIC LEVELS

Part #	OE	State
PL580-38 (LVPECL)	0 (Default)	Output enabled
	1	Tri-state
PL580-35 (LVPECL) PL580-37 (LVCMOS) PL580-39 (LVDS)	0	Tri-state
	1 (Default)	Output enabled

Note: Connect to VDD to set to "1", connect to GND to set to "0".
In case of "0 (Default)" an internal pull-down resistor will set to "0" when pin is left open.
In case of "1 (Default)" an internal pull-up resistor will set to "1" when pin is left open.

PIN DESCRIPTIONS

Name	TSSOP Pin number	3x3mm QFN Pin number	Type	Description
VDDANA	1	11	P	V_{DD} for analog Circuitry.
XIN	2	12	I	Crystal input pin. (See Crystal Specifications on page 4).
XOUT	3	13	O	Crystal output pin. (See Crystal Specifications on page 4).
SEL2	4	14	I	Output frequency Selector pin.
OE_CTRL	5	15	I	Output enable control pin. (See OUTPUT ENABLE LOGIC LEVELS above).
VCON	6	16	I	Voltage control input.
GNDANA	7	1	P	Ground for analog circuitry.
LP	8	2	-	Tuning inductor connection. The inductor is recommended to be a high Q small size 0402 or 0603 SMD component, and must be placed between LP and adjacent LM pin. Place inductor as close to the IC as possible to minimize parasitic effects and to maintain inductor Q.
LM	9	3	-	
GNDBUF	10	4	P	GND connection for output buffer circuitry.
Q	11	5	O	LVPECL or LVDS output.
VDDBUF	12	6	P	V_{DD} connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
QBAR	13	7	O	Complementary LVPECL, LVDS, Or single ended LVCMOS output.
GNDBUF	14	8	P	GND connection for output buffer circuitry.
SEL1	15	9	I	Output frequency Selector pin.
SEL0	16	10	I	Output frequency Selector pin.

FREQUENCY SELECTION TABLE

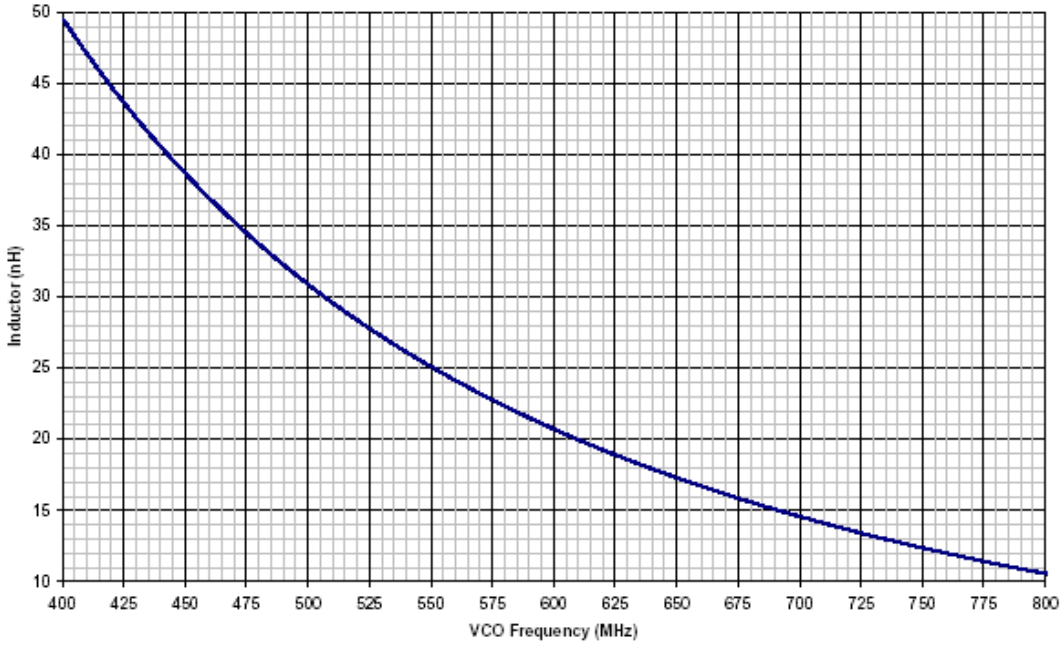
SEL2	SEL1	SEL0	Selected Multiplier/Output Frequency
0	0	0	VCO Max*
0	0	1	VCO Min*
0	1	0	Reserved
0	1	1	Reserved
1	0	0	F_{XTAL} x 2
1	0	1	F_{XTAL} x 8
1	1	0	F_{XTAL} x 16
1	1	1	F_{XTAL} x 4

All SEL pads have internal pull-ups (default value is '1'). Bond to GND to set to 0.
* Special Test Modes to help selecting the inductor value for the target output frequency.

PERFORMANCE TUNING & INDUCTOR VALUE SELECTION

Please refer to PhaseLink's 'PhasorV Tuning Assistance' software to automatically calculate the optimum inductor values for your application. In addition, the chart below could be used as a reference for quick inductor value selection. Please note that the inductor values mentioned in the table below, or when using 'PhasorV Tuning Assistance' are derived based on the parasitic values of PhaseLink's evaluation board. For performance enhancement of your custom board design, please follow the following instruction:

Use the special test modes "VCO Max" and "VCO Min" to determine the optimum inductor value. "VCO Max" represents the high end of the VCO range and "VCO Min" represents the low end of the VCO range. The output frequency in the "VCO Max" and "VCO Min" test modes is VCO/16. This means that the output frequencies are around the crystal frequency that will be used. The optimum inductor value is where the target crystal frequency is closest to the middle between the "VCO Max" and "VCO Min" output frequencies. In this case the VCO will lock in the middle of its tuning range with maximum margin on either side.



ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model		2		kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.* Note: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XTAL}	Parallel Fundamental Mode	19		40	MHz
Crystal Loading Rating	$C_{L\ (XTAL)}$	at VCON = 0V		17.7		pF
		at VCON = 1.65V		9.5		
		at VCON = 3.3V		5.4		
Crystal Pullability	$C_0/C_{1\ (XTAL)}$	AT cut			250	-
Recommended ESR	R_E	AT cut			30	Ω

Note: Crystal Loading rating: The listed numbers are for the IC only. Specify the crystal for the value at VCON = 1.65V and add the PCB & package parasitic. A round number (i.e. 12pF) can be achieved by adding external capacitors. Try to add the same value to XIN and XOUT, and please note, that frequency pulling and oscillator gain may decrease.

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	I_{DD}	LVPECL/ LVDS/ LVCMOS	38MHz<F_{OUT}<100MHz			65/45/30	mA
			100MHz<F_{OUT}<320MHz			80/60/40	
Operating Voltage	V_{DD}			2.97		3.63	V
Output Clock Duty Cycle		@ 50% V_{DD} (LVCMOS) @ 1.25V (LVDS) @ V_{DD} – 1.3V (LVPECL)		45	50	55	%
Short Circuit Current					±50		mA

Note: LVCMOS output is not advised above 200MHz with 15pF load; and 320MHz with 10pF load.

4. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		F_{XTAL} = 19 to 40MHz; XTAL C_0/C_1 < 250 0V ≤ VCON ≤ 3.3V		500		ppm
CLK Output Pullability		VCON=1.65V, ±1.65V	±200			ppm
VCXO Tuning Characteristic				150		ppm/V
Pull Range Linearity					10	%
VCON Input Impedance			60	80		kΩ
VCON Modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

5. Jitter Specifications

PARAMETERS	CONDITIONS	FREQUENCY	MIN.	TYP.	MAX.	UNITS
Integrated Jitter RMS	With capacitive decoupling between V_{DD} and GND. Integrated 12kHz to 20MHz	155.52MHz		0.4	0.5	ps
		311.04MHz		0.4	0.5	
Period Jitter RMS	With capacitive decoupling between V_{DD} and GND. Over 10,000 cycles.	77.76MHz		2.5	4	ps
		155.52MHz		3	5	
		311.04MHz		4	7	
Period Jitter Peak-to-Peak	With capacitive decoupling between V_{DD} and GND. Over 10,000 cycles.	77.76MHz		18	30	ps
		155.52MHz		20	30	
		311.04MHz		25	35	

6. Phase Noise Specifications

PARAMETERS	FREQ.	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	@1M	@10M	UNITS
Phase Noise relative to carrier (typical)	77.76MHz	-66	-96	-124	-134	-132	-145	-149	dBc/Hz
	155.52MHz	-62	-92	-120	-132	-128	-144	-150	
	311.04MHz	-59	-86	-116	-129	-124	-140	-148	

Note: Phase Noise measured at VCON = 0V.

7. LVCMOS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Drive Current	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	30			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	30			mA
Output Clock Rise/Fall Time		0.3V ~ 3.0V with 15 pF load		0.7		ns
Output Clock Rise/Fall Time		20%-80% with 50Ω Load		0.3		ns

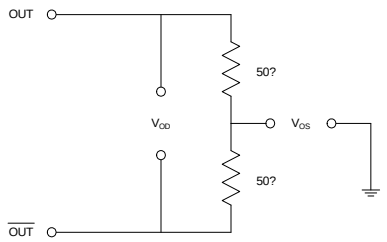
8. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

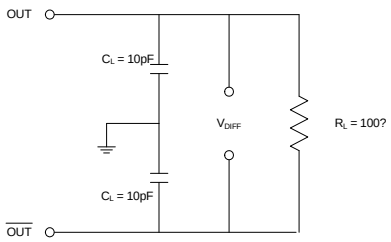
9. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

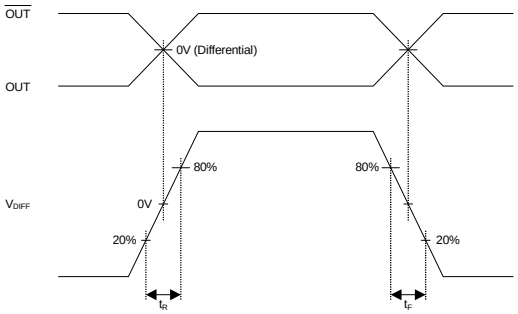
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



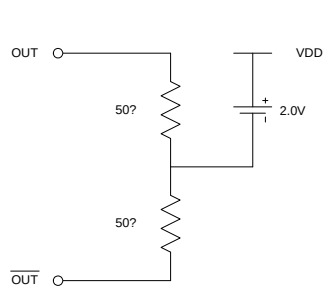
10. LVPECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

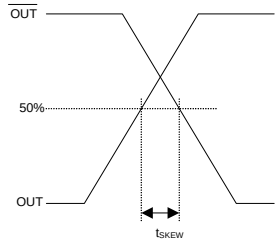
11. LVPECL Switching Characteristics

PARAMETERS	SYMBOL	FREQ.	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise & Fall Times	t_r & t_f	<150MHz	20/80% - LVPECL	0.2	0.5	0.7	ns
Clock Rise & Fall Times		>150MHz <320MHz	80/20% - LVPECL	0.2	0.4	0.55	

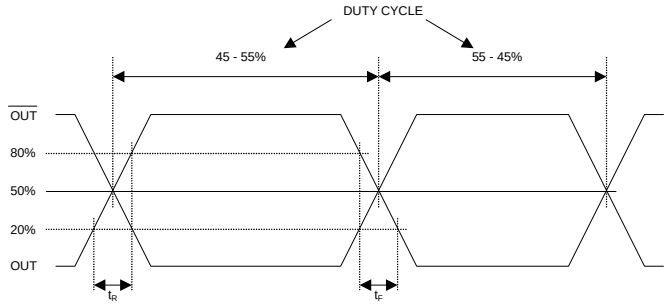
LVPECL Levels Test Circuit



LVPECL Output Skew



LVPECL Transistion Time Waveform



LAYOUT RECOMMENDATIONS

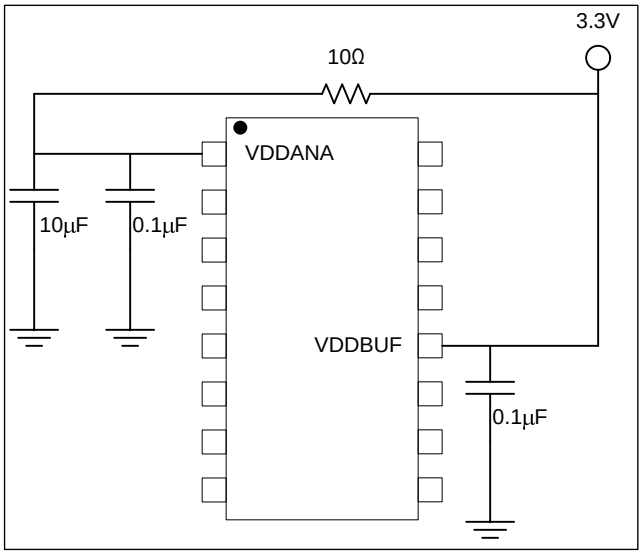
PCB LAYOUT CONSIDERATIONS FOR PERFORMANCE OPTIMIZATION

The following guidelines are to assist you with a performance optimized PCB design:

- Keep all the PCB traces to PL580 as short as possible, as well as keeping all other traces as far away from it as possible.
- Place the crystal as close as possible to both crystal pins of the device. This will reduce the cross-talk between the crystal and the other signals.
- Separate crystal pin traces from the other signals on the PCB, but allow ample distance between the two crystal pin traces.
- Place a 0.01µF~0.1µF decoupling capacitor between VDD and GND, on the component side of the PCB, close to the VDD pin. It is not recommended to place this component on the backside of the PCB. Going through vias will reduce the signal integrity, causing additional jitter and phase noise.
- It is highly recommended to keep the VDD and GND traces as short as possible.
- When connecting long traces (> 1 inch) to a CMOS output, it is important to design the traces as a transmission line or 'stripline', to avoid reflections or ringing. In this case, the CMOS output needs to be matched to the trace impedance. Usually 'striplines' are designed for 50Ω impedance and CMOS outputs usually have lower than 50Ω impedance so matching can be achieved by adding a resistor in series with the CMOS output pin to the 'stripline' trace.
- Please contact PhaseLink for the application note on how to design outputs driving long traces or the Gerber files for the PL580 layout.

POWER SUPPLY FILTERING CIRCUIT

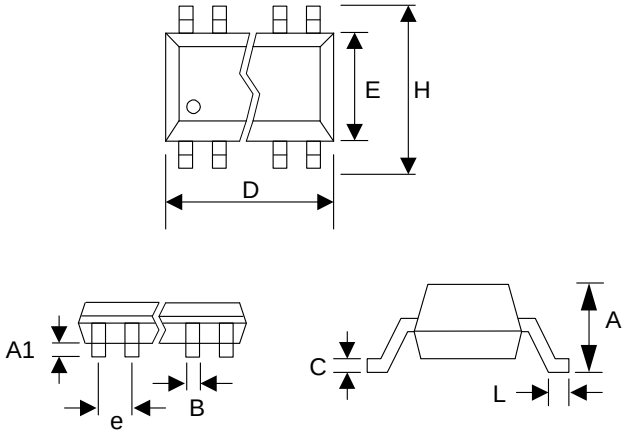
In order to keep power supply noise from affecting the jitter performance, the following power supply filtering circuit is recommended for all designs.



PACKAGE INFORMATION

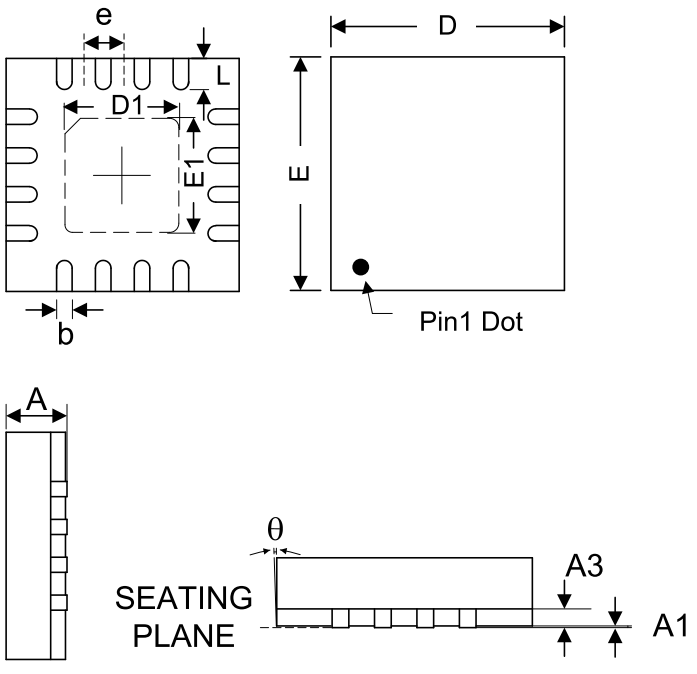
16-PIN SSOP

16 PIN TSSOP (mm)		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



16-PIN 3x3 QFN

Symbol	Dimension (mm)		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.203 Ref		
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.65	1.70	1.75
E1	1.65	1.70	1.75
L	0.250	0.300	0.350
e	0.50BSC		



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL580-3X X X - X

Part Number

None=Tubes
R=Tape and Reel

Package Type
O = TSSOP-16L
Q = QFN-16L

Temperature Range
C=Commercial (0°C to 70°C)
I=Industrial (-40°C to 85°C)

Order Number	Marking*	Package Option
PL580-3xOC	P580-3x OC LLLLL	TSSOP - Tube
PL580-3xOC-R		TSSOP - Tape & Reel
PL580-3xQC-R	P580 3x LLL	QFN - Tape & Reel
PL580-3xOI	P580-3x OI LLLLL	TSSOP - Tube
PL580-3xOI-R		TSSOP - Tape & Reel
PL580-3xQI-R	P580 3xI LLL	QFN - Tape & Reel

*Note: LLLLL and LLL designate lot number