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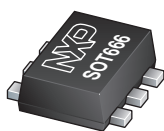
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Kind regards,

Team Nexperia



# PMDT290UNE

20 V, 800 mA dual N-channel Trench MOSFET

Rev. 1 — 13 September 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

### 1.3 Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

### 1.4 Quick reference data

Table 1. Quick reference data

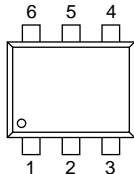
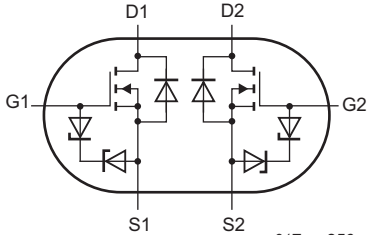
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	20	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	800	mA
<b>Static characteristics (per transistor)</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 500\text{ mA}; T_j = 25\text{ °C}$	-	290	380	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p><b>SOT666</b></p>	 <p>017aaa256</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
PMDT290UNE	-	plastic surface-mounted package; 6 leads	SOT666

## 4. Marking

**Table 4. Marking codes**

Type number	Marking code
PMDT290UNE	AE

## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

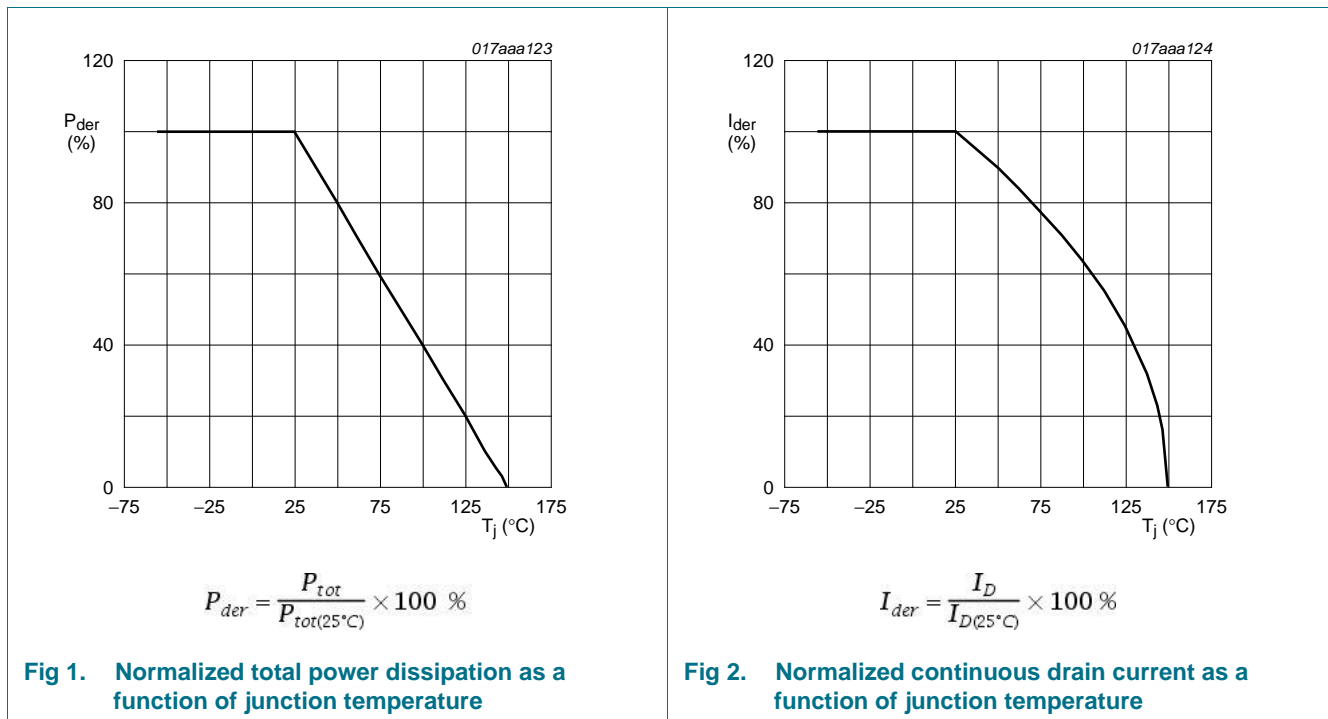
Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per transistor</b>					
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	20	V
$V_{GS}$	gate-source voltage		-8	8	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	800	mA
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	500	mA
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$	-	3.2	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	330	mW
			[1]	390	mW
		$T_{sp} = 25\text{ °C}$	-	1090	mW
<b>Per device</b>					
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	500	mW
$T_j$	junction temperature		-55	150	°C
$T_{amb}$	ambient temperature		-55	150	°C

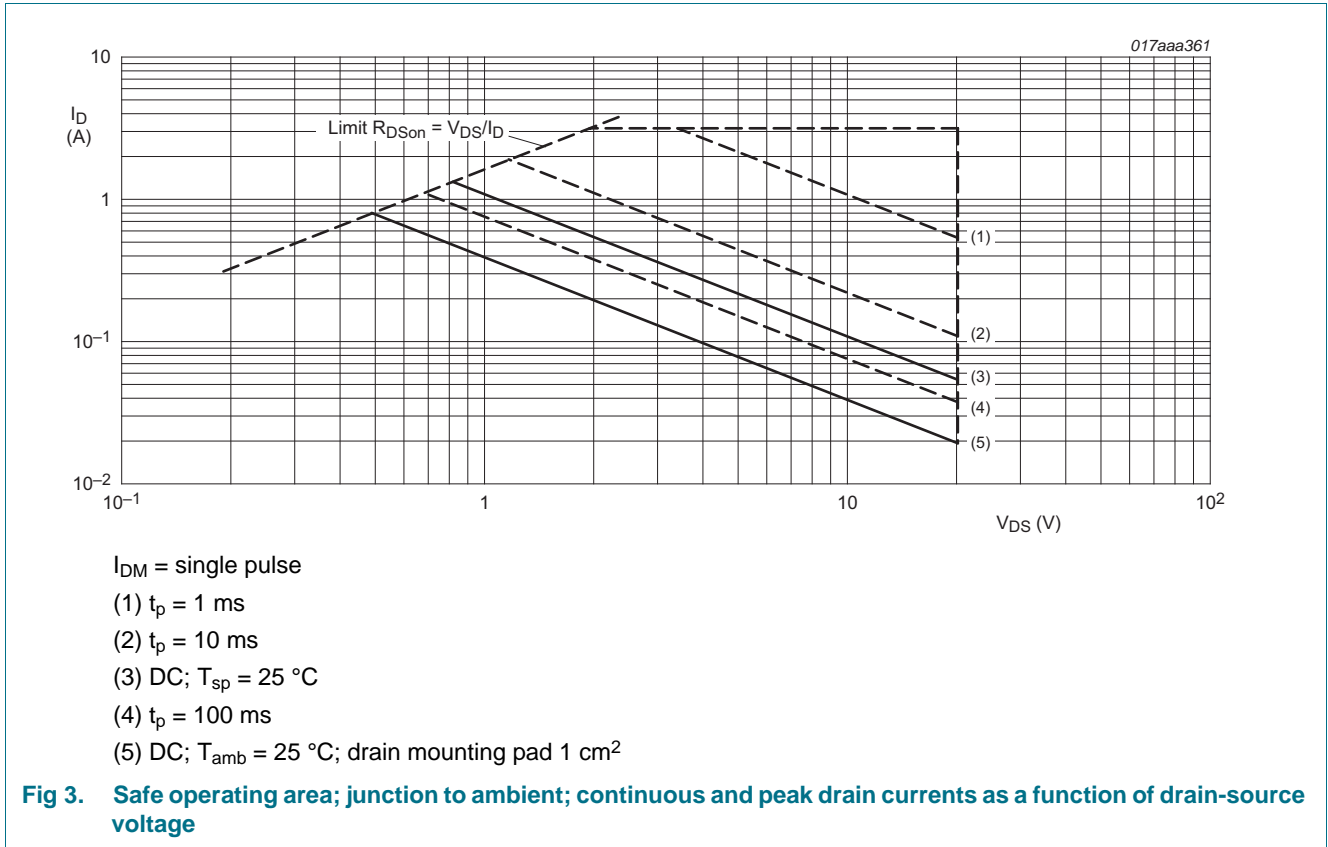
**Table 5. Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>stg</sub>	storage temperature		-65	150	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	-	370	mA
<b>ESD maximum rating</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[3]	2000	V

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





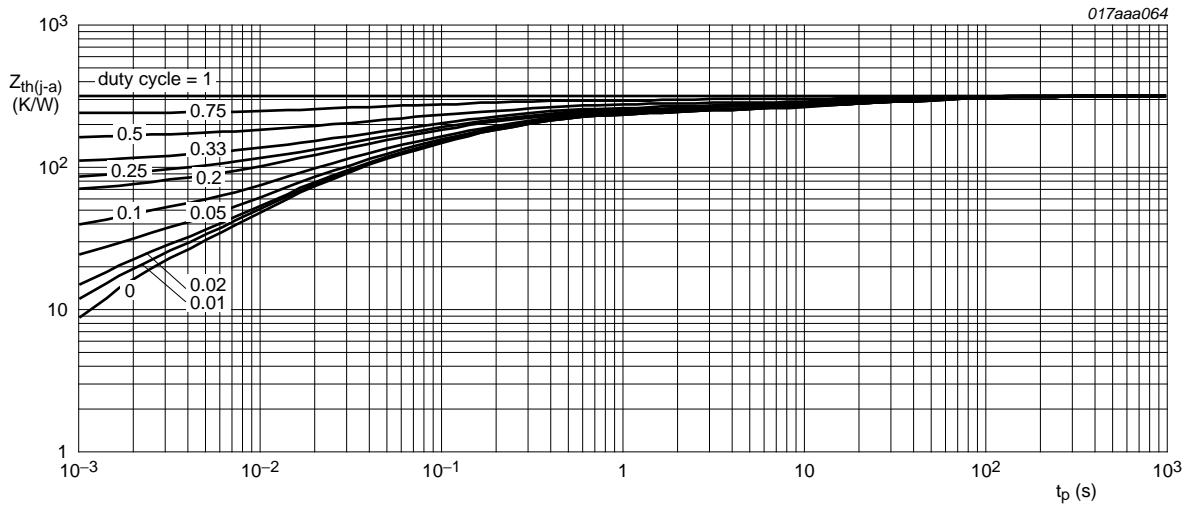
## 6. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	330	380	K/W
			[2]	-	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	115	K/W
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250	K/W

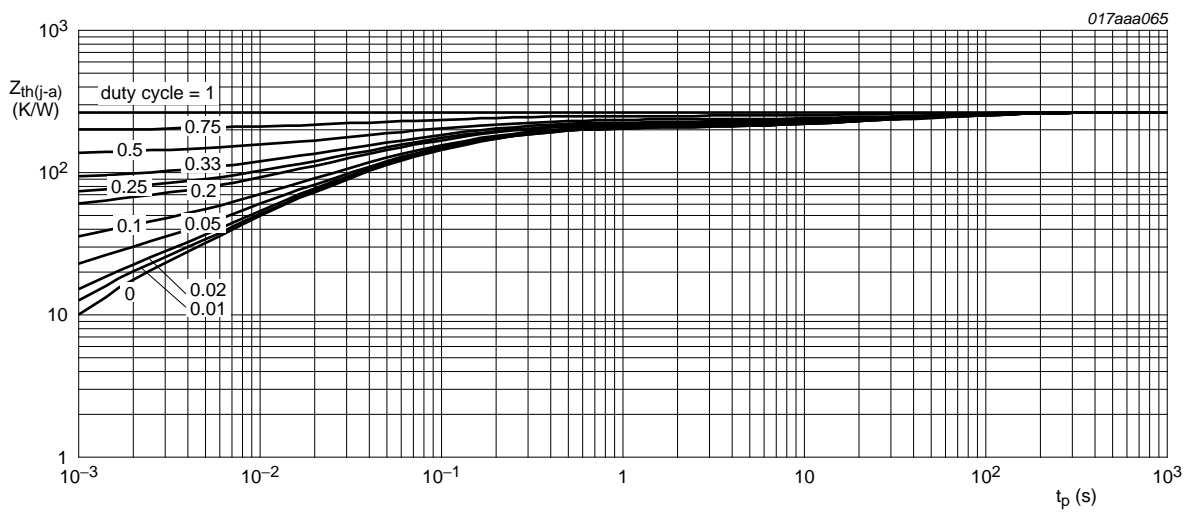
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $1$  cm<sup>2</sup>.



FR4 PCB; standard footprint

**Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



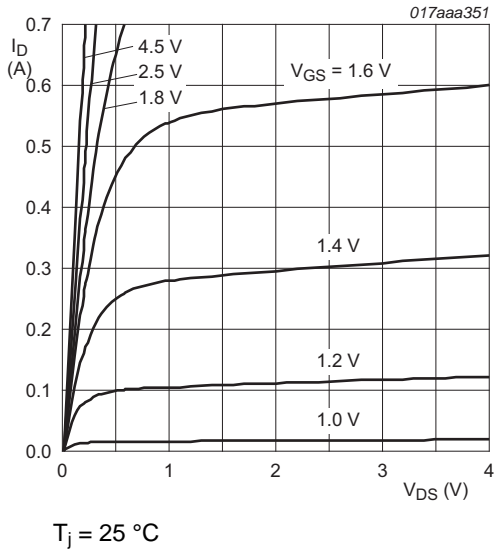
FR4 PCB, mounting pad for drain 1 cm<sup>2</sup>

**Fig 5. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

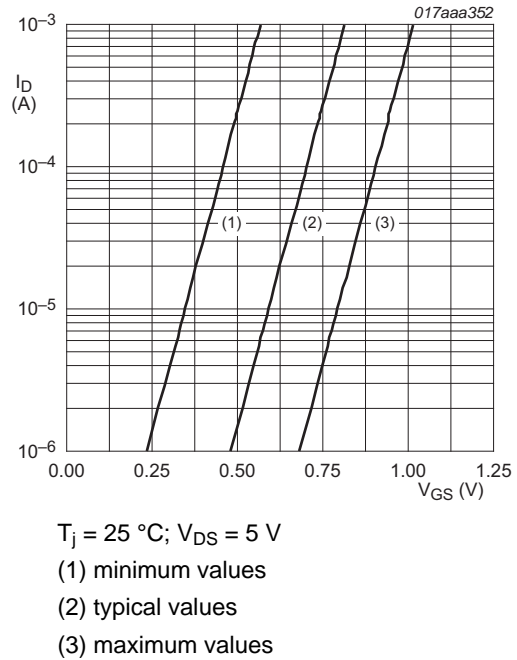
## 7. Characteristics

Table 7. Characteristics

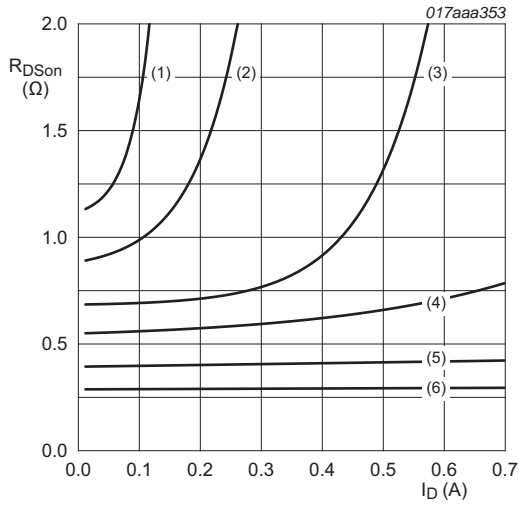
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$	0.5	0.75	0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = 20 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 20 V$ ; $V_{GS} = 0 V$ ; $T_j = 150 \text{ }^\circ C$	-	-	10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	2	$\mu A$
		$V_{GS} = -8 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	2	$\mu A$
		$V_{GS} = 4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	500	nA
		$V_{GS} = -4.5 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	-	500	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 V$ ; $I_D = 500 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	290	380	m $\Omega$
		$V_{GS} = 4.5 V$ ; $I_D = 500 \text{ mA}$ ; $T_j = 150 \text{ }^\circ C$	-	460	610	m $\Omega$
		$V_{GS} = 2.5 V$ ; $I_D = 400 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	420	620	m $\Omega$
		$V_{GS} = 1.8 V$ ; $I_D = 100 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	600	1100	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 V$ ; $I_D = 200 \text{ mA}$ ; $T_j = 25 \text{ }^\circ C$	-	1.6	-	S
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 10 V$ ; $I_D = 500 \text{ mA}$ ; $V_{GS} = 4.5 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.45	0.68	nC
$Q_{GS}$	gate-source charge		-	0.15	-	nC
$Q_{GD}$	gate-drain charge		-	0.15	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 10 V$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	55	83	pF
$C_{oss}$	output capacitance		-	15	-	pF
$C_{rss}$	reverse transfer capacitance		-	7	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 V$ ; $R_L = 250 \text{ } \Omega$ ; $V_{GS} = 4.5 V$ ; $R_{G(ext)} = 6 \text{ } \Omega$ ; $T_j = 25 \text{ }^\circ C$	-	6	12	ns
$t_r$	rise time		-	4	-	ns
$t_{d(off)}$	turn-off delay time		-	86	172	ns
$t_f$	fall time		-	31	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = 300 \text{ mA}$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	0.48	0.77	1.2	V



**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**

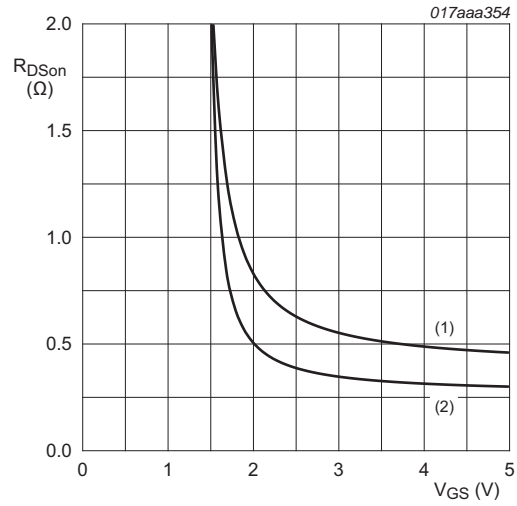


**Fig 7. Sub-threshold drain current as a function of gate-source voltage**  
 (1) minimum values  
 (2) typical values  
 (3) maximum values



$T_j = 25\text{ °C}$   
 (1)  $V_{GS} = 1.3\text{ V}$   
 (2)  $V_{GS} = 1.4\text{ V}$   
 (3)  $V_{GS} = 1.6\text{ V}$   
 (4)  $V_{GS} = 1.8\text{ V}$   
 (5)  $V_{GS} = 2.5\text{ V}$   
 (6)  $V_{GS} = 4.5\text{ V}$

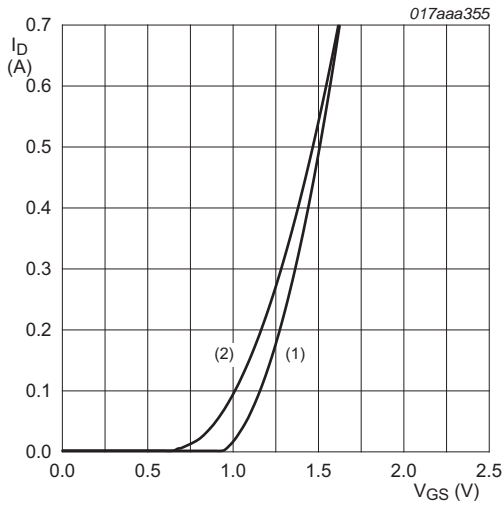
**Fig 8. Drain-source on-state resistance as a function of drain current; typical values**



$I_D = 400\text{ mA}$   
 (1)  $T_j = 150\text{ °C}$   
 (2)  $T_j = 25\text{ °C}$

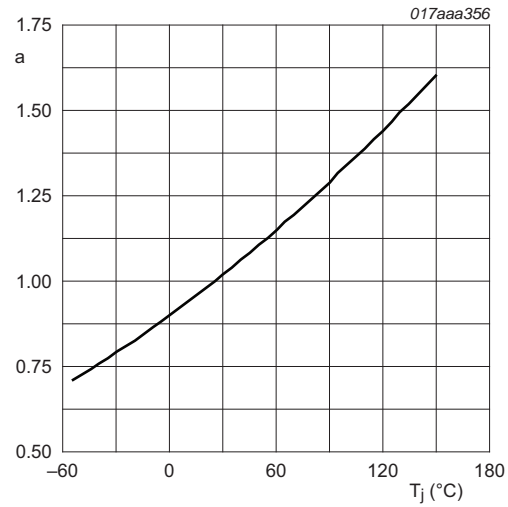
**Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**





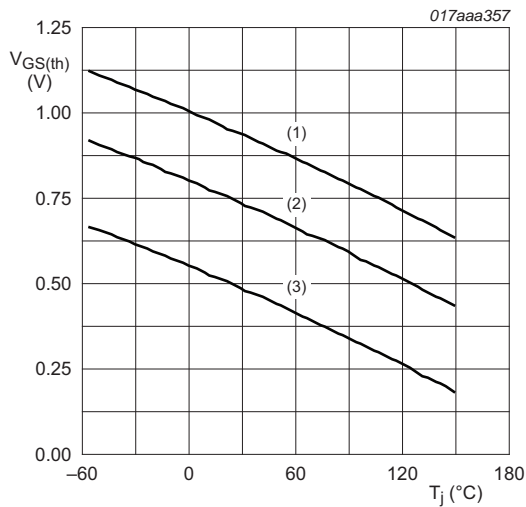
$V_{DS} > I_D \times R_{DS(on)}$   
 (1)  $T_j = 25\text{ °C}$   
 (2)  $T_j = 150\text{ °C}$

**Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



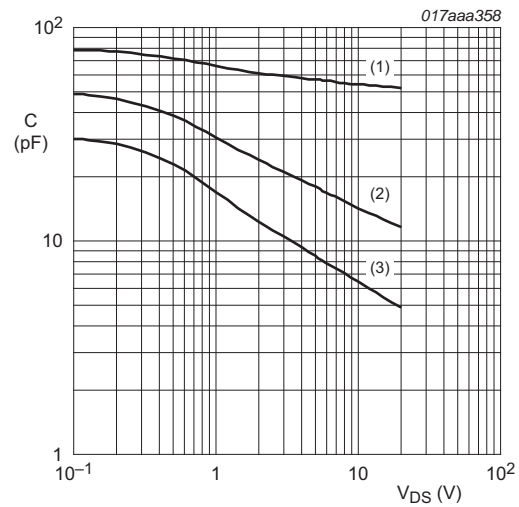
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ C)}}$$

**Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**



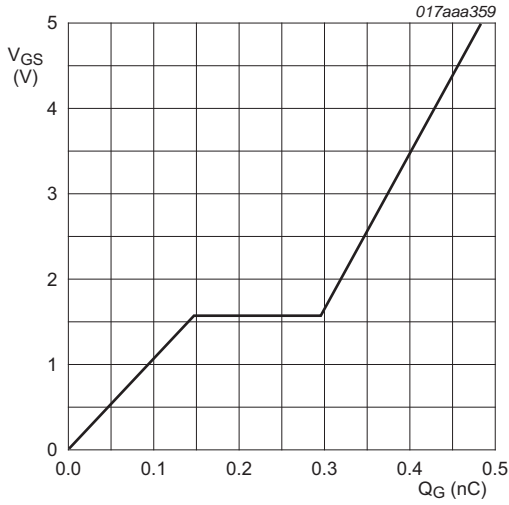
$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

**Fig 12. Gate-source threshold voltage as a function of junction temperature**



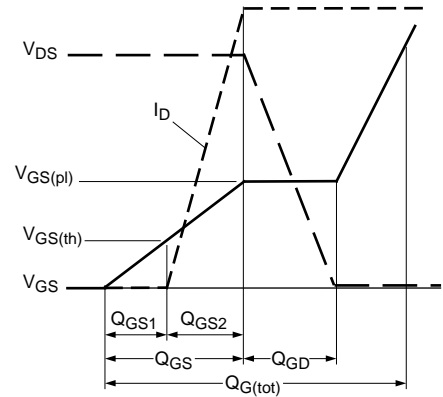
$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

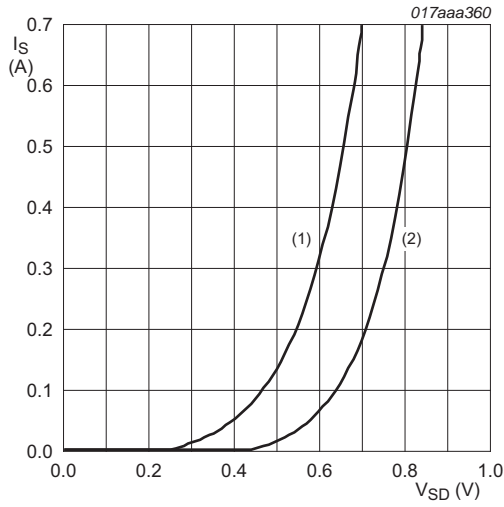


$I_D = 0.5 \text{ A}; V_{DS} = 10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



**Fig 15. Gate charge waveform definitions**



$V_{GS} = 0 \text{ V}$   
 (1)  $T_j = 150 \text{ }^\circ\text{C}$   
 (2)  $T_j = 25 \text{ }^\circ\text{C}$

**Fig 16. Source current as a function of source-drain voltage; typical values**

## 8. Test information

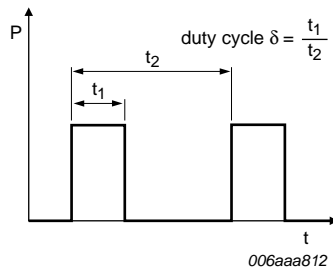


Fig 17. Duty cycle definition

### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

**9. Package outline**

Plastic surface-mounted package; 6 leads

SOT666

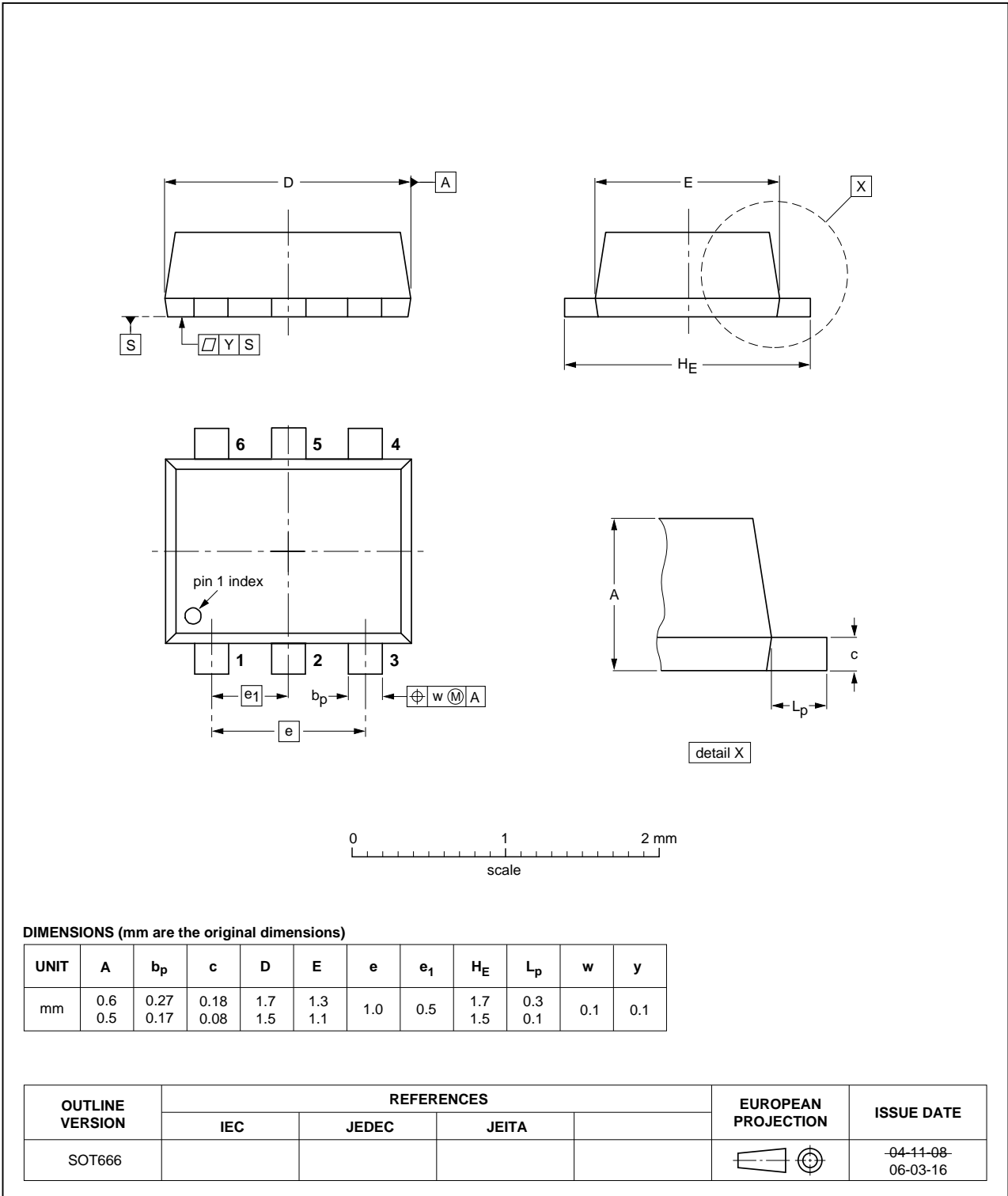
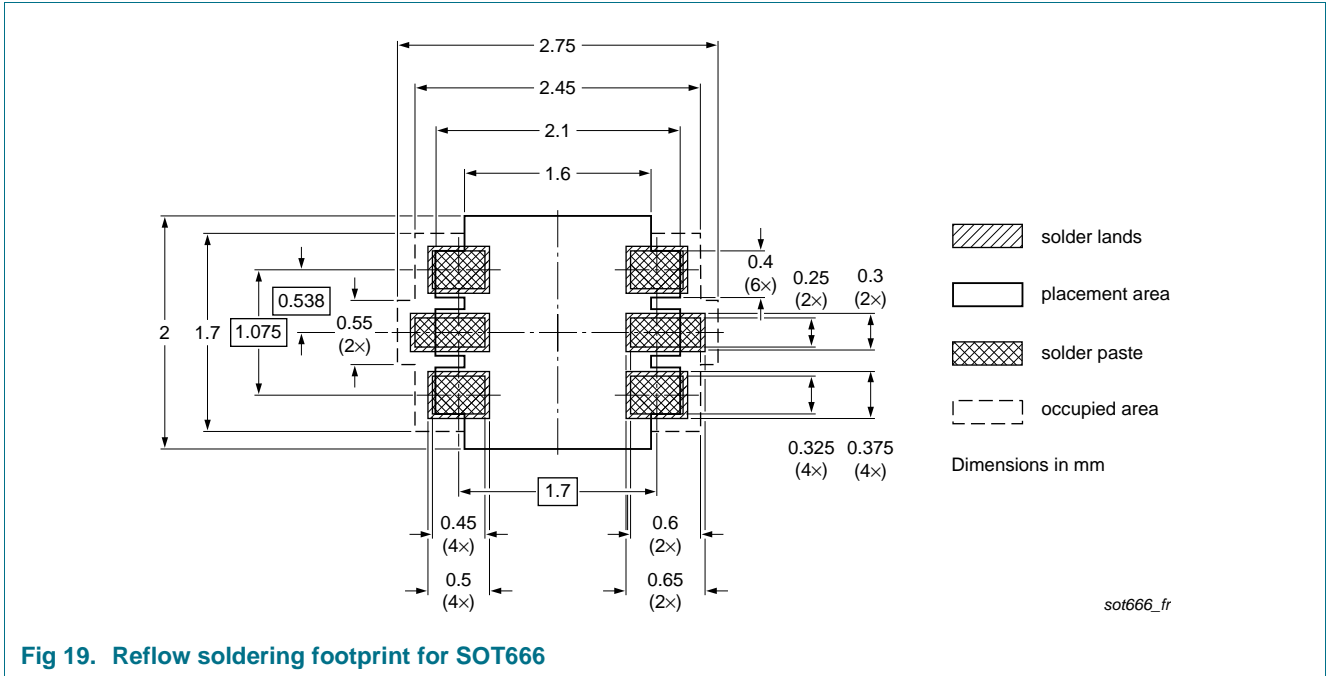


Fig 18. Package outline SOT666

**10. Soldering**



**Fig 19. Reflow soldering footprint for SOT666**

## 11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMDT290UNE v.1	20110913	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <a href="#">[1]</a> <a href="#">[2]</a>	Product status <a href="#">[3]</a>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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