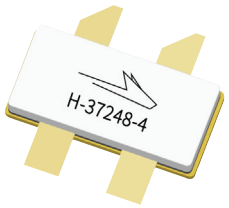
PXAC182002FC

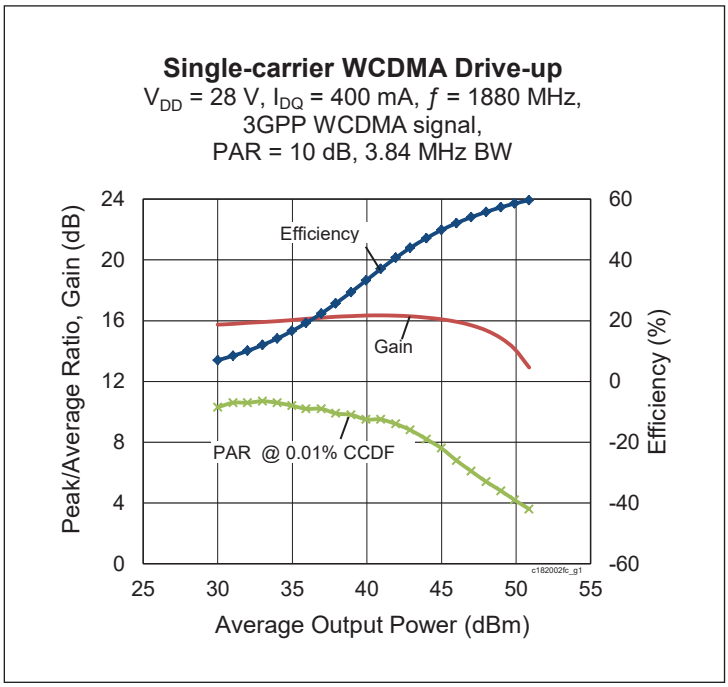
Thermally-Enhanced High Power RF LDMOS FET
180 W, 28 V, 1805 – 1880 MHz

Description

The PXAC182002FC is a 180-watt LDMOS FET with an asymmetrical design intended for use in multi-standard cellular power amplifier applications in the 1805 to 1880 MHz frequency band. Features include dual-path design, input and output matching, high gain and thermally-enhanced package with earless flanges. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PXAC182002FC
Package H-37248-4





Features

- Broadband internal input and output matching
- Asymmetrical Doherty design
  - Main: 70 W Typ (P_{1dB})
  - Peak: 110 W Typ (P_{1dB})
- Typical pulsed CW performance, 1880 MHz, 28 V, combined outputs
  - Output power at P_{3dB} = 194 W
  - Efficiency = 64%
  - Gain = 14 dB
- Capable of handling 10:1 VSWR @28 V, 110 W (CW) output power
- Integrated ESD protection
- Human Body Model Class 1C (per ANSI/ESDA/JEDEC/JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in Wolfspeed Doherty test fixture)
V_{DD} = 28 V, I_{DQ} = 400 mA, V_{GSPEAK} = 1.1 V, P_{OUT} = 28.2 W avg, f = 1880 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	15.5	16.5	—	dB
Drain Efficiency	η_D	48.5	51	—	%
Adjancent Channel Power Ratio	ACPR	—	–30	–26	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	0.1	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
On-State Resistance (main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.18	—	Ω
(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.135	—	Ω
Operating Gate Voltage (main)	V_{DS} = 28 V, I_{DQ} = 400 mA	V_{GS}	2.55	2.65	2.75	V
(peak)	V_{DS} = 28 V, I_{DQ} = 0 A	V_{GS}	0.9	1.2	1.3	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	0.1	µA

Maximum Ratings

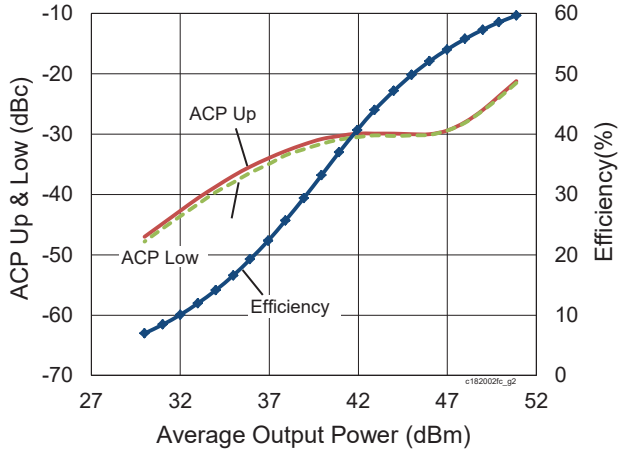
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance (main, T_{CASE} = 70°C, 28 W CW)	$R_{\theta JC}$	1.088	°C/W
(peak, T_{CASE} = 70°C, 100 W CW)	$R_{\theta JC}$	0.587	°C/W

Ordering Information

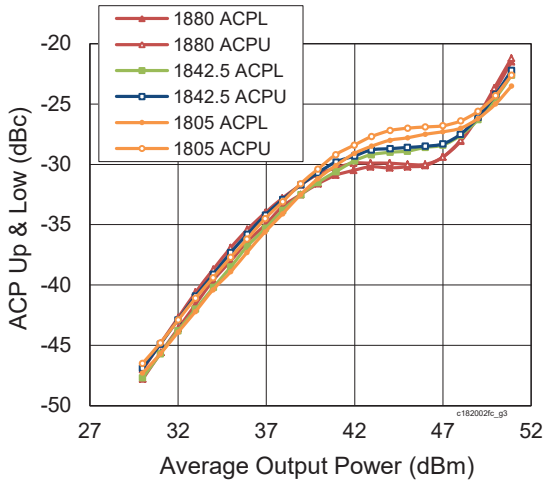
Type and Version	Order Code	Package Description	Shipping
PXAC182002FC V1 R0	PXAC182002FC-V1-R0	H-37248-4, earless flange	Tape & Reel, 50 pcs
PXAC182002FC V1 R250	PXAC182002FC-V1-R250	H-37248-4, earless flange	Tape & Reel, 250 pcs

Typical Performance (data taken in a production test fixture)

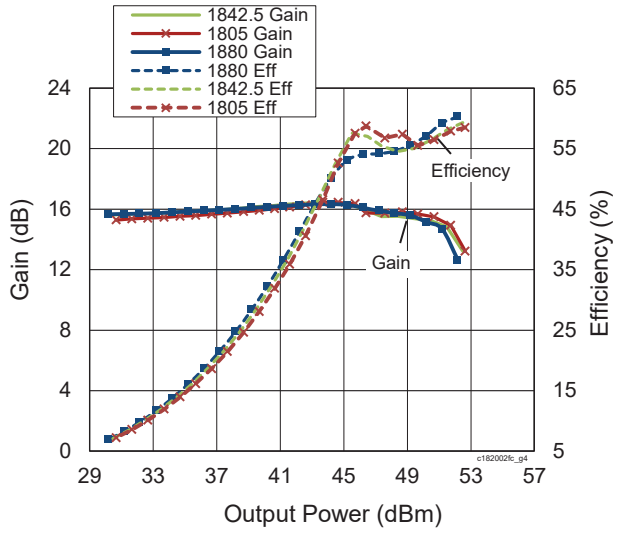
Single-carrier WCDMA Drive-up
V_{DD} = 28 V, I_{DQ} = 400 mA, f = 1880 MHz,
3GPP WCDMA signal, PAR = 10 dB,
BW = 3.84 MHz



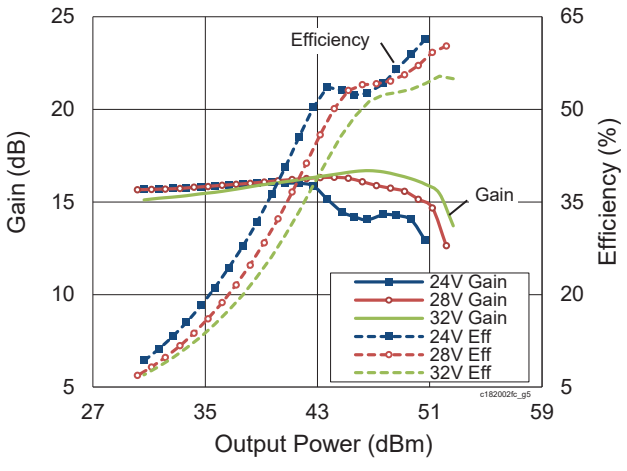
Single-carrier WCDMA 3GPP Drive-up
V_{DD} = 28 V, I_{DQ} = 400 mA, f = 1805-1880 MHz,
3GPP WCDMA signal, PAR = 10 dB,
BW = 3.84 MHz



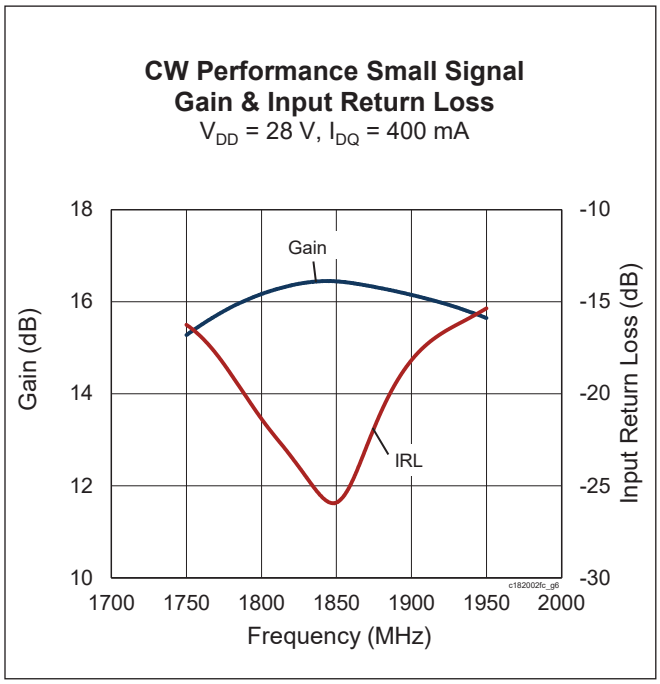
CW Performance
V_{DD} = 28 V, I_{DQ} = 400mA



CW Performance
at various V_{DD}
I_{DQ} = 400 mA, f = 1880 MHz



Typical Performance (cont.)



Load Pull Performance

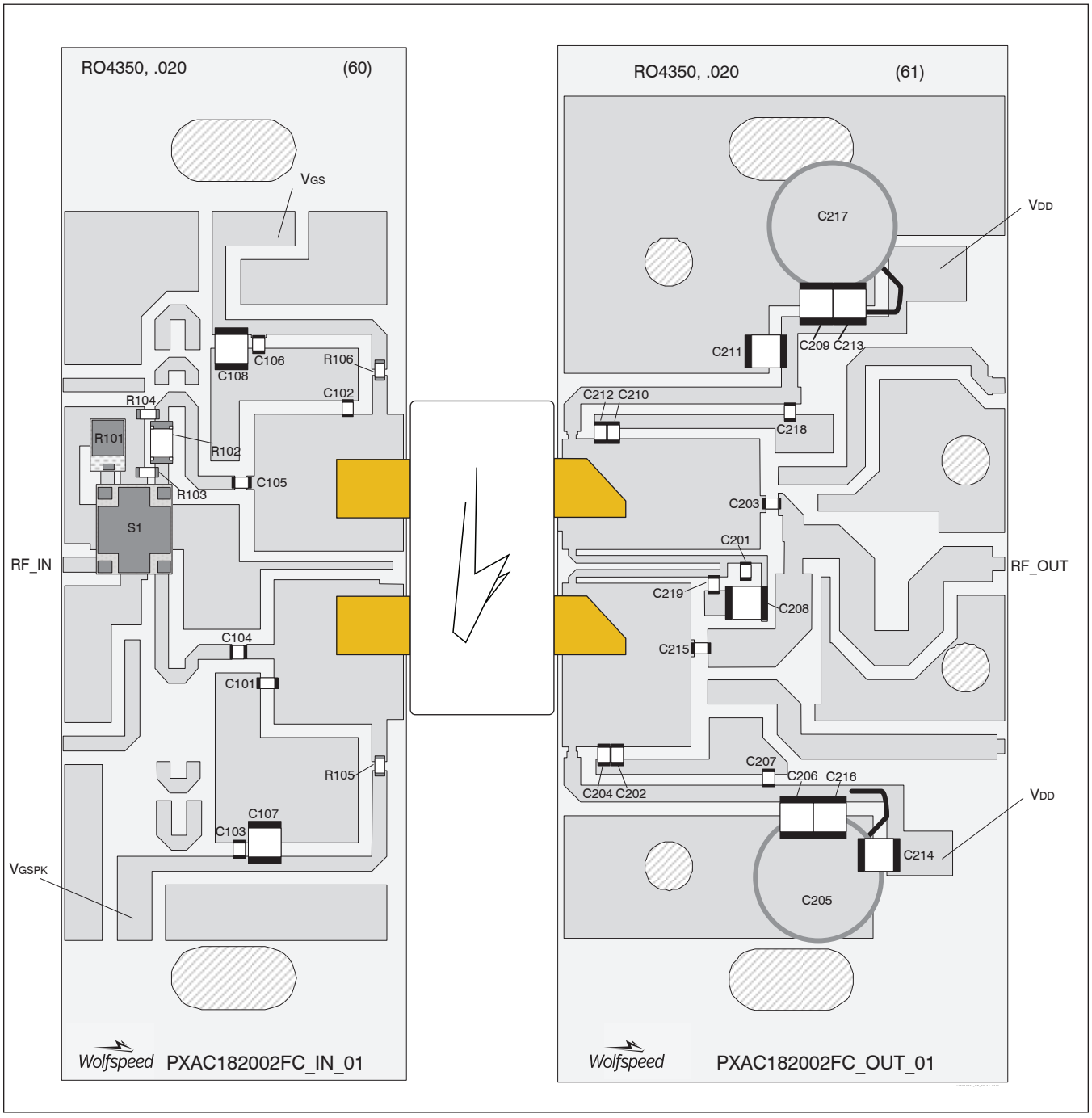
Main Side Load Pull Performance – Pulsed CW signal: 160 µs, 10% duty cycle, 28 V, I_{DQ} = 405 mA

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
1810	3.94 – j10.15	2.92 – j5.27	19.2	49.4	86	54.0	6.49 – j2.19	21.9	47.2	52	66.6
1840	5.13 – j10.93	2.93 – j4.16	19.5	49.3	85	57.6	5.82 – j2.44	21.7	47.5	56	66.3
1880	5.90 – j12.44	2.73 – j5.17	19.2	49.5	89	55.2	4.53 – j2.29	21.5	47.7	59	67.9

Peak Side Load Pull Performance – Pulsed CW signal: 160 µs, 10% duty cycle, 28 V, I_{DQ} = 685 mA

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
1810	3.71 – j9.13	4.64 – j5.44	20.5	50.9	123	55.5	3.52 – j2.84	22.7	49.7	94	66.2
1840	4.76 – j8.65	4.66 – j5.68	20.6	50.7	117	54.5	3.39 – j3.01	23.2	49.2	84	64.1
1880	6.40 – j9.13	4.63 – j5.74	20.8	50.7	116	54.3	2.83 – j3.50	23.1	49.2	83	64.3

Reference Circuit , 1805 – 1880 MHz



Reference circuit assembly diagram (not to scale)

Reference Circuit (cont.)

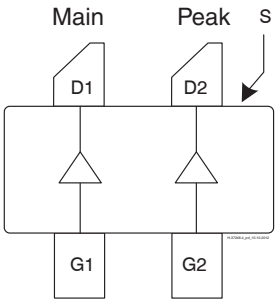
Reference Circuit Assembly

DUT	PXAC182002FC V1
Test Fixture Part No.	LTA/PXAC182002FC V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, ε_r = 3.66, f = 1805 – 1880 MHz
Find Gerber files for this test fixture on the Wolfspeed Web site at www.wolfspeed.com/RF	

Components Information

Component	Description	Manufacturer	P/N
Input			
C101	Capacitor, 1.2 pF	ATC	ATC600F1R2CW250T
C102	Capacitor, 0.5 pF	ATC	ATC600F0R5CW250T
C103, C104, C105, C106	Capacitor, 18 pF	ATC	ATC600F180JW250T
C107, C108	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
R101	Resistor, 50 Ω	Richardson	C8A50Z4A
R102	Resistor, 18 ohms	Panasonic Electronic Components	ERJ-8GEYJ180V
R103, R104	Resistor, 301 Ω	Venkel	CR0603-16W-3010FT
R105, R106	Resistor, 10 Ω	Panasonic Electronic Components	ERJ-3GEYJ100V
S1	Hybrid Coupler	Anaren	X3C19P1-03S
Output			
C201, C207, C215, C218, C219	Capacitor, 18 pF	ATC	ATC600F180JW250T
C202	Capacitor, 0.8 pF	ATC	ATC600F0R8AW250T
C203	Capacitor, 5.1 pF	ATC	ATC600F5R1AW250T
C204	Capacitor, 1.6 pF	ATC	ATC600F1R6AW250T
C205, C217	Capacitor, 220 µF	Cornell Dubilier Electronics	SK221M050ST
C206, C208, C209, C211, C213, C214, C216	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
C210	Capacitor, 0.5 pF	ATC	ATC600F0R5AW250T
C212	Capacitor, 1.6 pF	ATC	ATC600F1R6AW250T

Pinout Diagram (top view)



Pin Description
D1 Drain device 1 (Main)
D2 Drain device 2 (Peak)
G1 Gate device 1 (Main)
G2 Gate device 2 (Peak)
S Source (flange)

Lead connections for PXAC182002FC

Package Outline Specifications

Package H-37248-4

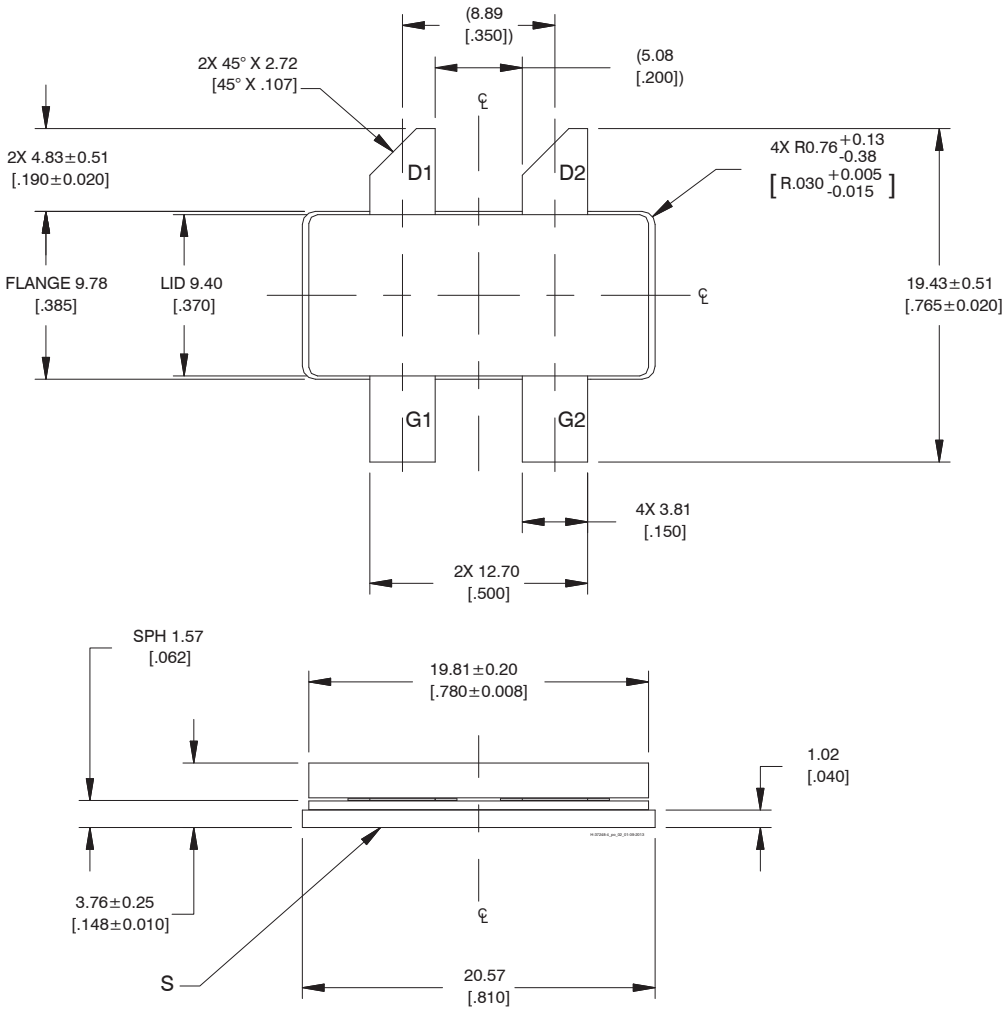


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source.
5. Lead thickness: 0.10 + 0.076/–0.025 mm [0.004+0.003/–0.001 inch].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2014-09-23	Advance	All	Data Sheet reflects advance specification for product development
02	2015-03-24	Production	All All	Data Sheet reflects released product specification Revised all data and includes updated final specs, typical performance graphs, loadpull, reference circuit, package outline
02.1	2015-05-20	Production	1	Updated single-carrier WCDMA test spec
02.2	2015-06-05	Production	1	Corrected I/O in description paragraph, removed f_1 from single-carrier WCDMA test spec condition
02.3	2016-06-17	Production	1, 2	Updated ESD rating and ordering information to include R0
03	2018-06-25	Production	All	Converted to Wolfspeed Data Sheet

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Notes

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