N-channel 600 V, 0.550 Ω typ., 7.5 A MDmesh™ M2 EP Power MOSFET in a TO-220FP package

TO-220FP

D(2)

G(1)

S(3)

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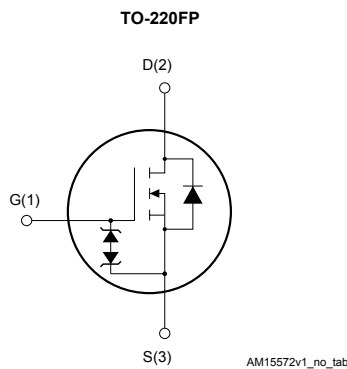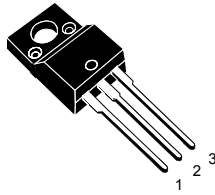
Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF11N60M2-EP	600 V	0.595 Ω	7.5 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 enhanced performance (EP) technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Product status
STF11N60M2-EP

Product summary	
Order code	STF11N60M2-EP
Marking	11N60M2EP
Package	TO-220FP
Packing	Tube

DS11598 - Rev 4 - April 2018
For further information contact your local STMicroelectronics sales office.

www.st.com

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	7.5	A
	Drain current (continuous) at T_C = 100 °C	4.7	A
I_{DM}[1]	Drain current (pulsed)	30	A
P_{TOT}	Total dissipation at T_C = 25 °C	25	W
dv/dt[2]	Peak diode recovery voltage slope	15	V/ns
dv/dt[3]	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width limited by safe operating area.*

2. *$I_{SD} \leq 7.5$ A, di/dt $\leq$ 400 A/µs, $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD} = 400 V*

3. *$V_{DS} \leq 480$ V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2.4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	115	mJ

2   Electrical characteristics

$T_C = 25 \, °C$ unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \, V$, $I_D = 1 \, mA$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0 \, V$, $V_{DS} = 600 \, V$			1	µA
		$V_{GS} = 0 \, V$, $V_{DS} = 600 \, V$, $T_C = 125 \, °C$ [1]			100	µA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0 \, V$, $V_{GS} = ±25 \, V$			±10	µA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \, µA$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 \, V$, $I_D = 3.75 \, A$		0.550	0.595	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100 \, V$, $f = 1 \, MHz$, $V_{GS} = 0 \, V$	-	390	-	pF
C_{oss}	Output capacitance		-	22	-	pF
C_{rss}	Reverse transfer capacitance		-	0.7	-	pF
$C_{oss \, eq.}$ [1]	Equivalent output capacitance	$V_{DS} = 0 \text{ to } 480 \, V$, $V_{GS} = 0 \, V$	-	49	-	pF
R_G	Intrinsic gate resistance	$f = 1 \, MHz$, $I_D = 0 \, A$	-	9	-	Ω
Q_g	Total gate charge	$V_{DD} = 480 \, V$, $I_D = 7.5 \, A$, $V_{GS} = 0 \text{ to } 10 \, V$ (see Figure 15. Test circuit for gate charge behavior)	-	12.4	-	nC
Q_{gs}	Gate-source charge		-	2.1	-	nC
Q_{gd}	Gate-drain charge		-	6	-	nC

1. $C_{oss \, eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% V_{GS} to 0% I_D)	$V_{DD} = 400 \, V$, $I_D = 1 \, A$, $R_G = 4.7 \, Ω$, $V_{GS} = 10 \, V$	-	2.5	-	µJ
		$V_{DD} = 400 \, V$, $I_D = 3 \, A$, $R_G = 4.7 \, Ω$, $V_{GS} = 10 \, V$	-	9	-	µJ

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 3.75 A,	-	9	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	5.5	-	ns
$t_{d(off)}$	Turn-off-delay time	(see Figure 14. Test circuit for resistive load switching times and	-	26	-	ns
t_f	Fall time	Figure 19. Switching time waveform)	-	8	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7.5	A
I_{SDM} [1]	Source-drain current (pulsed)		-		30	A
V_{SD} [2]	Forward on voltage	V_{GS} = 0 V, I_{SD} = 7.5 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 7.5 A, di/dt = 100 A/μs,	-	192		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	1.32		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	13.8		A
t_{rr}	Reverse recovery time	I_{SD} = 7.5 A, di/dt = 100 A/μs,	-	262		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C	-	1.74		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	13.3		A

1. *Pulse width is limited by safe operating area*
2. *Pulsed: pulse duration = 300 μs, duty cycle 1.5%*

2.1 Electrical characteristics curves

Figure 1. Safe operating area
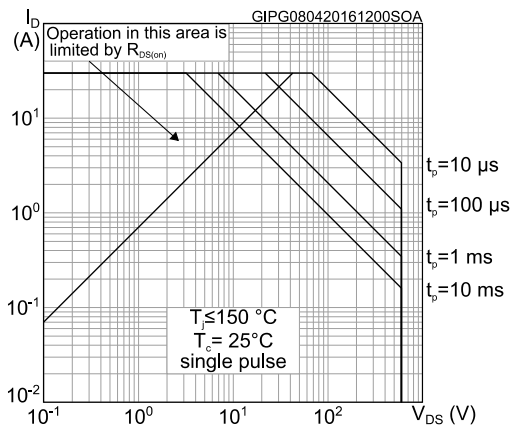
Figure 2. Thermal impedance
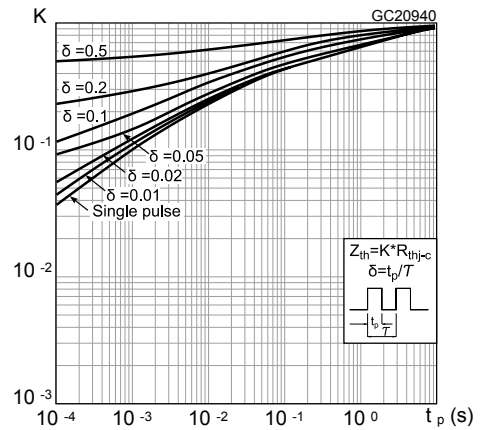
Figure 3. Output characteristics
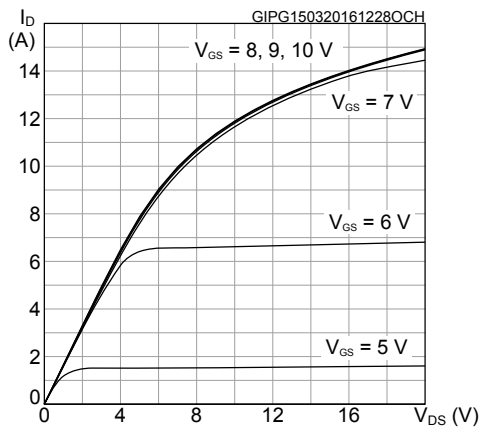
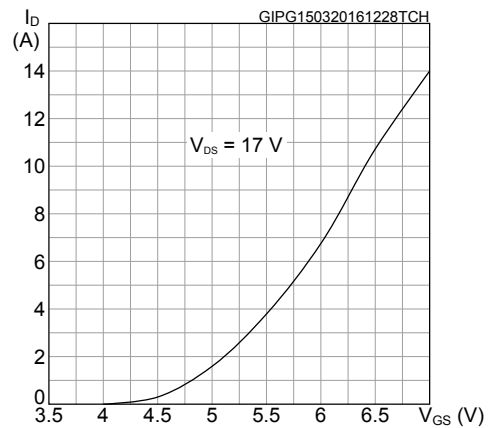**Figure 4. Transfer characteristics**

Figure 5. Gate charge vs gate-source voltage
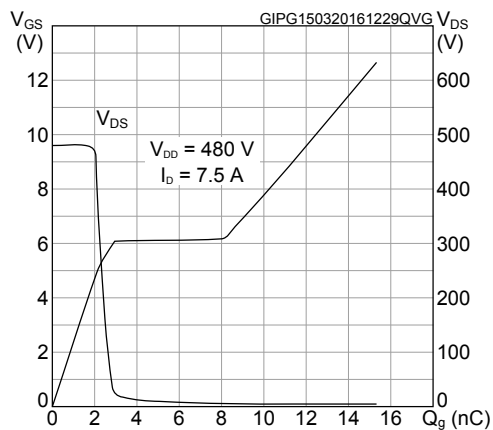
Figure 6. Static drain-source on-resistance

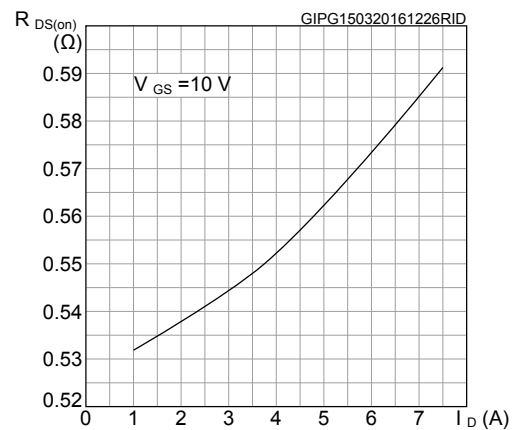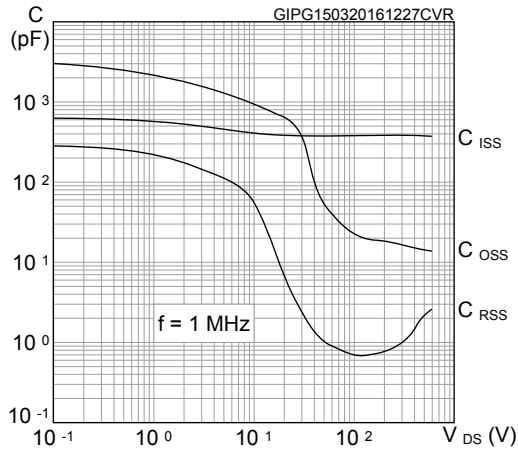**Figure 7. Capacitance variations**

GIPG150320161227CVR

C (pF)

C_{ISS}
C_{OSS}
C_{RSS}

f = 1 MHz

V_{DS} (V)

Figure 8. Turn-off switching energy vs drain current

GIPG160320160901ALS

E_{off} [µJ]

V_{DD} = 400 V
R_G = 4.7 Ω
V_{GS} = 10 V

I_d [A]
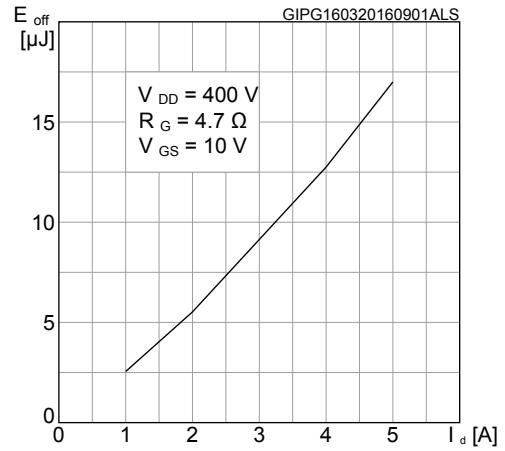
Figure 9. Normalized gate threshold voltage vs temperature

GIPG181120141615ALS

$V_{GS(th)}$ (norm)

I_D = 250 µA

T_J (°C)
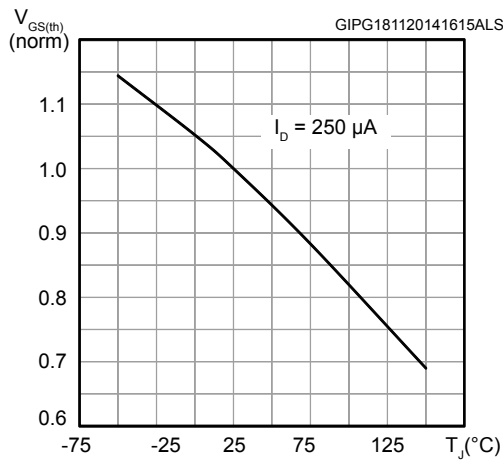
Figure 10. Normalized on-resistance vs temperature

GIPG181120141628ALS

$R_{DS(on)}$ (norm)

V_{GS} = 10 V

T_J (°C)
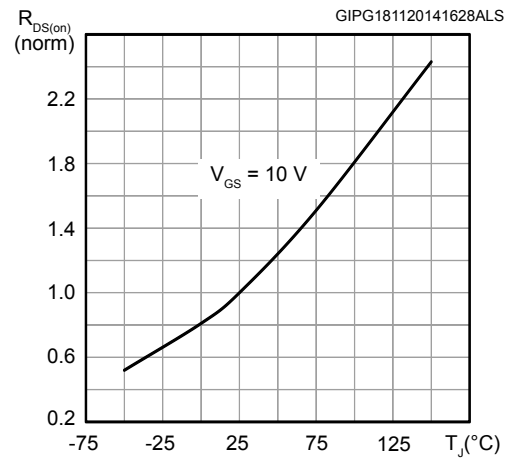
Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

GIPG191120141457ALS

$V_{(BR)DSS}$ (norm)

I_D = 1mA

T_J (°C)
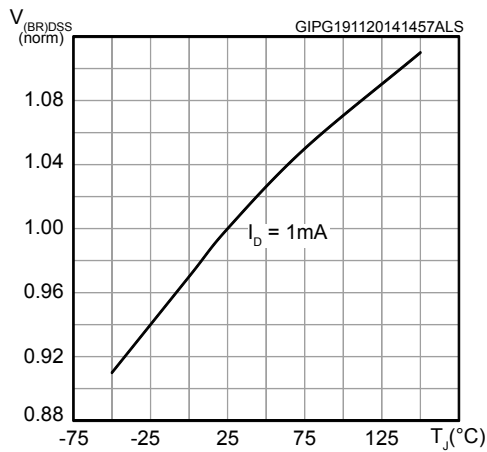
Figure 12. Output capacitance stored energy

GIPG150320161230EOS

E_{OSS} (µJ)

V_{DS} (V)
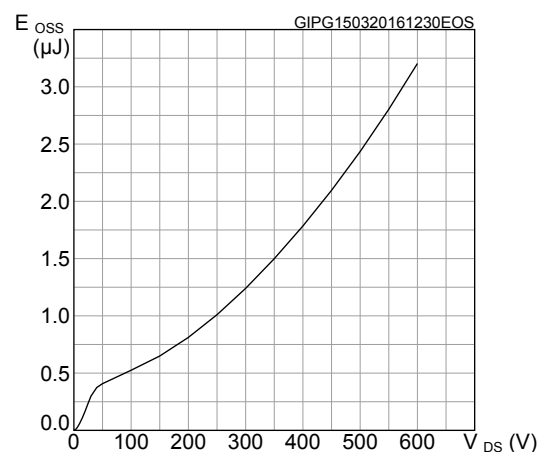
Figure 13. **Source-drain diode forward characteristics**
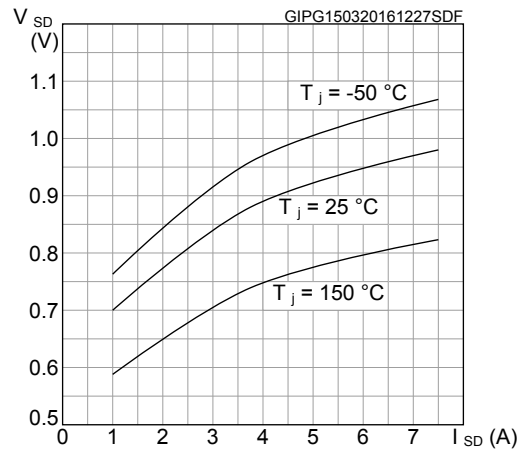
3 Test circuits

Figure 14. Test circuit for resistive load switching times
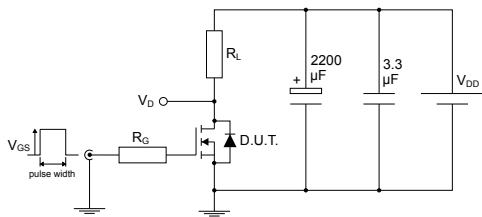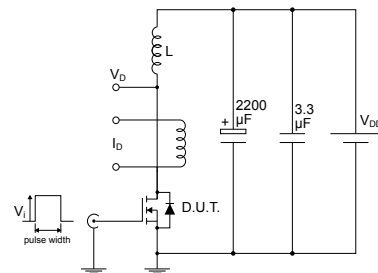

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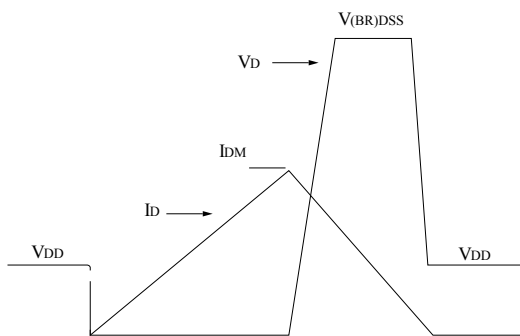**Figure 15. Test circuit for gate charge behavior**
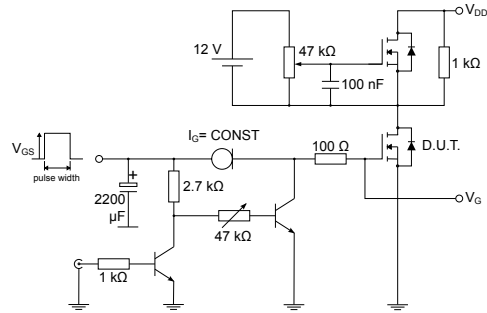
AM01469v1

Figure 16. Test circuit for inductive load switching and diode recovery times
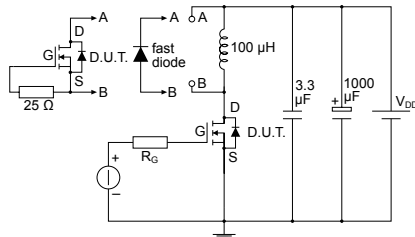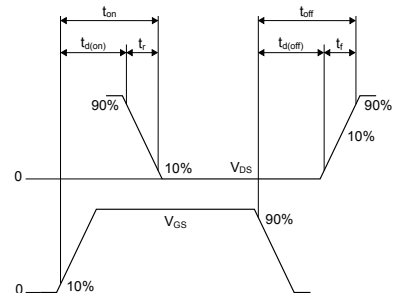

AM01470v1

Figure 17. Unclamped inductive load test circuit

AM01471v1

Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform

AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 20. TO-220FP package outline
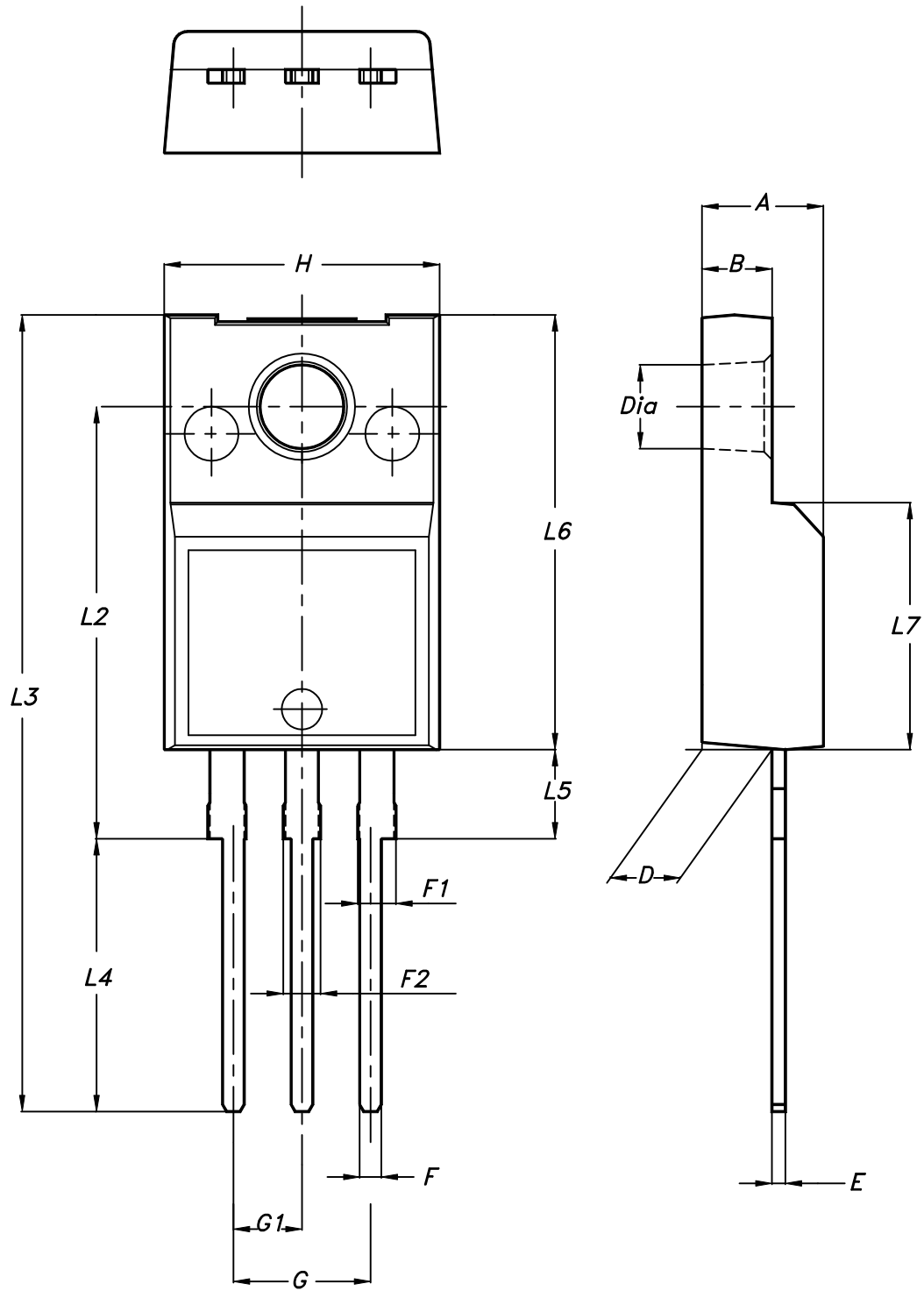
7012510_Rev_12_B

Table 9. TO-220FP package mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 10. Document revision history

Date	Revision	Changes
11-Apr-2016	1	First release.
07-Oct-2016	2	Document status changed from preliminary to production data.
02-Mar-2018	3	Removed document maturity status from cover page. Updated *Table 1. Absolute maximum ratings, Table 4. On/off states, Table 5. Dynamic* and *Table 8. Source drain diode.* Updated *Figure 1. Safe operating area, Figure 3. Output characteristics, Figure 4. Transfer characteristics* and *Figure 5. Gate charge vs gate-source voltage.* Minor text changes
23-Apr-2018	4	Modified Table 1. Absolute maximum ratings, Table 5. Dynamic and Table 8. Source drain diode. Modified Figure 1. Safe operating area. Minor text changes.

Contents

IMPORTANT NOTICE – PLEASE READ CAREFULLY