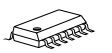
Multifunctional Voltage Regulator and Watchdog TLE 6363

Data Sheet

Overview



P-DSO-14-2

Features

- Step up converter (Boost Voltage)
- Boost Over- and Under-Voltage-Lockout
- Step down converter (Logic Voltage)
- 2% output voltage tolerance
- Logic Over- and Under-Voltage-Lockout
- Overtemperature Shutdown
- Power ON/OFF reset generator
- Digital window watchdog
- System Enable Output
- Ambient operation temperature range – 40 °C to 125 °C
- Wide Supply voltage operation range
- Very low current consumption
- Very small P-DSO-14-2 SMD package

Type	Ordering Code	Package
TLE 6363 G	Q67006-A9601	P-DSO-14-2

Functional Description

General

The **TLE 6363 G** is a multifunctional power supply circuit especially designed for automotive applications.
It delivers a programmable step up voltage (Boost) and a precise 5 V fully short circuit protected output voltage (Buck).
The **TLE 6363 G** contains a power on reset feature to start up the system, an integrated digital window watchdog to monitor the connected microcontroller and a system enable output to indicate the microcontroller window watchdog faults.
The device is based on Infineon's power technology SPT® which allows bipolar and CMOS control circuitry to be integrated with DMOS power devices on the same monolithic circuitry.
The very small **P-DSO-14-2** SMD packages meet the application requirements.

Furthermore, the build-in features like under- and overvoltage lockout for boost- and buck-voltage and the overtemperature shutdown feature increase the reliability of the **TLE 6363 G** supply system.

Pin Definitions and Functions

Pin No. SO-14	Symbol	Function
1	R	**Reference Input**; an external resistor from this pin to GND determines the reference current and the oscillator frequency
2	RO	**Reset Output**; open drain output from reset comparator with an internal pull up resistor
3	WDI	**Watchdog Input**; input for the watchdog control signal from the controller
4	GND	**Ground**; analog signal ground
5	SEN	**System Enable Output**; open drain output from Watchdog fail-circuit with an internal pull up resistor
6	BUC	**Buck-Converter Compensation Input**; output of internal error amplifier; for loop-compensation connect an external R-C-series combination to GND
7	V_{CC}	**Supply Voltage Output**; buck converter output; external blocking capacitor necessary
8	BUO	**Buck Converter Output**; source of the integrated power-DMOS
9	V_{BOOST}	**Boost Converter Input**; input supply voltage of the IC; coming from the boost converter output voltage; buck converter input voltage
10	BDS	**Buck Driver Supply Input**; voltage to drive the buck converter powerstage
11	OVL	**Boost Status Output**; open drain output from boost PWM comparator
12	BOFB	**Boost Converter Feedback Input**; connect boost voltage divider to this pin; internal reference is the boost feedback threshold V_{BOFBTH}
13	BOGND	**Boost-Ground**; power signal ground; source of boost converter power-DMOS
14	BOI	**Boost Converter Input**; drain of the integrated buck converter power-DMOS

Pin Configuration

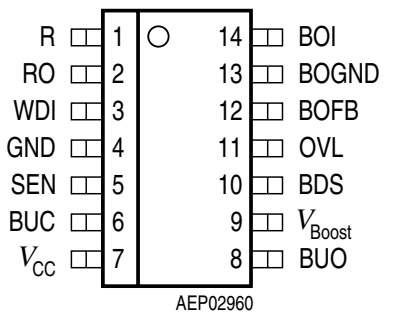


Figure 1 **Pin Configuration** (top view)

Block Diagram

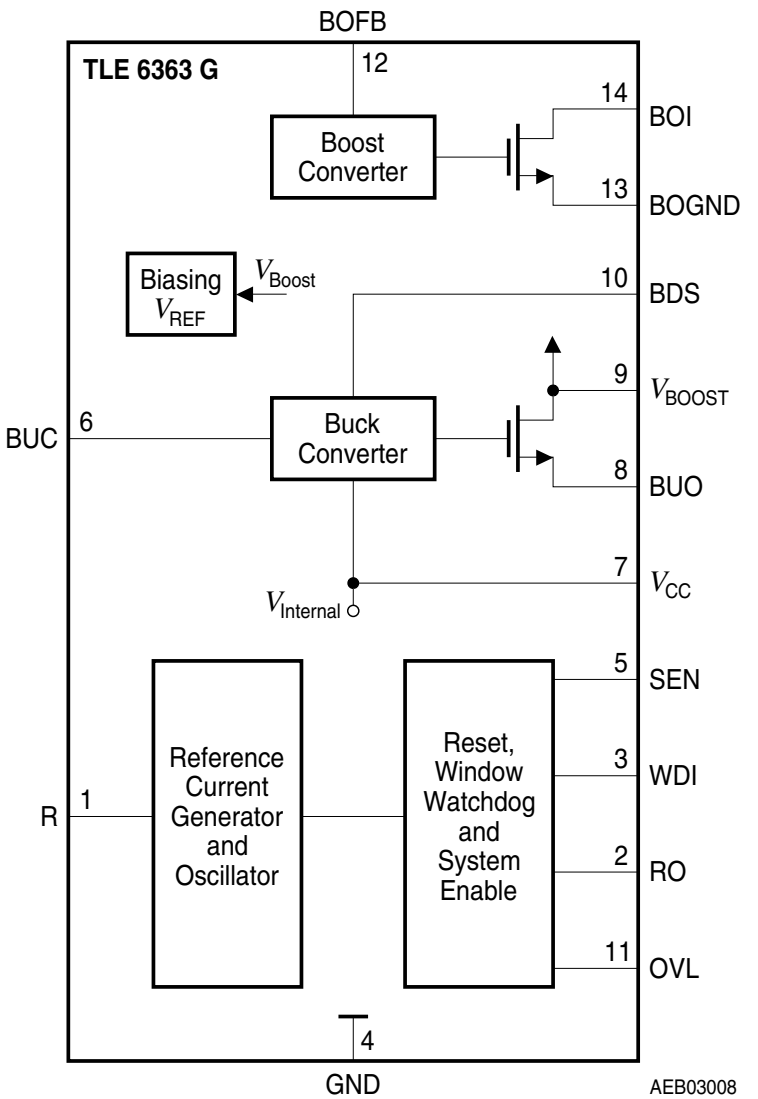


Figure 2 Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Boost input voltage	V_{BOI}	– 0.3	46	V	–
Boost output voltage	V_{BOOST}	– 0.3	46	V	–
Boost feedback voltage	V_{BOFB}	– 0.3	46	V	–
Buck output voltage	V_{BUO}	– 1	46	V	–
Buck driver supply voltage	V_{BDS}	– 0.3	48	V	–
Buck compensation input voltage	V_{BUC}	– 0.3	6.8	V	–
Logic supply voltage	V_{CC}	– 0.3	6.8	V	–
Reset output voltage	V_{RO}	– 0.3	6.8	V	–
System Enable output voltage	V_{SEN}	– 0.3	6.8	V	–
Current reference voltage	V_{R}	– 0.3	6.8	V	–
Watchdog input voltage	V_{WDI}	– 0.3	6.8	V	–
OVL output voltage	V_{OVL}	– 0.3	6.8	V	–
ESD-Protection (Human Body Model; R = 1.5 kΩ; C = 100 pF)					
All pins to GND	V_{HBM}	– 2	2	kV	–
Temperatures					
Junction temperature	T_{j}	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Boost input voltage	V_{BOI}	– 0.3	40	V	–
Boost input voltage; (normal operation)	V_{BOOST}	5	35	V	V_{BOOST} increasing
Boost input voltage; (normal operation)	V_{BOOST}	4.5	36	V	V_{BOOST} decreasing
Boost input voltage	V_{BOOST}	– 0.3	4.5	V	Boost- and Buck-Converter OFF
Boost feedback voltage	V_{BOFB}	0	3.0	V	–
Buck output voltage	V_{BUO}	– 0.6	40	V	–
Buck driver supply voltage	V_{BDS}	– 0.3	48	V	–
Buck compensation input voltage	V_{BUC}	0	3.0	V	–
Logic supply voltage	V_{CC}	4.00	6.25	V	–
Reset output voltage	V_{RO}	– 0.3	V_{CC} + 0.3	V	–
System Enable output voltage	V_{SEN}	– 0.3	V_{CC} + 0.3	V	–
Watchdog input voltage	V_{WDI}	0	V_{CC} + 0.3	V	–
Current reference voltage	V_R	0	3.0	V	–
Junction temperature	T_j	– 40	150	°C	–

Thermal Resistance

Junction ambient	R_{thj-a}	–	120	K/W	–

Note: In the operating range, the functions given in the circuit description are fulfilled.

Electrical Characteristics

8 V < V_{Boost} < 35 V; 4.75 V < V_{CC} < 5.25 V; – 40 °C < T_j < 150 °C; R_R = 47 kΩ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Current Consumption						
Current consumption; see application circuit	I_{Boost}	–	1.5	4	mA	I_{CC} = 0 mA; I_{BoLoad} = 0 mA
Current consumption; see application circuit	I_{Boost}	–	5	10	mA	I_{CC} = 200 mA; I_{BoLoad} = 50 mA
Under- and Over-Voltage Lockout at V_{Boost}						
UV ON voltage; boost and buck conv. ON	V_{BOUVON}	4.0	4.5	5.0	V	V_{BOOST} increasing;
UV OFF voltage; boost and buck conv. OFF	$V_{BOUVOFF}$	3.5	4.0	4.5	V	V_{BOOST} decreasing
UV Hysteresis voltage	V_{BOUVHY}	0.2	0.5	1.0	V	HY = ON - OFF
OV OFF voltage; boost conv. OFF	$V_{BOOVOFF}$	34	37	40	V	V_{BOOST} increasing
OV ON voltage; boost conv. ON	V_{BOOVON}	30	33	36	V	V_{BOOST} decreasing
OV Hysteresis voltage	V_{BOUVHY}	1.5	4	10	V	HY = OFF - ON
Over-Voltage Lockout at V_{CC}						
OV OFF voltage; buck conv. OFF	$V_{BUOVOFF}$	5.5	6.0	6.5	V	V_{CC} increasing
OV ON voltage; buck conv. ON	V_{BUOVON}	5.25	5.75	6.25	V	V_{CC} decreasing
OV Hysteresis voltage	V_{BUOVHY}	0.10	0.25	0.50	V	HY = OFF - ON

Electrical Characteristics (cont'd)

8 V < V_{Boost} < 35 V; 4.75 V < V_{CC} < 5.25 V; – 40 °C < T_j < 150 °C; R_R = 47 kΩ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Boost-Converter; BOI, BOFB and V_{BOOST}						
Boost voltage; see application circuit	V_{BOOST}	24.0	27.5	31.0	V	5 mA < I_{Boost} < 100 mA; T_j = 25 °C 8 V < V_{Batt} < 16 V
Boost Voltage; see application circuit	V_{BOOST}	23	–	32	V	5 mA < I_{Boost} < 100 mA; 8 V < V_{Batt} < 16 V
Efficiency; see. appl. circuit	η	–	80	–	%	I_{Boost} = 100 mA
Power-Stage ON resistance	R_{BOON}	–	0.6	0.75	Ω	T_j = 25 °C; I_{BOI} = 1 A
Power-Stage ON resistance	R_{BOON}	–	–	1.4	Ω	I_{BOI} = 1 A
Boost overcurrent threshold	I_{BOOC}	1.0	1.3	1.8	A	–
Feedback threshold voltage	V_{BOFBTH}	2.55	2.7	2.85	V	V_{BOI} = 12 V I_{Boost} = 25 mA
Feedback input current	I_{FB}	– 2	– 0.4	0	µA	2 V < V_{BOFB}< 4 V
Buck-Converter; BUO, BDS, BUC and V_{CC}						
Logic supply voltage	V_{CC}	4.9	–	5.1	V	1 mA < I_{CC} < 250 mA; see. appl. circuit
Efficiency; see. appl. circuit	η	–	85	–	%	I_{CC} = 250 mA; V_{Boost} = 25 V
Power-Stage ON resistance	R_{BUON}	–	0.38	0.5	Ω	T_j = 25 °C; I_{BUO} = 1 A
Power-Stage ON resistance	R_{BUON}	–	–	1.0	Ω	I_{BUO} = 1 A
Buck overcurrent threshold	I_{BUOC}	0.7	0.95	1.2	A	–
Input current on pin V_{CC}	I_{CC}	–	0.2	0.5	mA	V_{CC} = 5 V

Electrical Characteristics (cont'd)

8 V < V_{Boost} < 35 V; 4.75 V < V_{CC} < 5.25 V; – 40 °C < T_j < 150 °C; R_R = 47 kΩ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Buck Gate supply voltage; $V_{BGS} = V_{BDS} - V_{BUO}$	V_{BGS}	5	–	10	V	–

Reference Input; R
(Oscillator; Timebase for Boost- and Buck-Converter, Reset and Watchdog)

Voltage on pin R	V_R	1.3	1.4	1.5	V	–
Oscillator frequency	f_{OSC}	85	95	105	kHz	T_j = 25 °C
Oscillator frequency	f_{OSC}	75	–	115	kHz	–
Cycle time for watchdog and reset timing	t_{CYL}	–	1.05	–	ms	$t_{CYL} = 100/f_{OSC}$

Reset Generator; RO

Reset threshold; V_{CC} decreasing/increasing	V_{RT}	4.50	4.65	4.75	V	V_{RO} H to L or L to H transition; V_{RO} remains low down to V_{CC} > 1 V
Reset low voltage	V_{ROL}	–	0.2	0.4	V	I_{ROL} = 2 mA; 2.5 V < V_{CC} < V_{RT}
Reset low voltage	V_{ROL}	–	0.2	0.4	V	I_{ROL} = 0.2 mA; 1 V < V_{CC} < V_{RT}
Reset high voltage	V_{ROH}	V_{CC} – 0.1	–	V_{CC} + 0.1	V	I_{ROH} = 0 mA
Reset pull up current	I_{RO}	–	240	–	µA	0 V < V_{RO} < 4 V
Reset Reaction time	t_{RR}	50	100	150	µs	V_{CC} < V_{RT}
Power-up reset delay time	t_{RD}	–	64	–	t_{CYL}	V_{CC} ≥ 4.8 V

Electrical Characteristics (cont'd)

8 V < V_{Boost} < 35 V; 4.75 V < V_{CC} < 5.25 V; – 40 °C < T_j < 150 °C; R_R = 47 kΩ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Watchdog Generator; WDI						
H-input voltage threshold	V_{WDIH}	–	–	0.7 × V_{CC}	V	–
L-input voltage threshold	V_{WDIL}	0.3 × V_{CC}	–	–	V	–
Watchdog period	T_{WD}	–	128	–	t_{CYL}	V_{CC} ≥ 4.8 V
Start of reset; after watchdog time-out	t_{SR}	–	64	–	t_{CYL}	V_{CC} ≥ 4.8 V
Reset duration; after watchdog time-out	t_{WDR}	–	64	–	t_{CYL}	V_{CC} ≥ 4.8 V
Open window time	t_{OW}	–	32	–	t_{CYL}	V_{CC} ≥ 4.8 V
Closed window time	t_{CW}	–	32	–	t_{CYL}	V_{CC} ≥ 4.8 V
Window watchdog trigger time	t_{WD}	–	46.4	–	t_{CYL}	V_{CC} ≥ 4.8 V
System Enable Output; SEN						
Enable low voltage	V_{SENL}	–	0.2	0.4	V	I_{SENL} = 2 mA; 2.5 V < V_{CC} < V_{RT}
Enable low voltage	V_{SENL}	–	0.2	0.4	V	I_{SENL} = 0.2 mA; 1 V < V_{CC} < V_{RT}
Enable high voltage	V_{SENH}	V_{CC} – 0.1	–	V_{CC} + 0.1	V	I_{SENH} = 0 mA
Enable pull up current	I_{SEN}	–	240	–	µA	0 V < V_{SEN} < 4 V

Electrical Characteristics (cont'd)

8 V < V_{Boost} < 35 V; 4.75 V < V_{CC} < 5.25 V; – 40 °C < T_j < 150 °C; R_R = 47 kΩ; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Boost Status Output; OVL						
Enable low voltage	V_{OVLL}	–	0.2	0.4	V	I_{OVLL} = 1 mA; 2.5 V < V_{CC} < V_{RT}
Boost feedback threshold voltage;	V_{OVLTH}	2.3	2.45	2.6	V	See application circuit
Thermal Shutdown (Boost and Buck-Converter OFF)						
Thermal shutdown junction temperature	T_{jSD}	150	175	200	°C	–
Thermal switch-on junction temperature	T_{jSO}	120	–	170	°C	–
Temperature hysteresis	ΔT	–	30	–	K	–

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Circuit Description

Below some important sections of the **TLE 6363** are described in more detail.

Power On Reset

In order to avoid any system failure, a sequence of several conditions has to be passed. In case of V_{CC} power down ($V_{CC} < V_{RT}$ for $t > t_{RR}$) a logic LOW signal is generated at the pin RO to reset an external microcontroller. When the level of V_{CC} reaches the reset threshold V_{RT}, the signal at RO remains LOW for the Power-up reset delay time t_{RD} before switching to HIGH. If V_{CC} drops below the reset threshold V_{RT} for a time extending the reset reaction time t_{RR}, the reset circuit is activated and a power down sequence of period t_{RD} is initiated. The reset reaction time t_{RR} avoids wrong triggering caused by short “glitches” on the V_{CC}-line.

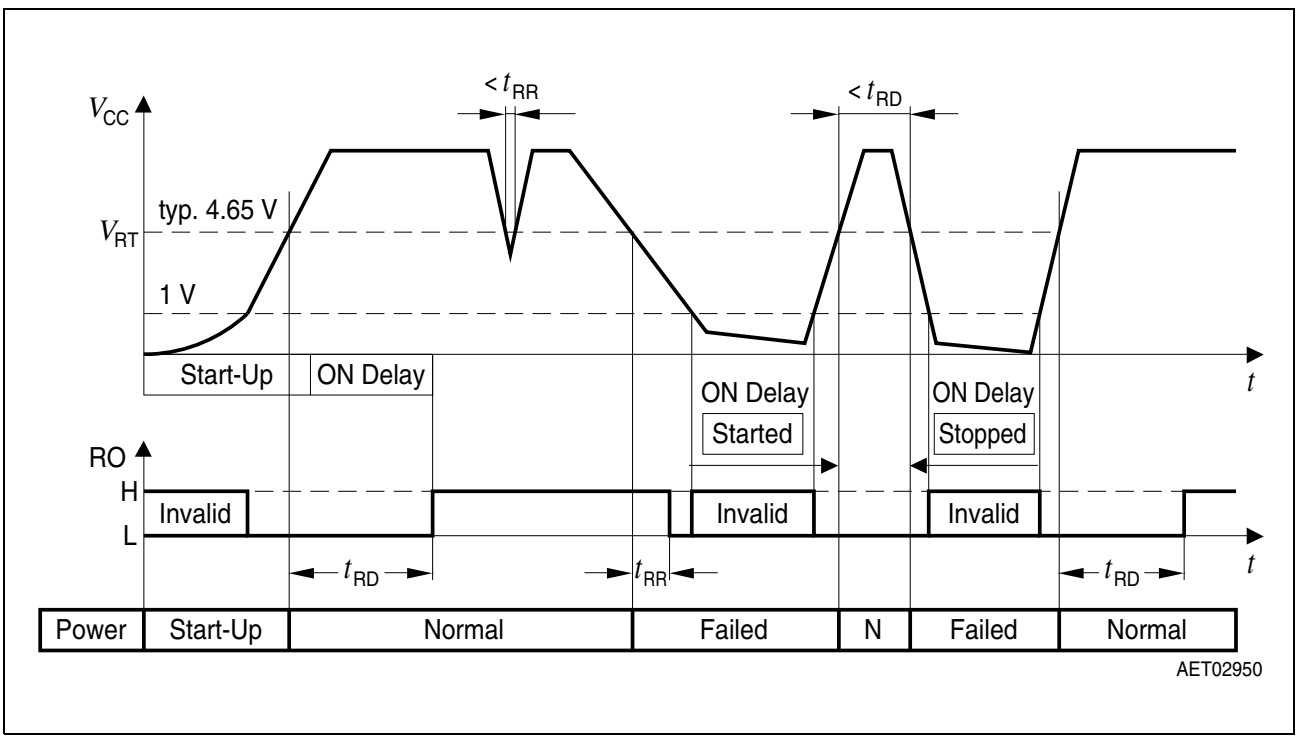


Figure 3 Reset Function

Watchdog Operation

The watchdog uses one hundred of the oscillator's clock signal period as a timebase, defined as the watchdog cycle time t_{CYL}.
After power-on, the reset output signal at the RO pin (microcontroller reset) is kept LOW for the reset delay time t_{RD}, i.e. 64 cycles. With the LOW to HIGH transition of the signal at RO the device starts the closed window time t_{CW} = 32 cycles. A trigger signal within this window is interpreted as a pretrigger failure according to the figures shown below. After the closed window the open window with the duration t_{OW} is started. The open window lasts at minimum until the trigger process has occurred, at maximum t_{OW} is 32 cycles.
A HIGH to LOW transition of the watchdog trigger signal on pin WDI is taken by a trigger. To avoid wrong triggering due to parasitic glitches two HIGH samples followed by two LOW samples (sample period t_{CYL}) are decoded as a valid trigger. If a trigger signal appears at the watchdog input pin WDI during the open window or a power up/down occurs, the watchdog window signal is reset and a new closed window follows.
A reset is generated (RO goes LOW) if there is no trigger pulse during the open window or if a pretrigger occurs during the closed window. This reset happens after 64 cycles after the latest valid closed window start time and lasts for further 64 cycles.
The triggering is correct also, if the first three samples (two HIGH one LOW) of the trigger pulse at pin WDI are inside the closed window and only the fourth sample (the second LOW sample) is taken in the open window.
In addition to the microcontroller reset signal RO the device generates a system enable signal at pin SEN. If RO is HIGH the system enable goes active HIGH with the first valid watchdog trigger pulse at pin WDI. The SEN output goes LOW immediately if a pretrigger, a missing trigger or a power down reset occurs.

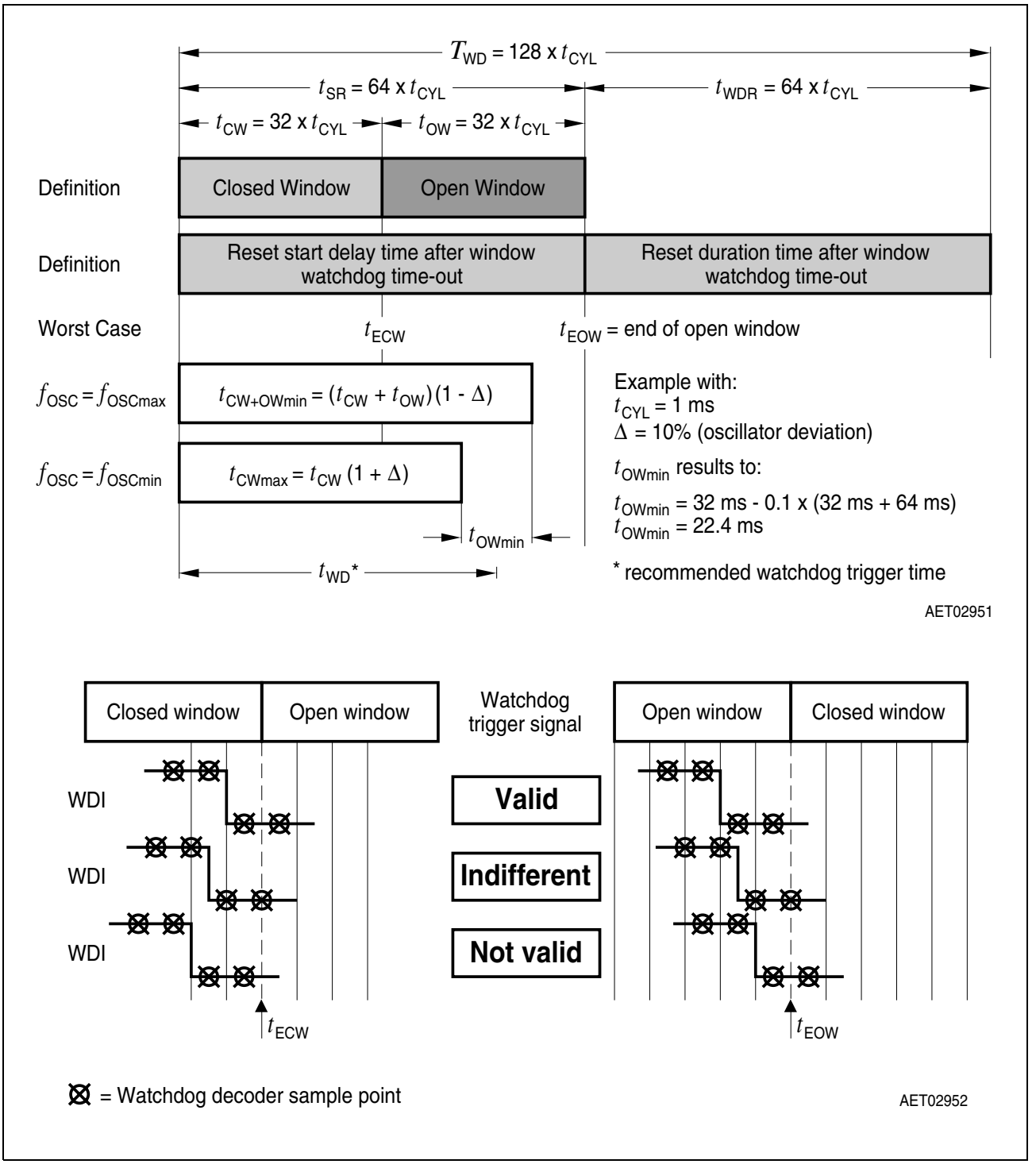
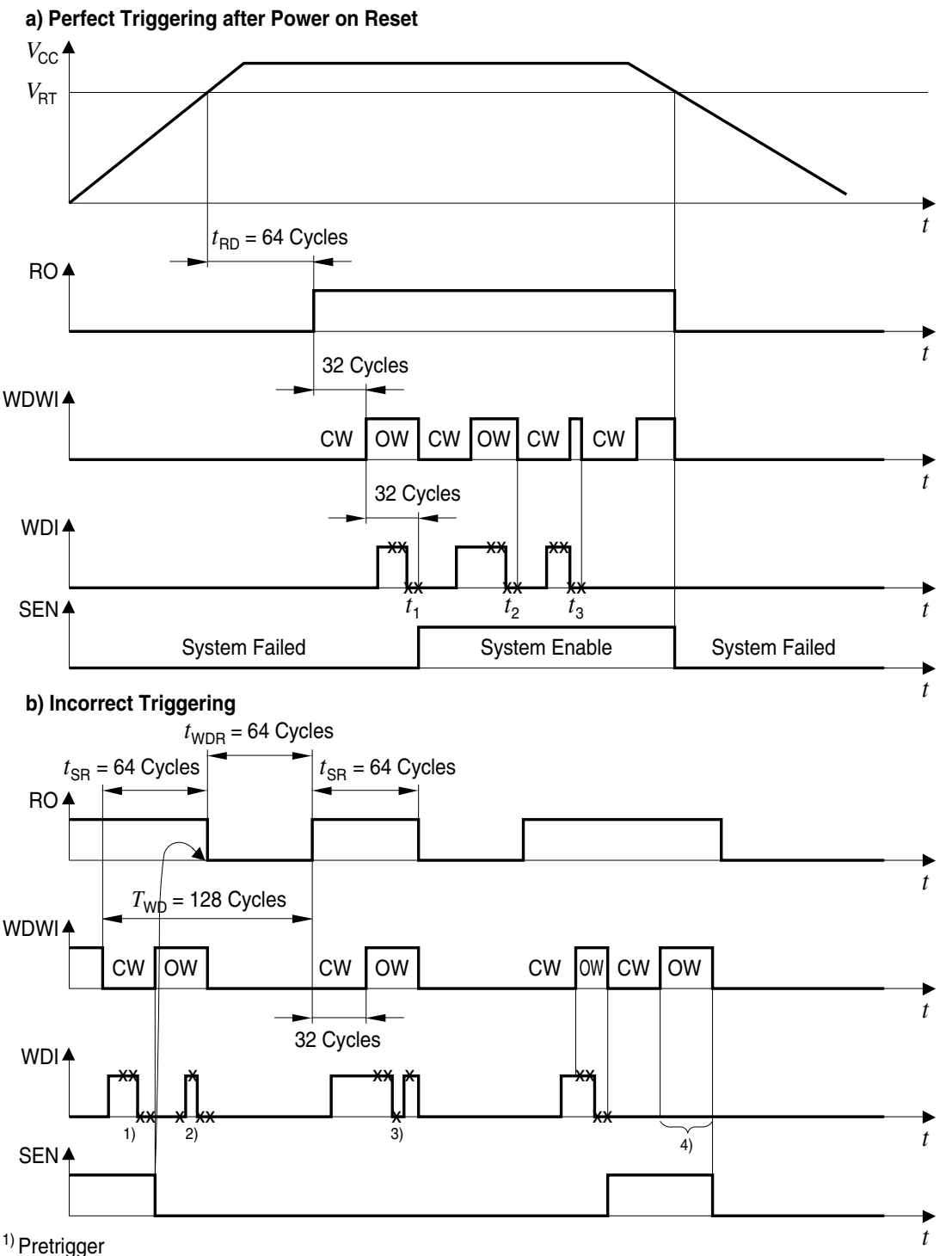


Figure 4 Window Watchdog Definitions



1) Pretrigger
2) Incorrect trigger duration within watchdog open window OW: t_{HIGH} < 2 Cycles
3) Incorrect trigger duration within watchdog open window OW: t_{LOW} < 2 Cycles
4) Missing trigger

Legend: WDWI = Internal Watchdog Window
OW = Open Window (trigger signal at WDI)
CW = Closed Window (trigger signal at WDI)
x = Sample Point

AED02945

Figure 5 Window Watchdog Function

Boost Converter

The TLE 6363 contains a fully integrated boost converter (except the boost-diode), which provides a supply voltage for an energy reserve e.g. an airbag firing system. The regulated boost output voltage V_{BOOST} is programmable by a divider network (external resistors) providing the feedback voltage for the boost feedback pin BOFB. The energy which is stored in the external electrolytic capacitor at V_{BOOST} guarantees accurate airbag firing, even if the battery is disconnected by a car crash.

The boost inductance L_{BO} (typ. 100 µH) is PWM-switched by an integrated current limited power DMOS transistor with a programmable (external resistor R_R) frequency. An internal bandgap reference provides a temperature independent, on chip trimmed reference voltage for the regulation loop. An error amplifier compares the reference voltage with the boost feedback signal V_{BOFB} from the external divider network (determination of the output boost voltage V_{BOOST}).

Application note for programming the output voltage at pin V_{BOOST}:

$$V_{BOOST} = V_{BOFBTH} \times \frac{(R_{BO1} + R_{BO2})}{R_{BO2}}$$

With a PWM (Pulse Width Modulation) comparator the output of the error amplifier is compared to a periodic linear ramp, provided by a sawtooth signal of the oscillator connected to pin R. A logic signal with variable pulse width is generated. It passes through the logic circuits (sets the output latch PWM-FF) and driver circuits to the power switching DMOS. The Schmitt-trigger output resets the output flip-flop PWM-FF by NOR 2. The PWM signal is gated by the NAND 2 to guarantee a dominant reset.

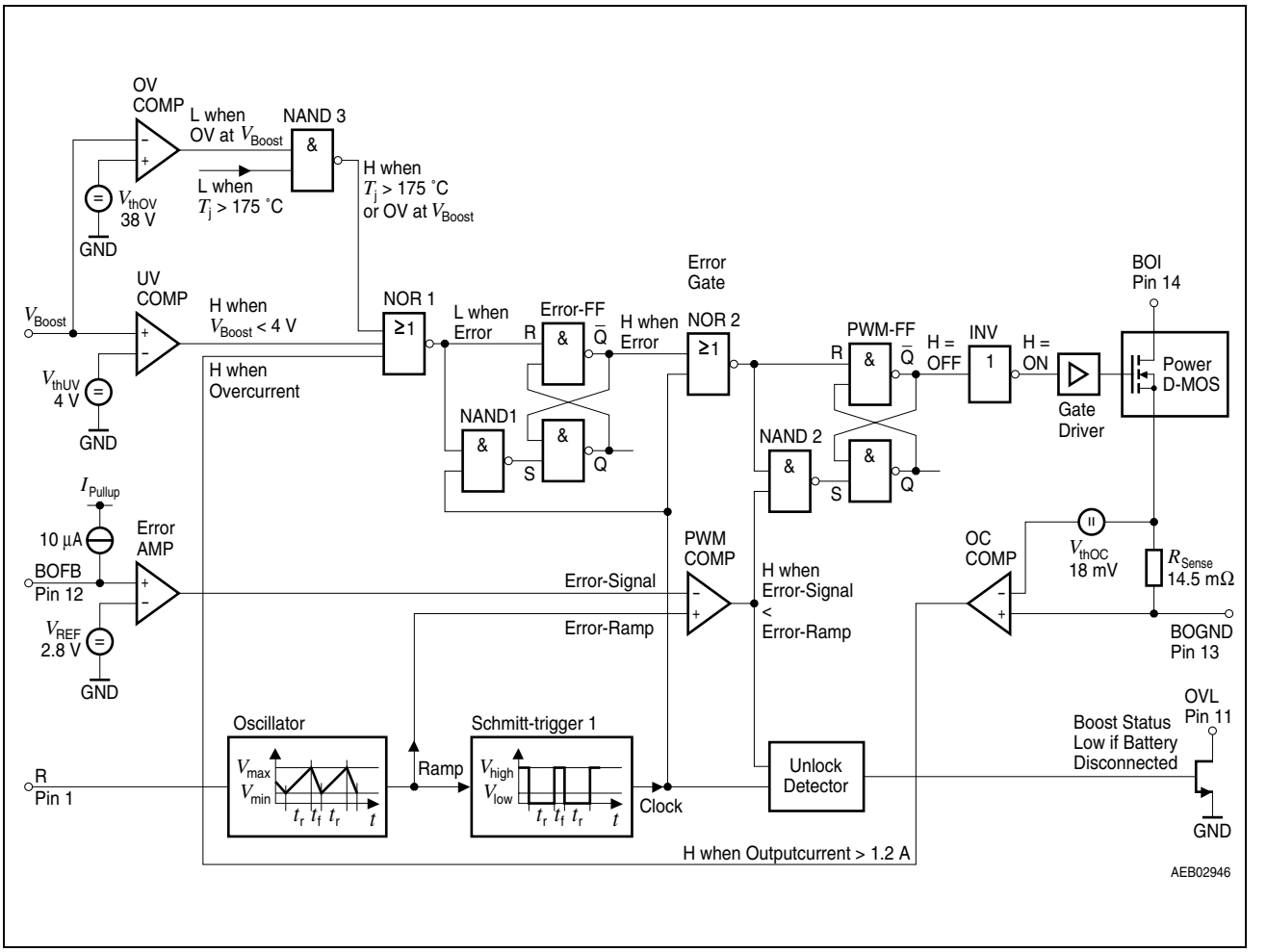


Figure 6 Boost Converter Block Diagram

Figure 7 shows the most important waveforms during operation; for low, medium and high loads up to overload condition. The output transistor is switched off immediately if the overcurrent comparator detects an overcurrent level at the power DMOS or if the sense output switches to low induced by a V_{BOOST} undervoltage command.

The **TLE 6363** is also protected against several boost loop errors:
In case of a feedback interruption a pull up current source (I_{FB} typ. 0.4 µA), integrated at pin BOFB pulls the voltage at the feedback pin BOFB above the reference voltage. The boost output is switched off by the high error voltage which controls the PWM-Comparator at a zero duty cycle.
In the case of a resistive loop error caused by leakage currents to ground, the boost output voltage would increase to very high values. In order to protect the V_{BOOST} input as well as the external load against catastrophic failures, an overvoltage protection is provided which switches the output transistor off as soon as the voltage at pin V_{BOOST} exceeds the internal fixed overvoltage threshold $V_{BOOVOFF}$ = typ. 37 V.

Application Note:

A short circuit from V_{BOOST} to ground will not destroy the IC, however, it may damage the external boost diode or the boost inductance if there is no overcurrent limitation in that path.

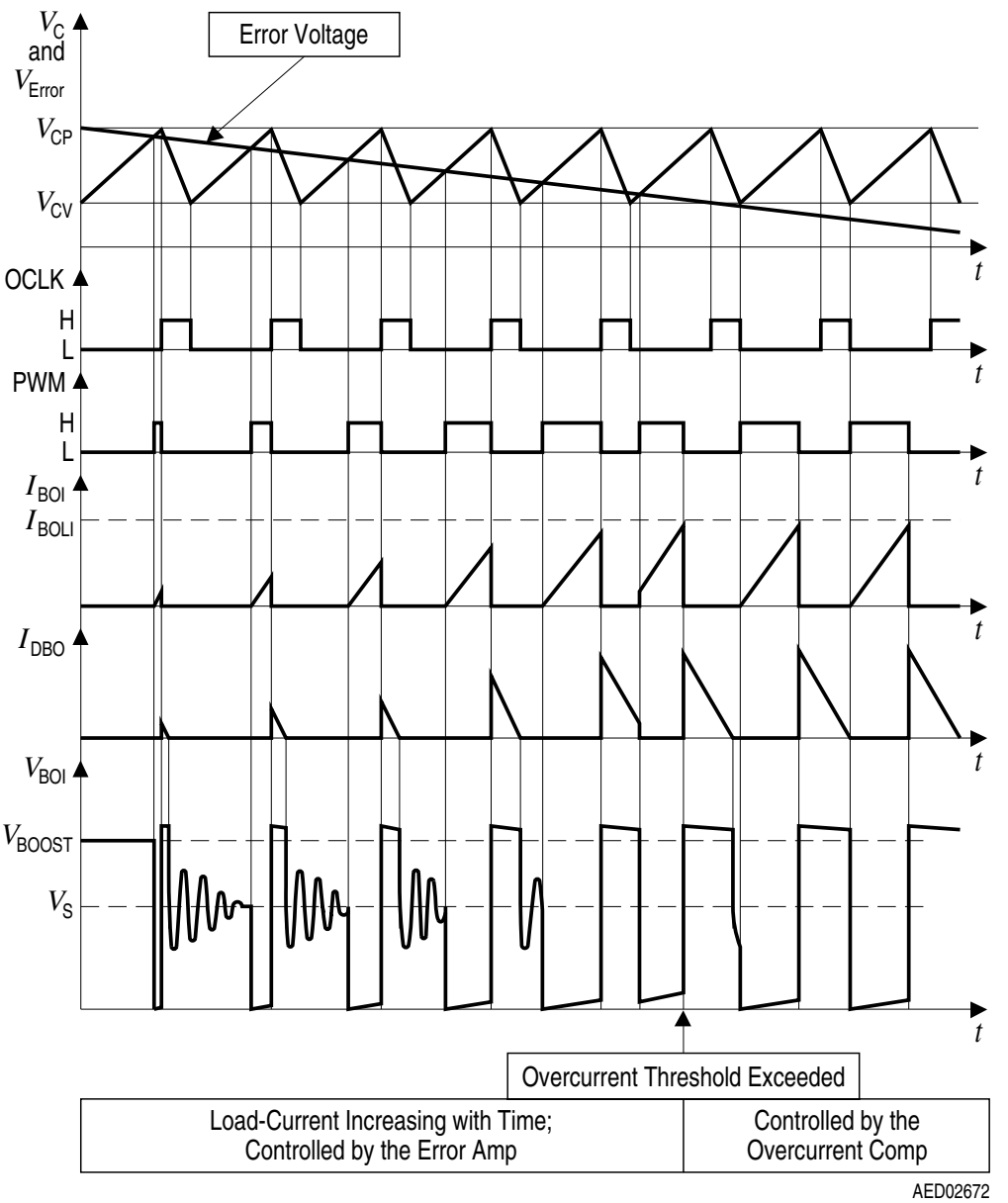


Figure 7 Most Important Waveforms of the Boost Converter Circuit

Buck Converter

A stabilized logic supply voltage (typ. 5 V) for general purpose is realized in the system by a buck converter. An external buck-inductance L_{BU} is PWM switched by a high side DMOS power transistor with the programmed frequency (pin R).

The buck regulator supply is given by the boost converter output V_{BOOST}, in case of a battery power-down the stored energy of the boost converter capacitor is used.

Like the boost converter, the buck converter uses the temperature compensated bandgap reference voltage (typ. 2.8 V) for its regulation loop.
This reference voltage is connected to the non-inverting input of the error amplifier and an internal voltage divider supplies the inverting input. Therefore the output voltage V_{CC} is fixed due to the internal resistor ratio to typ. 5.0 V.
The output of the error amplifier goes to the inverting input of the PWM comparator as well as to the buck compensation output BUC.
When the error amplifier output voltage exceeds the sawtooth voltage the output power MOS-transistor is switched on. So the duration of the output transistor conduction phase depends on the V_{CC} level. A logic signal PWM with variable pulse width is generated.

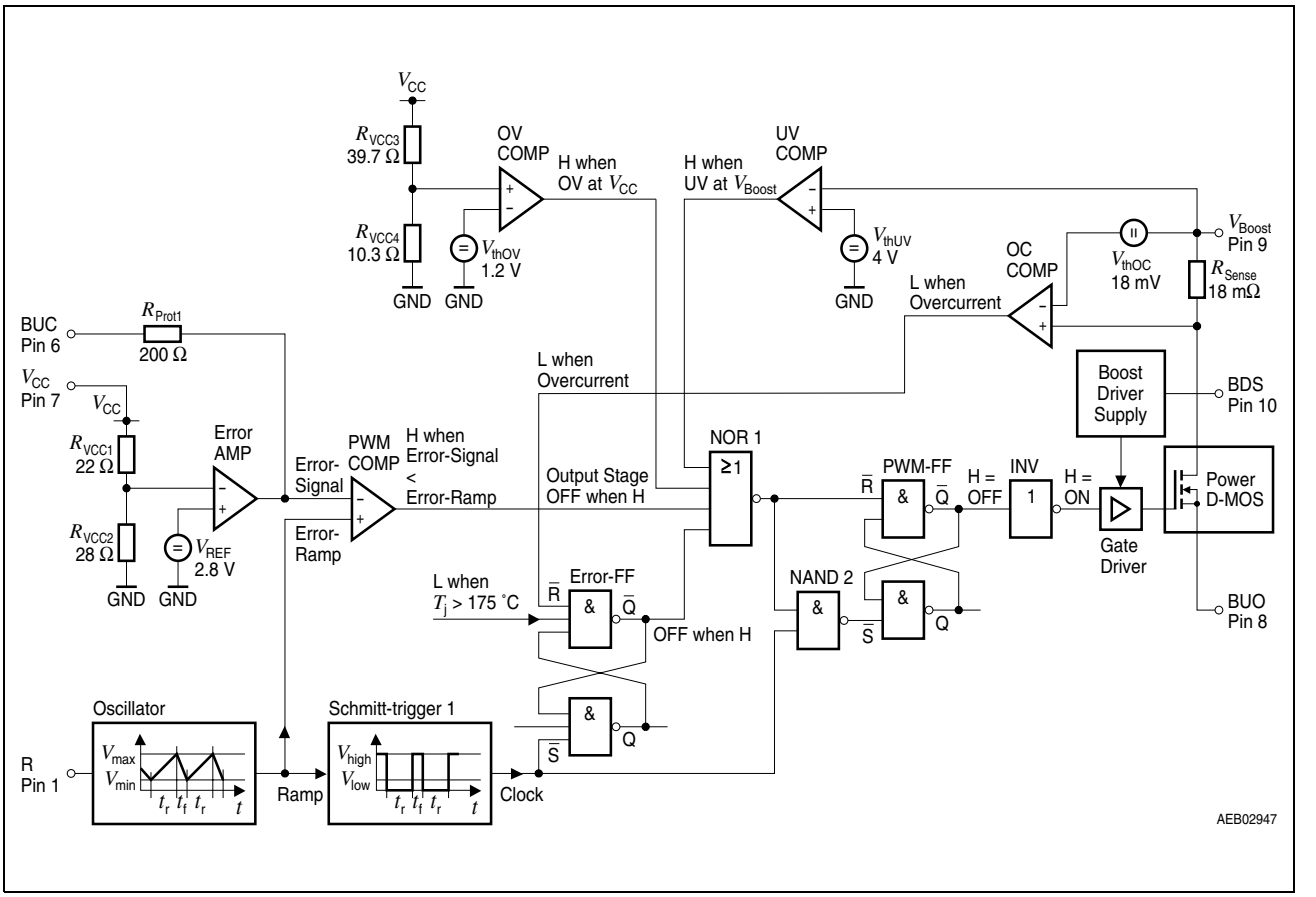


Figure 8 Buck Converter Block Diagram

External loop compensation is required for converter stability, and is formed by connecting a compensation resistor-capacitor series-network (R_{BUC}, C_{BUC}) between pin BUC and GND.

In the case of overload or short-circuit at V_{CC} (the output current exceeds the buck overcurrent threshold I_{BUOC}) the DMOS output transistor is switched off by the overcurrent comparator immediately. The pulse width is then controlled by the overcurrent comparator as seen before in the boost description.

In order to protect the V_{CC} input as well as the external load against catastrophic failures, an overvoltage protection is provided which switches the output transistor off as soon as the voltage at pin V_{CC} exceeds the internal fixed overvoltage threshold $V_{BUOVOFF}$ = typ. 6.0 V.

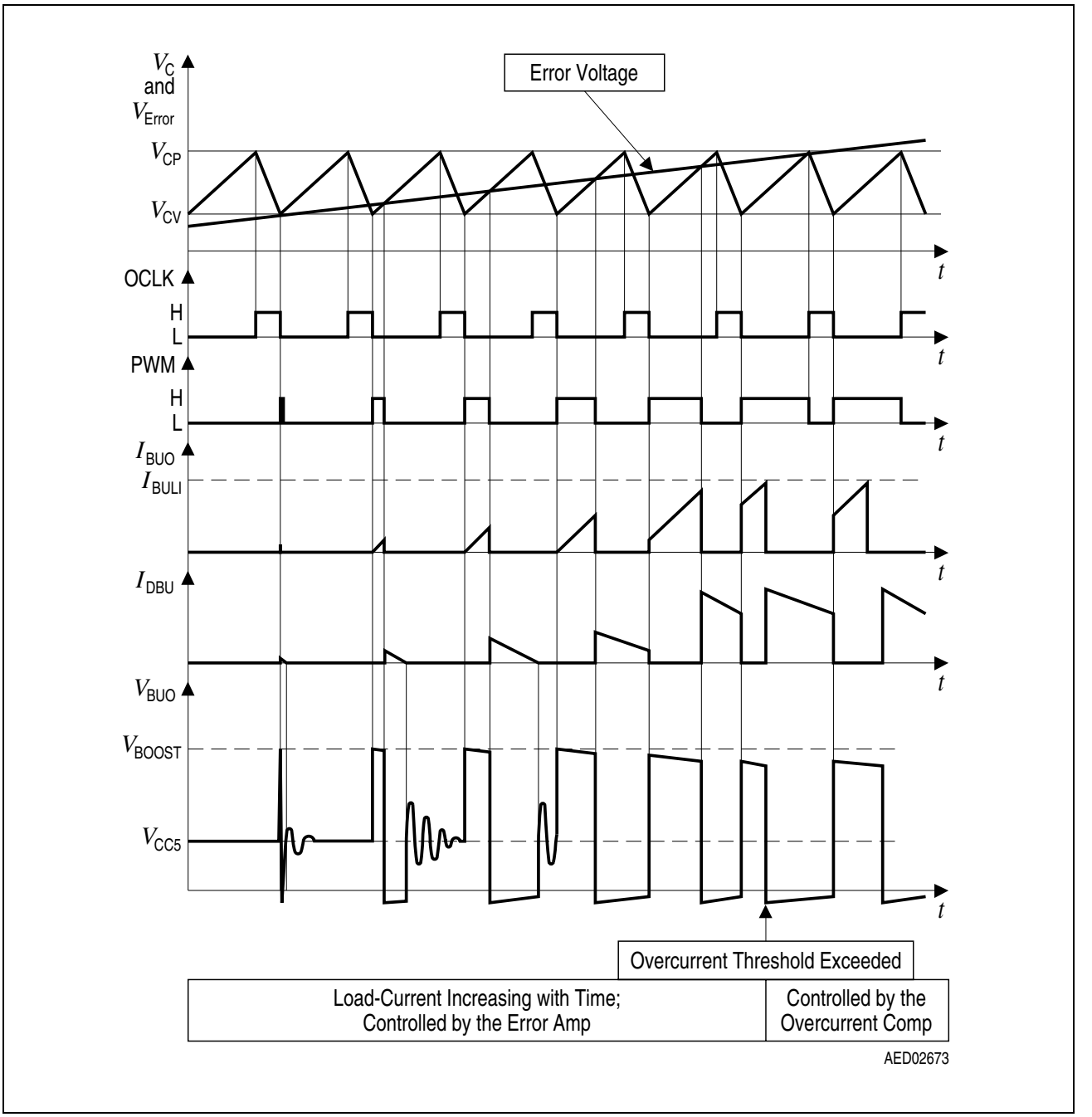
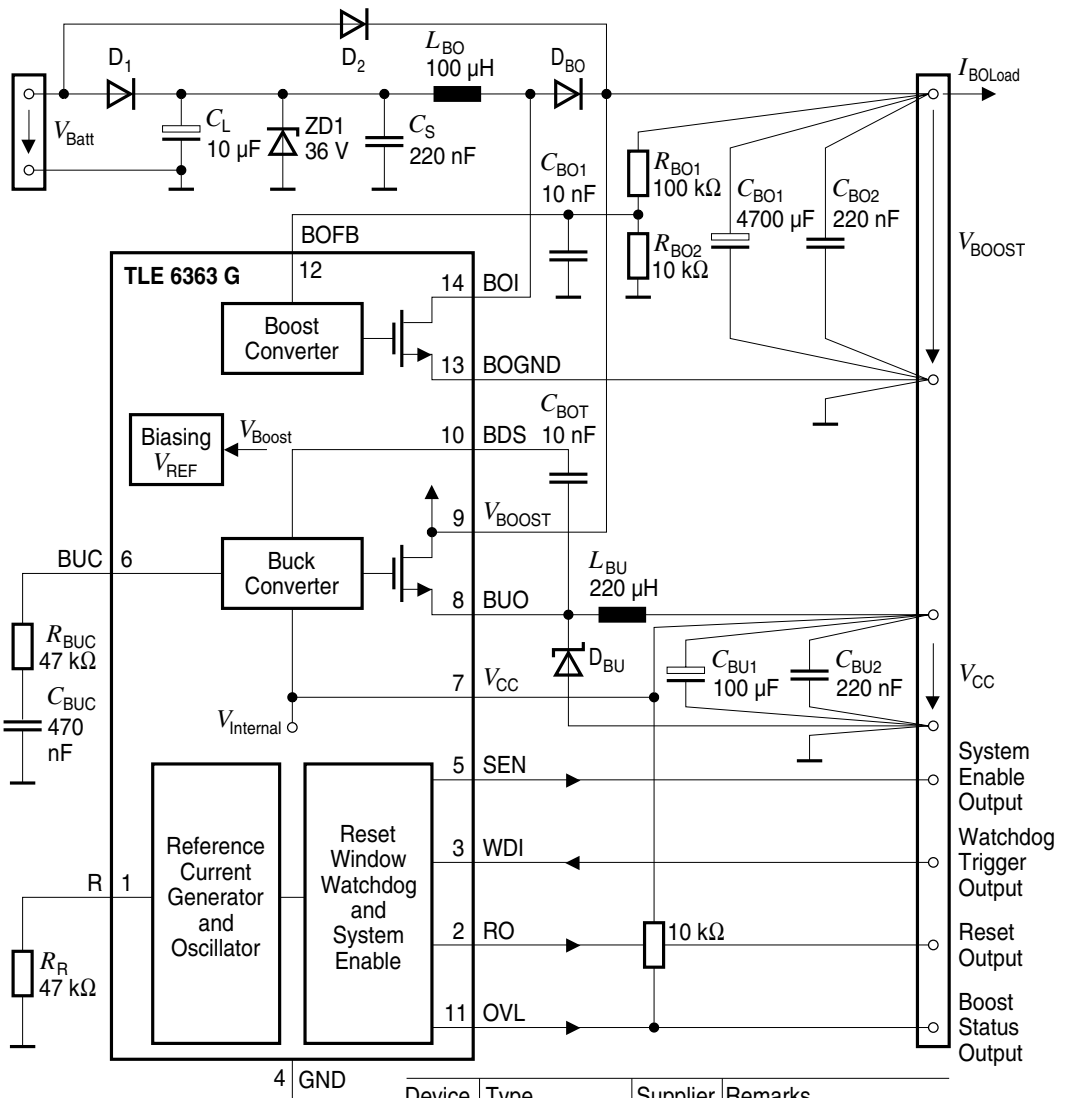


Figure 9 Most Important Waveforms of the Buck Converter Circuit

Application Circuit

Figure 10 shows the application circuit of the **TLE 6363** with the suggested external parts.



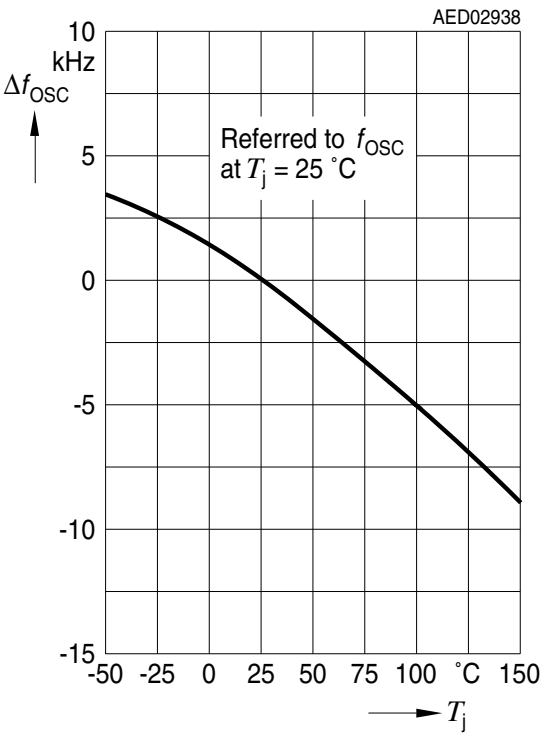
Device	Type	Supplier	Remarks
D_1	BAW78C	Infineon	200 V; 1 A; SOT-89
D_2	BAW78C	Infineon	200 V; 1 A; SOT-89
D_{BO}	BAW78B	Infineon	100 V; 1 A; SOT-89
D_{BO}	SS14	multiple	Schottky; 40 V; 1 A
D_{BU}	-	-	Schottky; 100 V; 1 A
L_{BO}	B82442-A1104	EPCOS	100 µH; 0.25 A; 1.28 Ω
L_{BO}	Do3316P-104	Coilcraft	100 µH; 1.2 A; 0.28 Ω
L_{BU}	B82442-H2204	EPCOS	220 µH; 0.24 A; 2.72 Ω
L_{BU}	Do3316P-224	Coilcraft	220 µH; 0.8 A; 0.61 Ω

Figure 10 Application Circuit

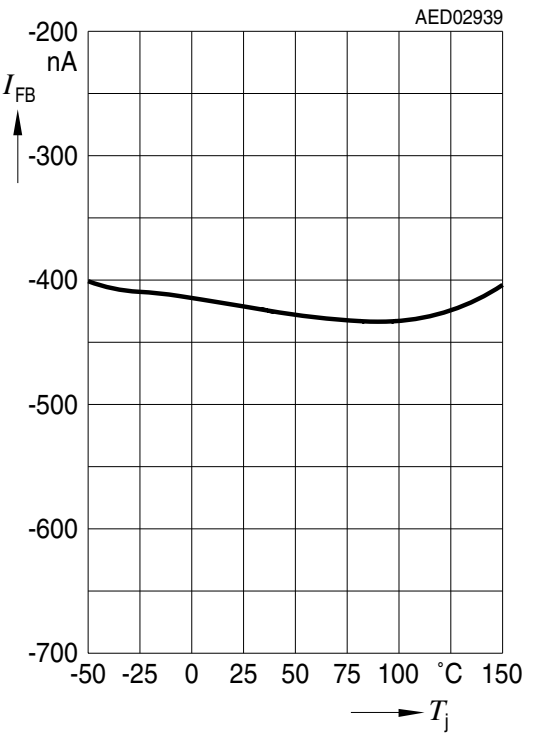
Diagrams: Oscillator and Boost/Buck-Converter Performance

In the following the behaviour of the Boost/Buck-converter and the oscillator is shown.

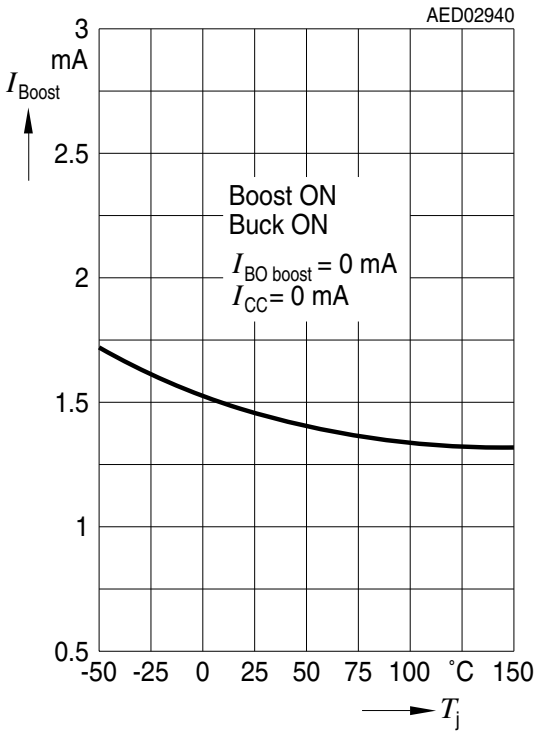
Oscillator Frequency Deviation vs. Junction Temperature



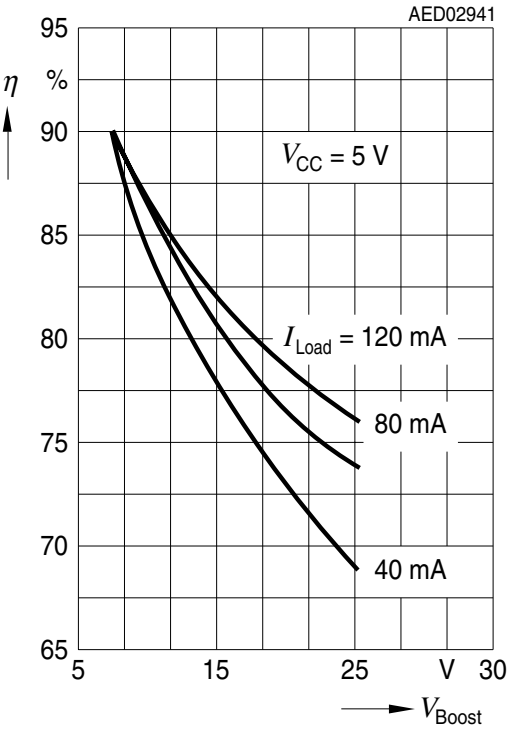
Boost Feedback Current vs. Junction Temperature



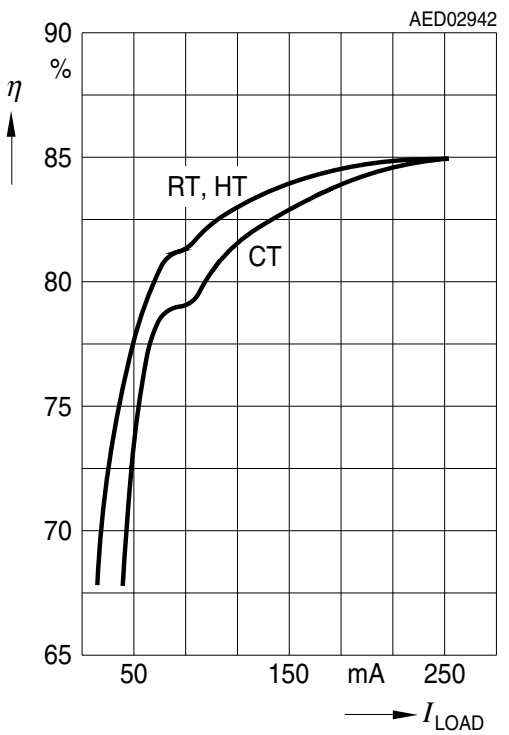
Current Consumption vs. Junction Temperature



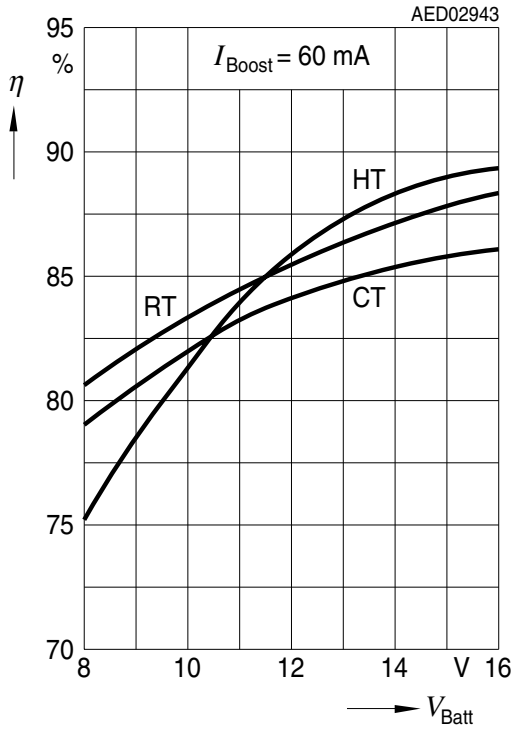
Efficiency Buck vs. Boost Voltage



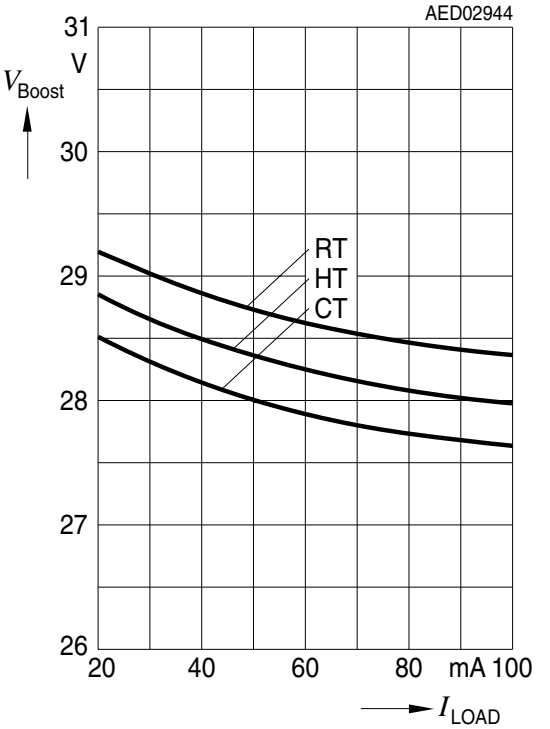
Efficiency Buck vs. Load



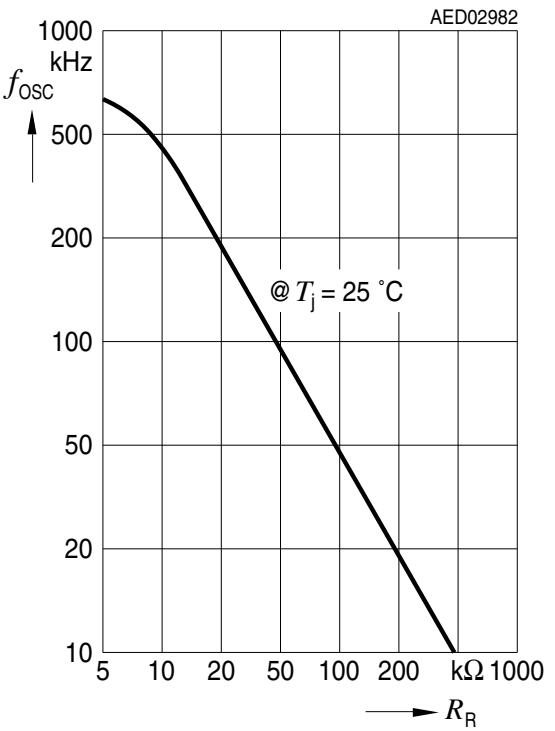
Efficiency Boost vs. Input Voltage



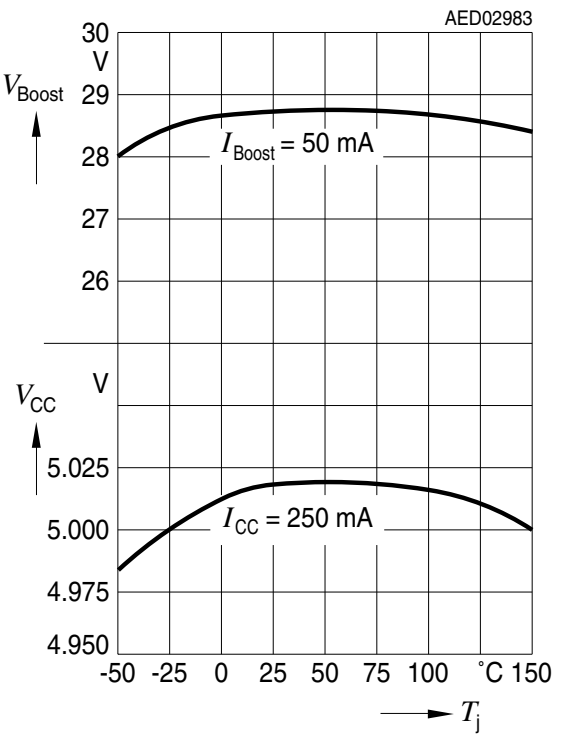
Boost Output Voltage vs. Load



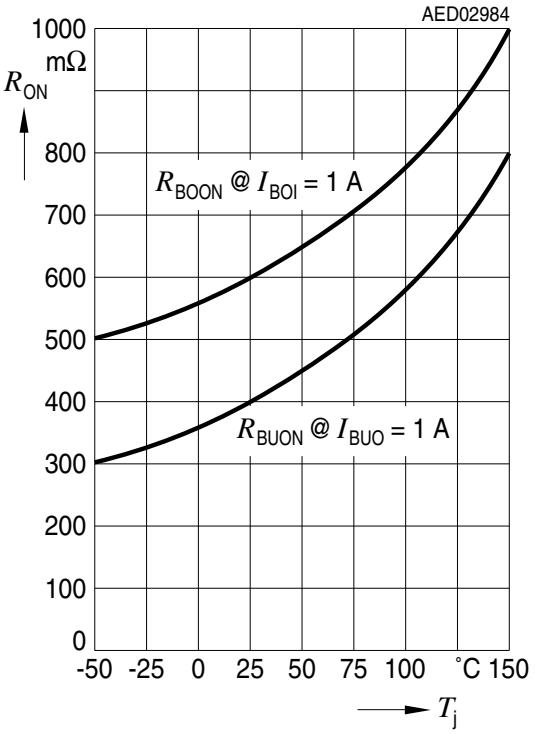
Oscillator Frequency vs. Resistor from R to GND



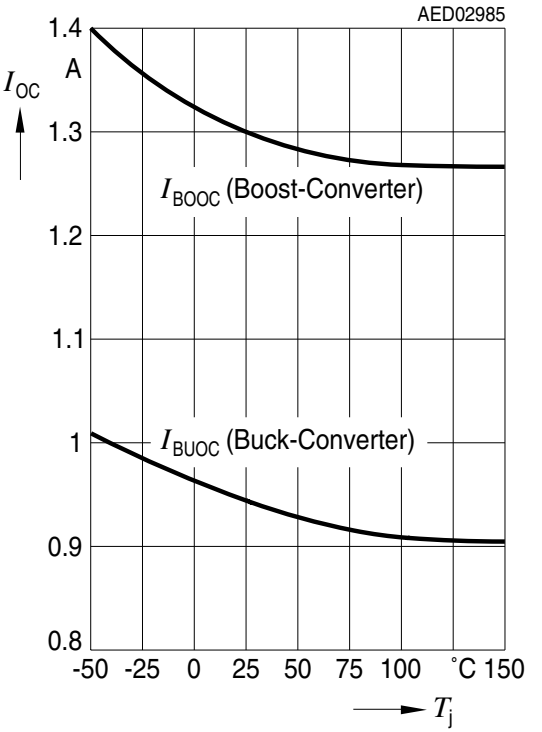
Boost and Logic Output Voltage vs. Junction Temperature



Boost and Buck ON Resistance vs. Junction Temperature

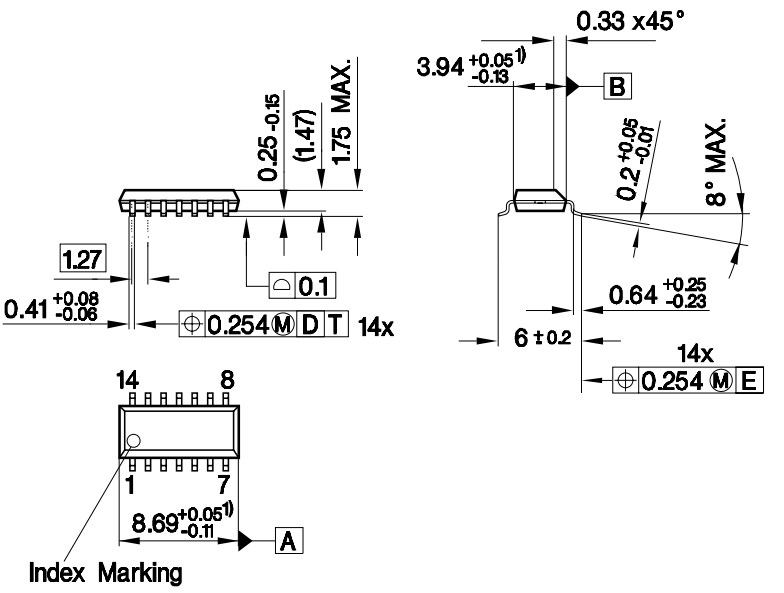


Boost and Buck Overcurrent Threshold vs. Junction Temperature



Package Outlines

P-DSO-14-2
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS05474

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm

Edition 2003-06-02

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