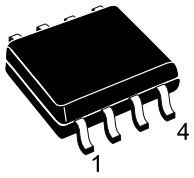
VN751S

High-side driver

Datasheet - production data



SO-8

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN751S	60 mΩ	2.5 A	36 V

- CMOS compatible input
- Thermal shutdown
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low standby current
- Compliance to 61000-4-4 IEC test up to 4 kV
- Open drain status output

Description

The VN751S is a monolithic device developed using STMicroelectronics' VIPower technology, intended to drive any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes. Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device automatically turns off in case of ground pin disconnection. This device is especially suitable for industrial applications in conformity with IEC 61131-2 programmable controller international standard.

Table 1: Device summary

Order code	Package	Packing
VN751S	PowerSO-8	Tube
VN751STR		Tape and reel

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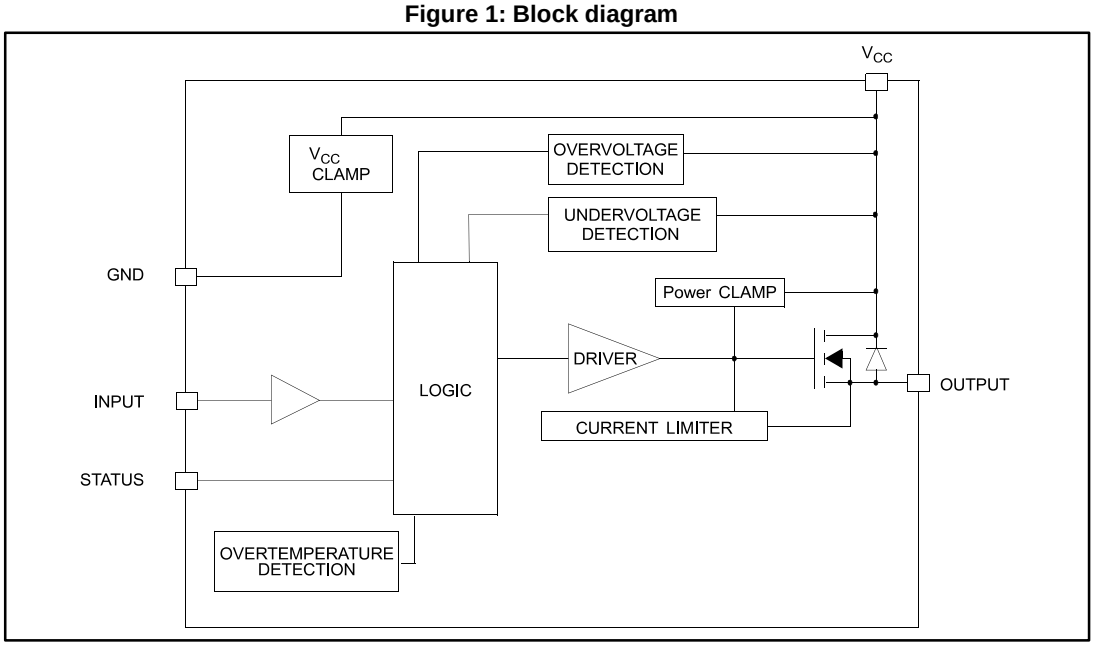
1 Block diagram

Figure 1: Block diagram



2 Pin connection

Figure 2: Connection diagram (top view)

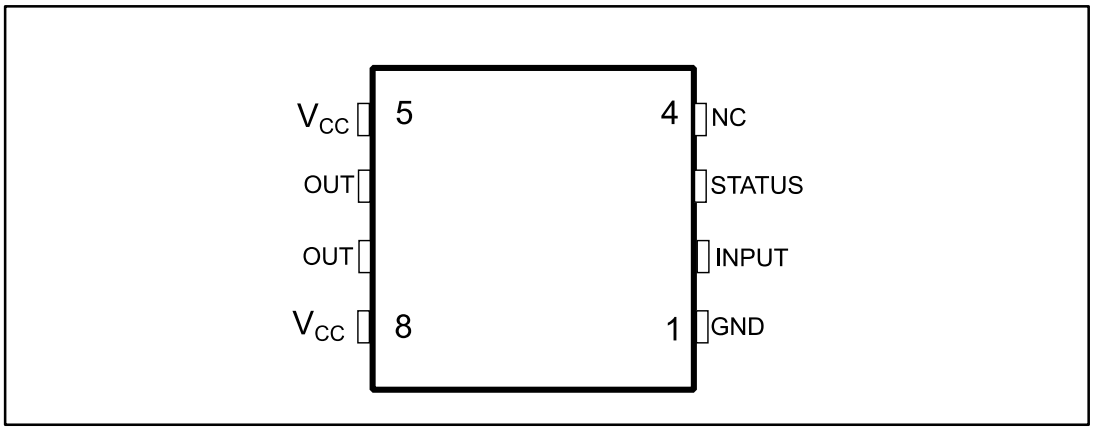
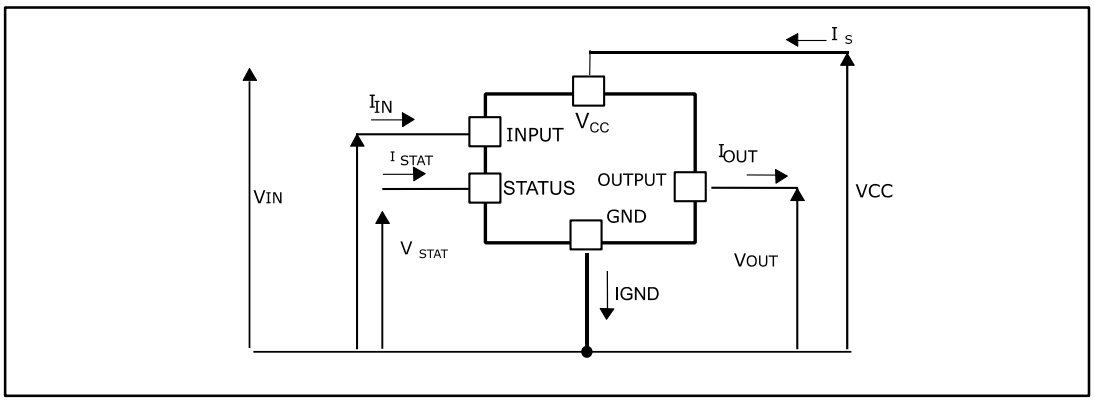


Figure 3: Current and voltage conventions



3 Maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	45	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-5	A
I_{IN}	DC input current	-1 to +10	mA
I_{STAT}	DC status current	-1 to +10	mA
V_{ESD}	Electrostatic discharge (R = 1.5 kΩ; C = 100 pF)	5000	V
E_{AS}	Single pulse avalanche energy	0.8	J
P_{TOT}	Power dissipation at T_C = 25 °C	Internally limited	W
T_J	Junction operating temperature	Internally limited	°C
T_C	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

Table 3: Thermal data

Symbol	Parameter		Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case	Max.	15	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	Max.	93 (1)	°C/W
			82 (2)	

Notes:

(1)When mounted on a standard single-sided FR-4 board with 0.5 cm^2 of Cu (at least 35 µm) thick connected to all VCC pins. Horizontal mounting and no artificial air flow.

(2)When mounted on a standard single-sided FR-4 board with 2 cm^2 of Cu (at least 35 µm) thick connected to all VCC pins. Horizontal mounting and no artificial air flow.

4 Electrical characteristics

8 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified

Table 4: Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		5.5		36	V
$R_{DS(on)}$	On-state resistance	I_{OUT} = 2 A at T_J = 25 °C		60		mΩ
		I_{OUT} = 2 A			180	
I_S(1)	Supply current	Off-state, V_{CC} = 24 V, T_J = 25 °C		10	20	µA
		On-state, V_{CC} = 24 V, T_J = 25 °C		3.5		mA
		On-state, V_{CC} = 24 V, T_J = 100 °C			3.8	mA
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown		36			V
$I_{L(off)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V	0		10	µA

Notes:

(1)Status: floating

Table 5: Switching (V_{CC} = 24 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(ON)}$	Turn-on delay time	R_L = 12 Ω from V_{IN} rising edge to V_{OUT} = 2.4 V		12		µs
$t_{d(OFF)}$	Turn-off delay time of output current	R_L = 12 Ω from V_{IN} falling edge to V_{OUT} = 21.6 V		35		µs
$dV_{OUT}/dt_{(on)}$	Turn -on voltage slope	R_L = 12 Ω from V_{OUT} = 2.4 V to V_{OUT} = 19.2 V		0.80		V/µs
$dV_{OUT}/dt_{(off)}$	Turn -off voltage slope	R_L = 12 Ω from V_{OUT} = 21.6 V to V_{OUT} = 2.4 V		0.30		

Table 6: Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	V_{IN} = 1.25 V	1			µA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	V_{IN} = 3.25 V			10	µA
V_{hyst}	Input hysteresis voltage		0.5			V
I_{IN}	Input current	V_{IN} = V_{CC} = 5 V			10	µA
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	6	6.8	8	V
		I_{IN} = -1 mA		-0.7		

Table 7: Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	I_{STAT} = 1.6 mA			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; V_{STAT} = 5 V			10	µA
C_{STAT}	Status pin input capacitance	Normal operation; V_{STAT} = 5 V			100	V
I_{IH}	High level input current	V_{IN} = 3.25 V			10	µA
V_{SCL}	Status clamp voltage	I_{STAT} = 1 mA	6	6.8	8	V
		I_{STAT} = -1 mA		-0.7		

Table 8: Protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{demag}	Turn-off output clamp voltage	R_L =12 Ω; L = 6 mH	V_{CC} -47	V_{CC} -52	V_{CC} -57	V
T_{TSD}	Shutdown temperature		150	175	200	°C
I_{lim}	Current limitation	V_{CC} = 24 V; R_{LOAD} = 10 mΩ, t = 0.4 ms	2.7		6.0	A
T_{hyst}	Thermal hysteresis		7	20		°C
T_R	Reset temperature		135			°C

5 Test circuits

Figure 4: Peak short-circuit current

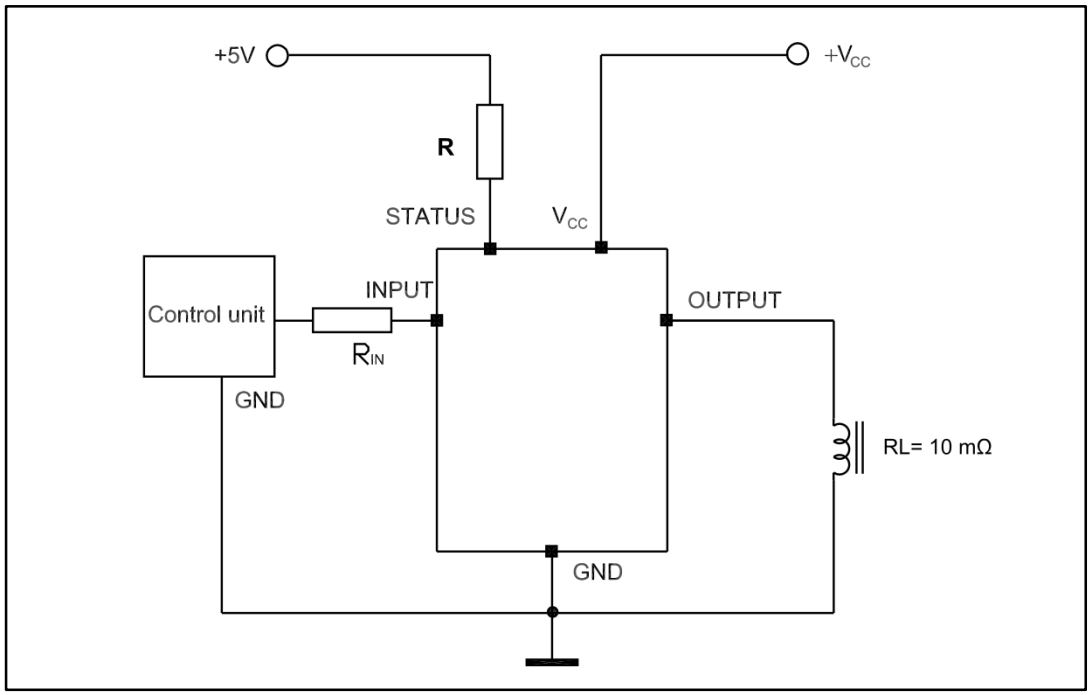
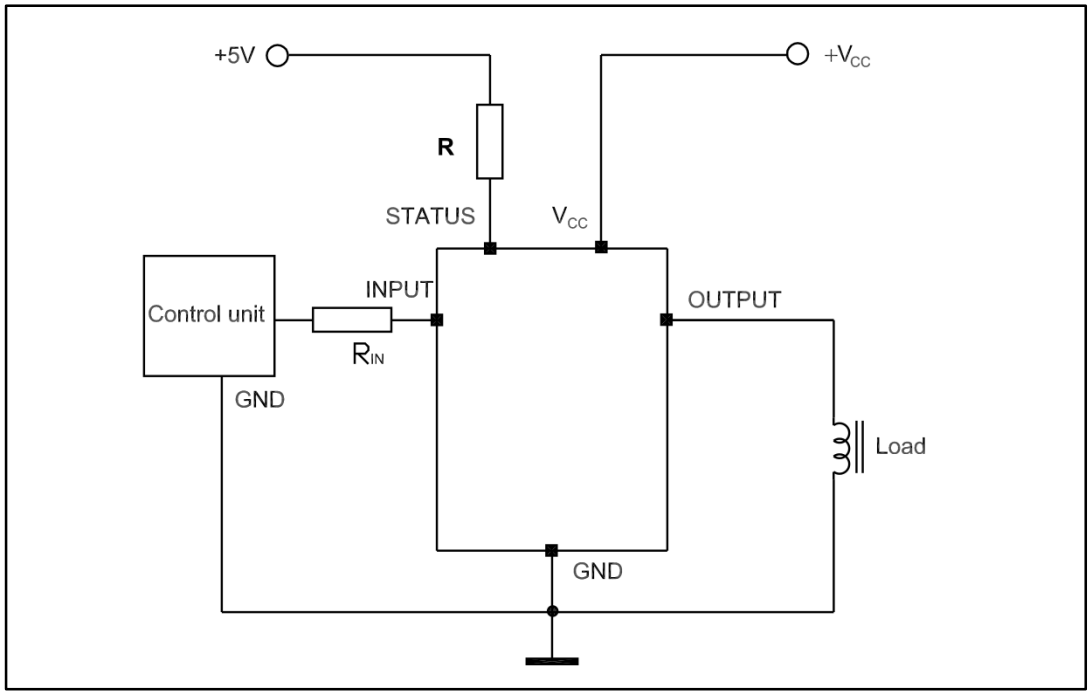


Figure 5: Avalanche energy test circuit



6 Switching time waveforms and truth table

Figure 6: Switching time waveforms

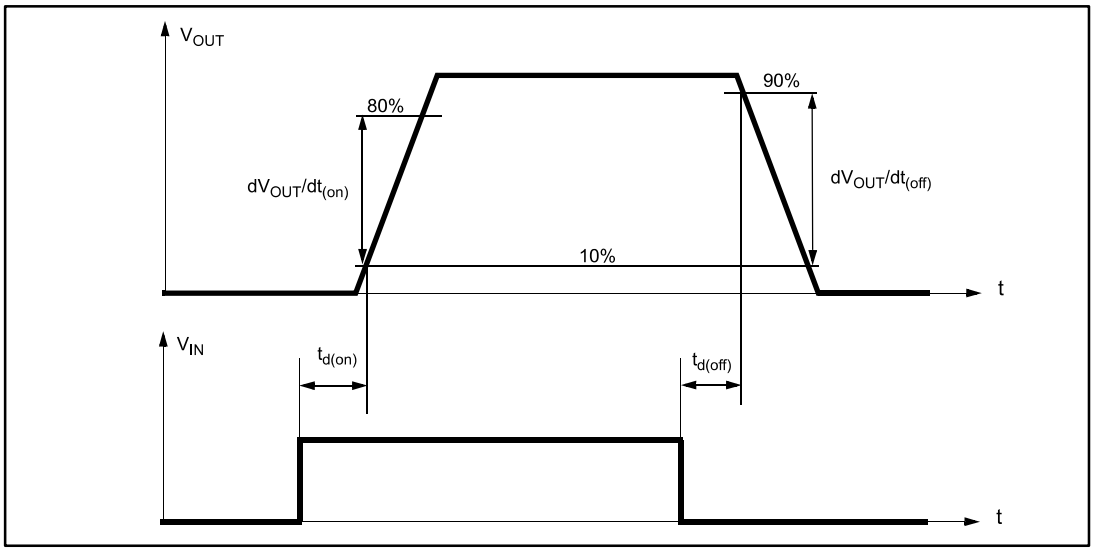
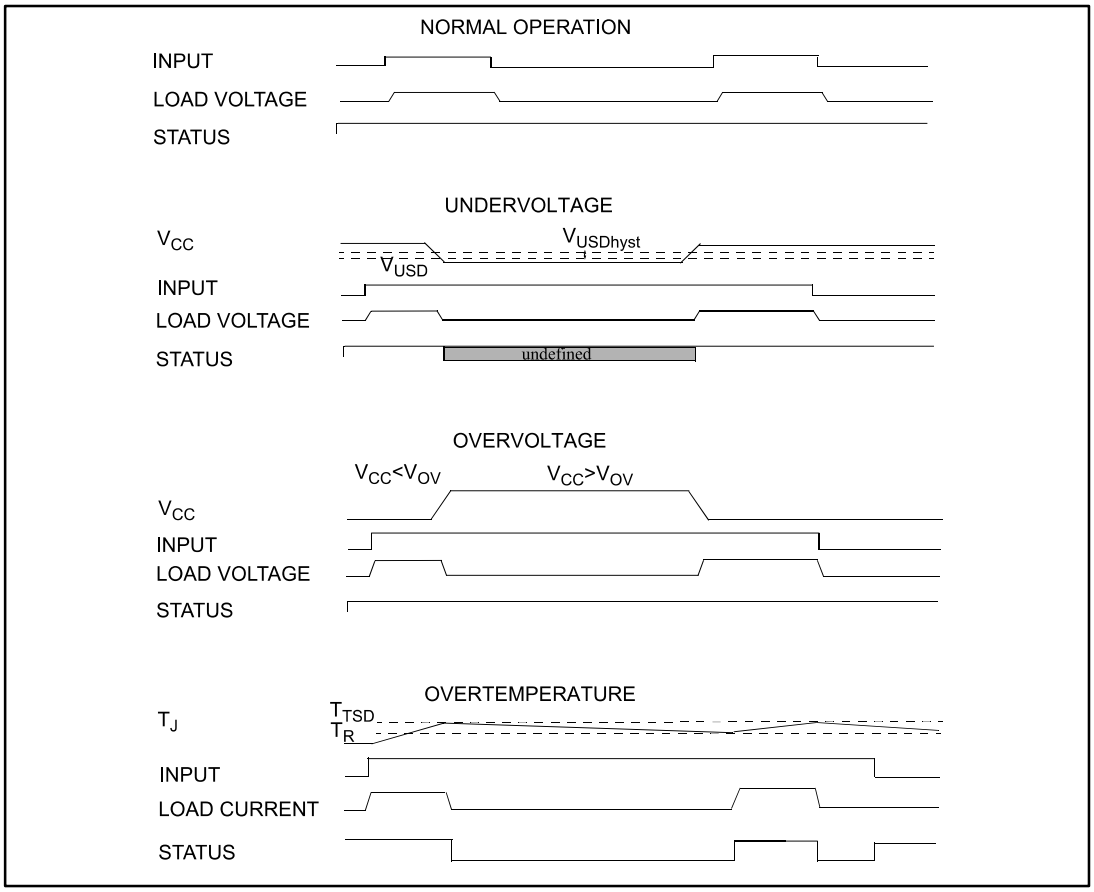


Table 9: Truth table

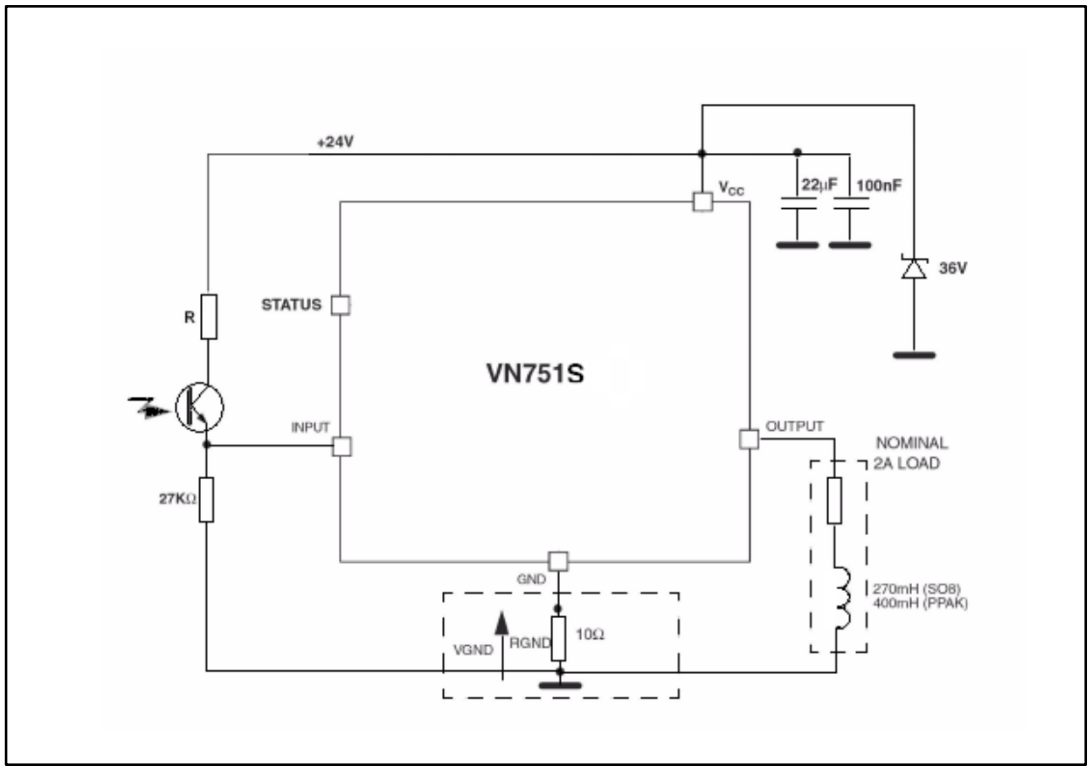
Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	($T_J < T_{TSD}$)H
	H	X	($T_J > T_{TSD}$)L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H

Figure 7: Waveforms



7 Application schematic

Figure 8: Application schematic



8 Reverse polarity protection

A schematic solution to protect the IC against a reverse polarity condition is proposed.

This schematic is effective with any type of load connected to the outputs of the IC. The R_{GND} resistor value can be selected according to the following conditions:

Equation 1:

$R_{GND} \leq 600\ mV / (I_S$ in ON-state max.).

Equation 2:

$R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

The power dissipation associated to R_{GND} during reverse polarity condition is:

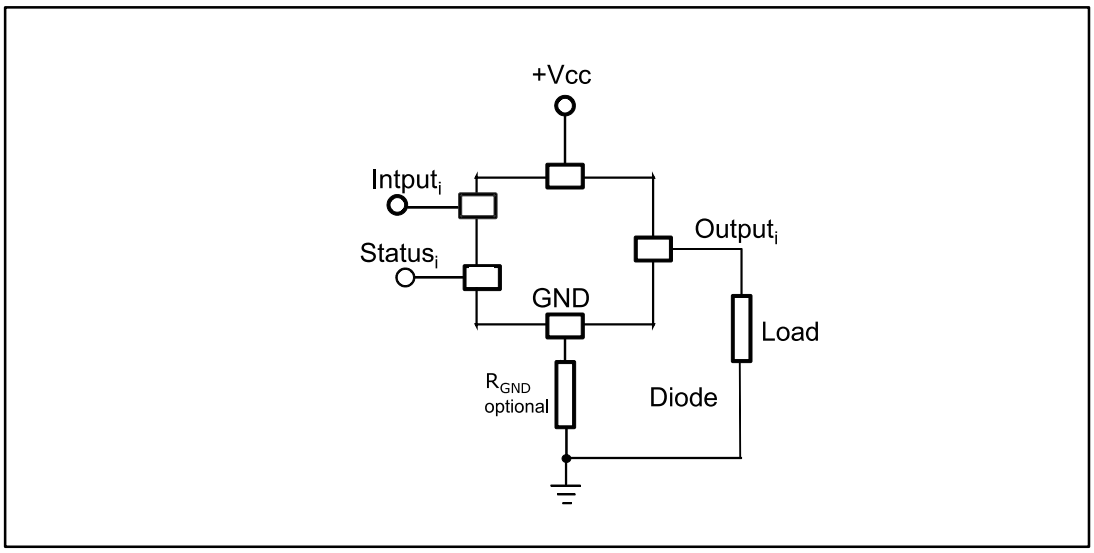
Equation 3:

$P_D = (-V_{CC})2 / R_{GND}$

This resistor can be shared by several different ICs.

In such case I_S value in equation 1 is the sum of the maximum ON-state currents of the different devices. Please note that if the microprocessor ground and the device ground are separated, the voltage drop across the R_{GND} (given by I^S in ON-state max. * R_{GND}) produces a difference between the generated input level and the IC input signal level. This voltage drop varies depending on how many devices are ON in case of several high-side switches sharing the same R_{GND}.

Figure 9: Reverse polarity protection



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

9.1 SO-8 package information

Figure 10: SO-8 package outline

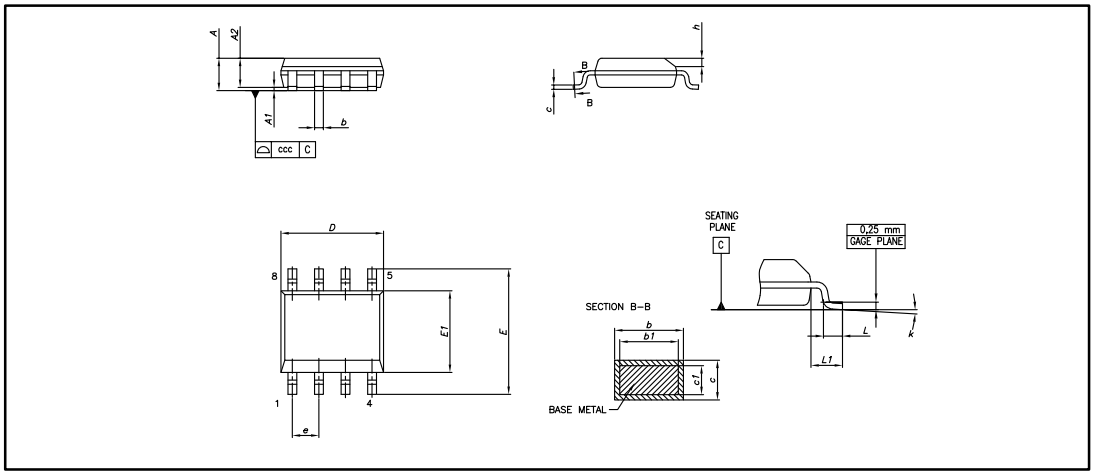
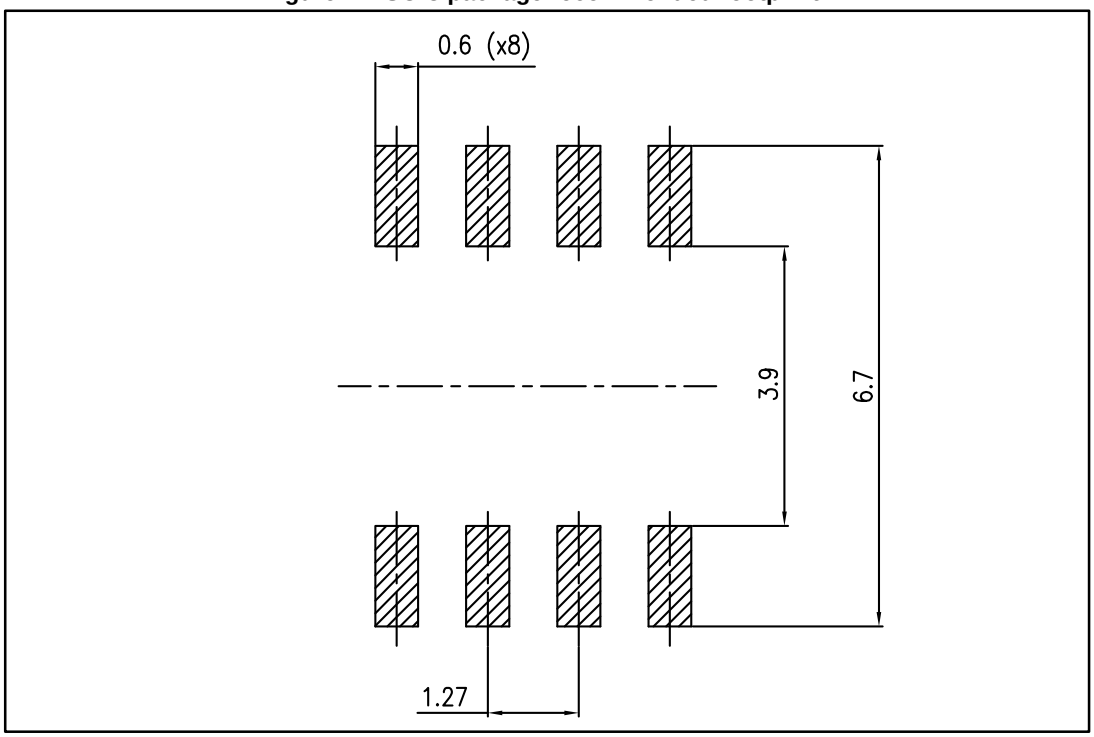


Table 10: SO-8 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

Figure 11: SO-8 package recommended footprint



9.2 SO-8 packing information

Figure 12: SO-8 tape and reel dimensions

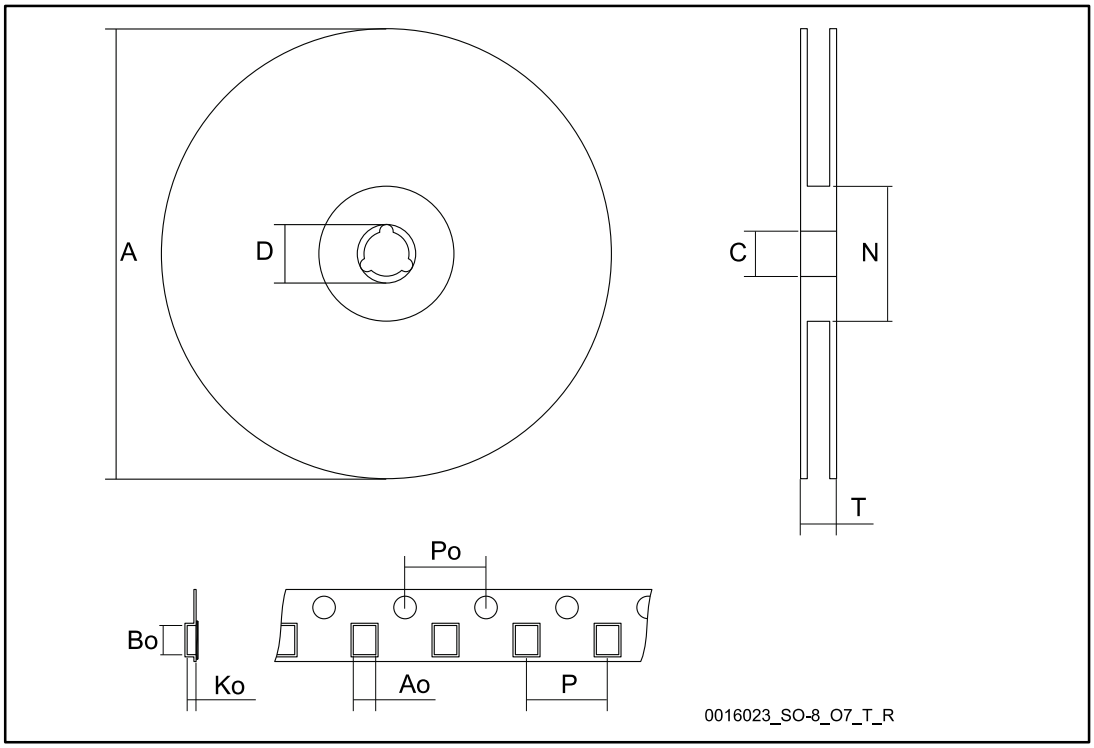


Table 11: SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

10 Revision history

Table 12: Document revision history

Date	Revision	Changes
18-Sep-2006	1	Initial release.
12-Mar-2007	2	Document reformatted, typo in *table 3*, updated P_{tot} value in *table 2*.
15-Mar-2007	3	Typo in *table 1* V_{ESD}.
18-Sep-2007	4	Added I_{STAT} value in *table 1*.
11-Oct-2007	5	Updated *table 2*.
08-Jul-2008	6	Added *section 7*.
30-Nov-2009	7	Updated cover page and *section 6*.
12-Jul-2016	8	Updated *Table 4: "Power section"*.

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