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Evaluating the ADP2140 Buck and LDO Combination Regulator

FEATURES

Buck regulator input voltage range: 2.3 V to 5.5 V
600 mA buck regulator output current
LDO input voltage range: 1.65 V to 5.5 V
300 mA LDO output current
LDO input can come from the output of the buck regulator or another supply
Operating temperature range: −40°C to +125°C

EQUIPMENT NEEDED

Voltmeters, ammeters, power supply
Electronic or resistive loads

DOCUMENTS NEEDED

ADP2140
UG-089

GENERAL DESCRIPTION

The ADP2140 evaluation board (ADP2140CP-EVALZ) is used to demonstrate the functionality of the ADP2140 buck and LDO combination regulator.

Basic electrical performance measurements, such as line and load regulation, dropout, efficiency, and ground current can be demonstrated with a few voltage supplies, voltmeters, current meters, and load resistors. For more details about the ADP2140 buck and LDO combination regulators, visit www.analog.com.

EVALUATION BOARD DIGITAL PICTURE

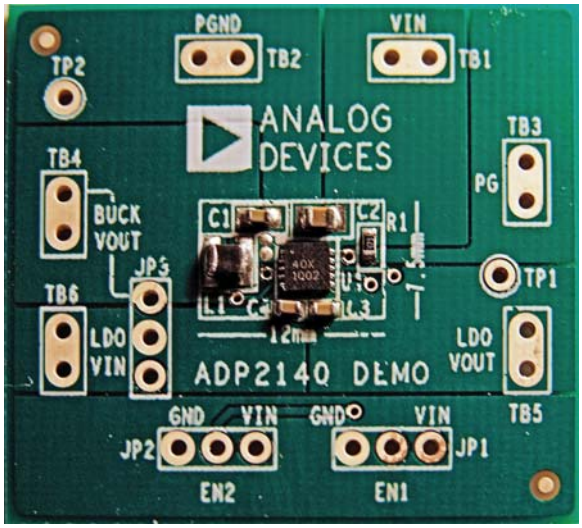

Figure 1.

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REVISION HISTORY

7/10—Revision 0: Initial Version

EVALUATION BOARD HARDWARE AND SCHEMATIC

EVALUATION BOARD CONFIGURATIONS

The ADP2140 evaluation board ships with all the components such as the input and output capacitors, buck inductor, and power-good pull-up resistor that are necessary to perform basic electrical performance measurements. The placement of the critical components in the buck (inductor and capacitors) have been optimized for low noise and the smallest footprint possible. Figure 2 shows the schematic of this evaluation board configuration. Table 1 lists and describes the hardware components.

The theory of operation and a functional description of the ADP2140 shown in Figure 2 are available in the ADP2140 data sheet.

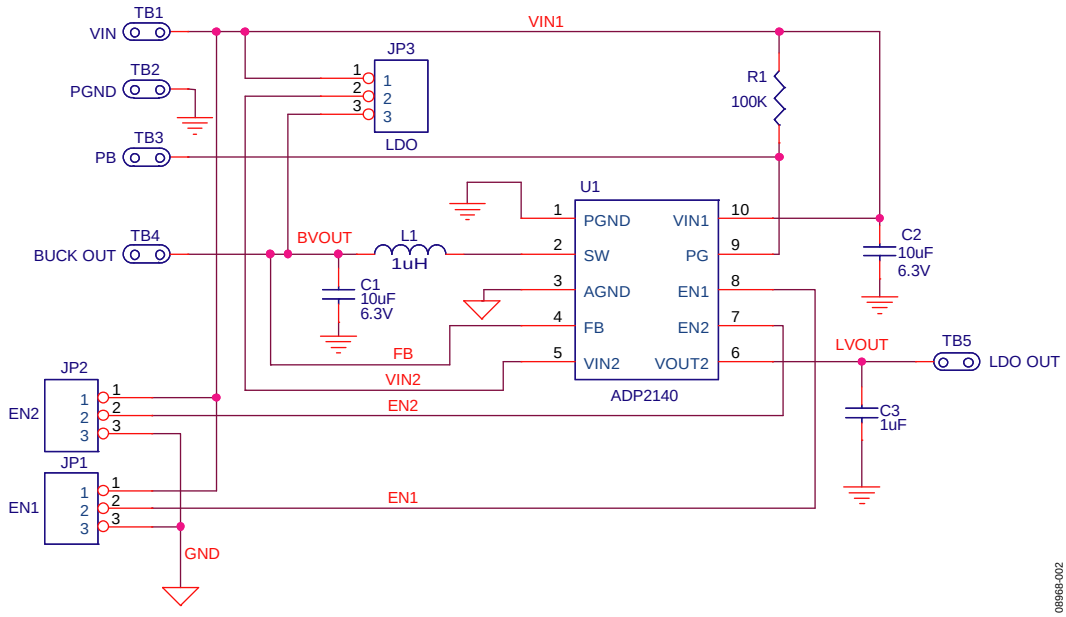

Figure 2. Evaluation Board Schematic

Table 1. Evaluation Board Hardware Components

Component	Function	Description
U1[1]	Linear regulator	ADP2140 buck and LDO combination regulator
C1	Buck output capacitor	10 µF output bypass capacitor required for transient performance
C2	Input capacitor	10 µF input capacitor required for stability and transient performance
C3	LDO output capacitor	1 µF output bypass capacitor required for transient performance
L1	Inductor	1 µH inductor
R1	Pull-up resistor	100 kΩ pull-up resistor for power good (PG)
JP1	Jumper	Connects EN1 to VIN1 or GND
JP2	Jumper	Connects EN2 to VIN1 or GND
JP3	Jumper	Connects LDO input to VIN1 or to the buck output

[1] Component varies depending on the evaluation board model ordered.

BUCK REGULATOR MEASUREMENTS

Figure 3 shows how to connect the evaluation board to a voltage source and a voltmeter for basic output voltage accuracy measurements. A resistor can be used as the load for the regulator.

Ensure that the resistor has a power rating adequate to handle the power that is expected to dissipate across it or, as an alternative, use an electronic load. In addition, ensure that the voltage source can supply enough current for the expected load levels.

Follow these steps to connect to a voltage source and voltage meter:

1. Connect the negative terminal (−) of the voltage source to the PGND (TB2) pad on the evaluation board.
2. Connect the positive terminal (+) of the voltage source to the VIN (TB1) pad of the evaluation board.
3. Connect a load between the BUCK VOUT (TB4) pad and one of the PGND pads.
4. Connect the negative terminal (−) of the voltmeter to one of the PGND pads.
5. Connect the positive terminal (+) of the voltmeter to the BUCK VOUT pad.
6. Connect a jumper between Pin 1 and Pin 2 of JP1 to enable the buck.
7. Connect a jumper between Pin 2 and Pin 3 of JP2 to disable the LDO.
8. Turn on the voltage source.

If the load current is large, connect the voltmeter as close as possible to TB4 to reduce the effects of IR drops.

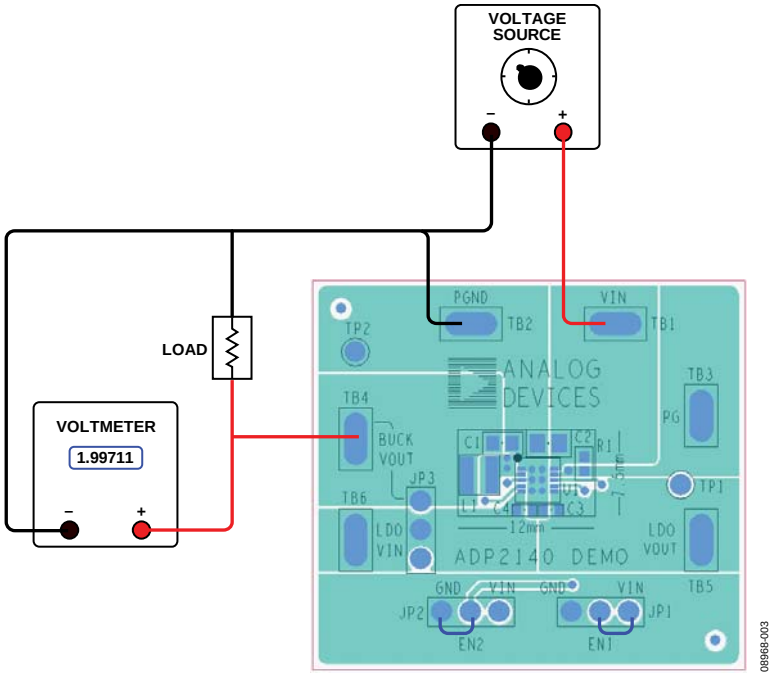

Figure 3. Buck Output Voltage Regulation Measurement Setup

LINE REGULATION—BUCK REGULATOR

For line regulation measurements, the buck output is monitored while its input is varied. For good line regulation, the output must change as little as possible with varying input levels.

For example, for an ADP2140 with a fixed 1.8 V output, V_{IN} needs to be varied between 2.5 V and 5.5 V. This measurement can be repeated under different load conditions. Figure 4 shows the typical line regulation performance of an ADP2140 with a fixed 1.8 V output.

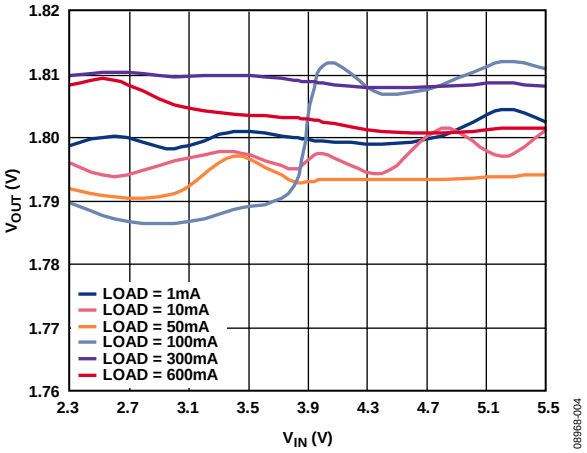

Figure 4. Output Voltage vs. Input Voltage

LOAD REGULATION—BUCK REGULATOR

For load regulation measurements, the output of the buck is monitored while the load is varied. For good load regulation, the output must change as little as possible with varying loads.

The input voltage must be held constant during this measurement. The load current can be varied from 0 mA to 600 mA. Figure 5 shows the typical load regulation performance of an ADP2140 with a fixed 1.8 V output for an input voltage of 3.0 V.

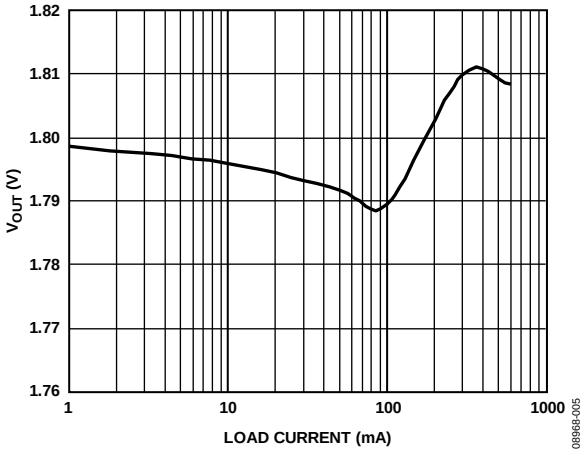

Figure 5. Output Voltage vs. Load Current

EFFICIENCY

Figure 6 shows how to connect the evaluation board to a voltage source, two voltmeters, and two ammeters for basic efficiency measurements. Use a resistor as the load for the buck regulator.

Ensure that the resistor has a power rating adequate to handle the power that is expected to dissipate across it, or, as an alternative, use an electronic load. In addition, ensure that the voltage source can supply enough current for the expected load levels.

Follow these steps to connect to a voltage source and meters:

1. Connect a jumper between Pin 1 and Pin 2 of JP1 to enable the buck regulator.
2. Connect a jumper between Pin 2 and Pin 3 of JP2 to disable the LDO regulator.
3. Connect the negative terminal (−) of the voltage source to the PGND pad on the evaluation board.
4. Connect the positive terminal (+) of the voltage source to the positive terminal (+) of an input ammeter.
5. Connect the negative terminal (−) of the input ammeter to the VIN pad of the evaluation board.
6. Connect the positive terminal (+) of the input voltmeter to the VIN pad of the evaluation board.
7. Connect the negative terminal (−) of the input voltmeter to the PGND pad of the evaluation board.
8. Connect the positive terminal (+) of the output ammeter to the buck output pad on the evaluation board. Connect a load between the negative terminal (−) of the output ammeter and the PGND pad.
9. Connect the positive terminal (+) of the output voltmeter to the buck output pad of the evaluation board.
10. Connect the negative terminal (−) of the output voltmeter to the PGND pad of the evaluation board.
11. Turn on the voltage source.

If the load current is large, connect the voltmeters as close as possible to the VIN and buck output pads to reduce the effects of IR drops.

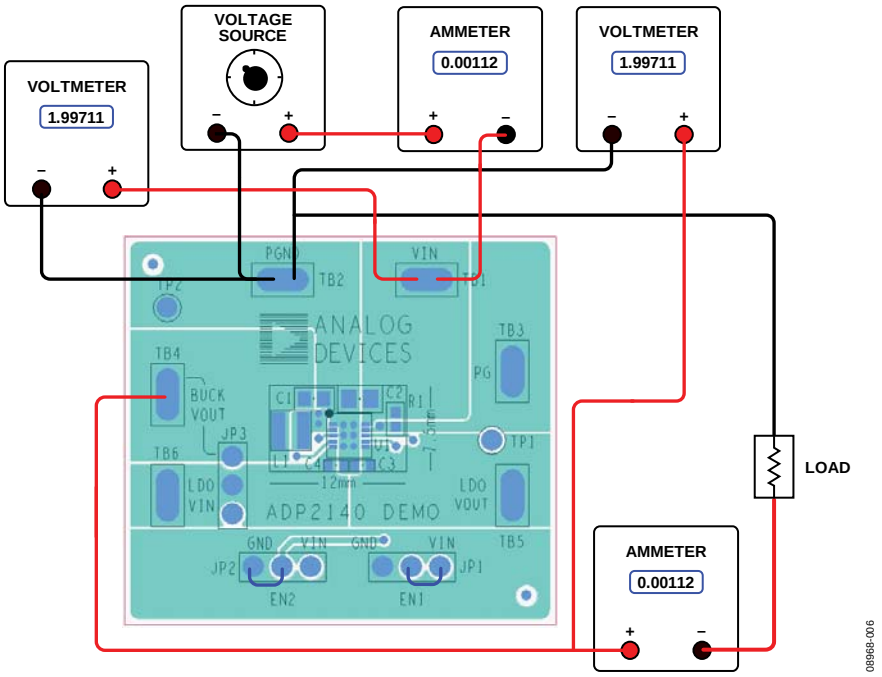

Figure 6. Buck Efficiency Measurement

The efficiency is calculated as follows:

$$Efficiency = 100\% \times (V_{OUT} \times I_{OUT})/(V_{IN} \times I_{IN})$$

The efficiency of the buck regulator can be measured over several combinations of input voltage and load currents. Figure 7 shows the efficiency of a 1.8 V output buck over input voltage and load current.

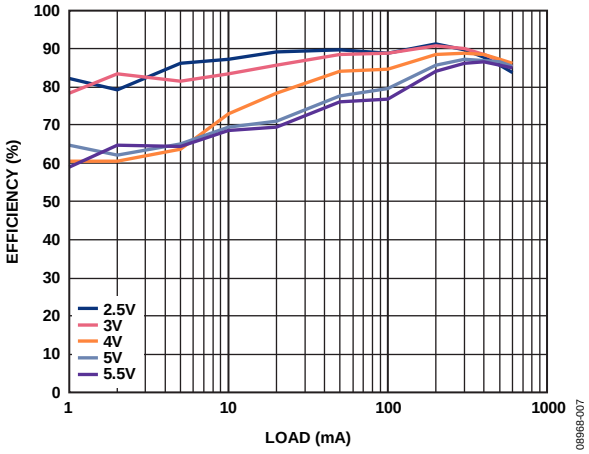

Figure 7. Efficiency vs. Input Voltage and Load

QUIESCENT CURRENT MEASUREMENT

Figure 8 shows how to connect the evaluation board to a voltage source and an ammeter for quiescent current measurements.

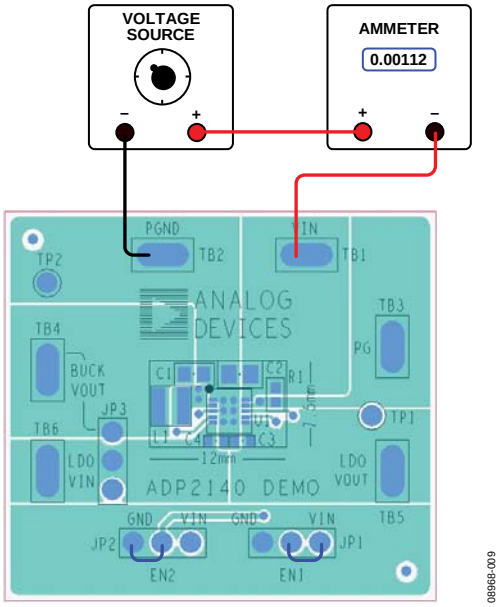

Figure 8. Buck Quiescent Current Measurement

Follow these steps to connect to a voltage source and ammeter:

1. Connect a jumper between Pin 1 and Pin 2 of JP1 to enable the buck regulator.
2. Connect a jumper between Pin 2 and Pin 3 of JP2 to disable the LDO regulator.
3. Connect the positive terminal (+) of the voltage source to the positive terminal (+) of the ammeter.
4. Connect the negative terminal (−) of the ammeter to the VIN pad of the evaluation board.
5. Connect the negative terminal (−) of the voltage source to the PGND pad of the evaluation board.
6. Remove R3. Alternatively, R3 can remain in circuit, but it increases the quiescent current by 100 kΩ/V_{IN}.
7. Turn on the voltage source.

QUIESCENT CURRENT CONSUMPTION

Quiescent current measurements can determine how much current the internal circuits of the buck regulator are consuming under no load conditions. To be efficient, the regulator needs to consume as little current as possible. Figure 9 shows the typical quiescent current consumption at no load for various input voltages. When the device is disabled (EN1 = PGND), ground current drops to less than 2 µA.

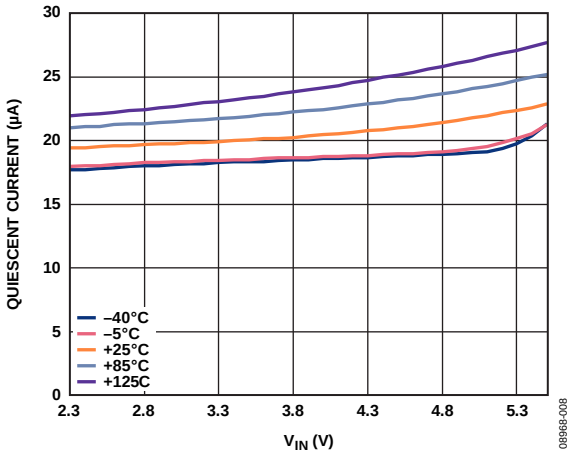

Figure 9. Quiescent Current vs. Input Voltage

LDO MEASUREMENTS

Figure 10 shows how to connect the evaluation board to a voltage source and a voltmeter for basic LDO output voltage accuracy measurements. A resistor can be used as the load for the regulator.

Ensure that the resistor has a power rating adequate to handle the power that is expected to dissipate across it or, as an alternative, use an electronic load. In addition, ensure that the voltage source can supply enough current for the expected load levels.

Follow these steps to connect the evaluation board to a voltage source and voltage meter:

1. Connect a jumper between Pin 3 and Pin 2 of JP1 to disable the buck.
2. Connect a jumper between Pin 2 and Pin 1 of JP2 to enable the LDO.
3. Connect the negative terminal (−) of a voltage source to one of the PGND pads on the evaluation board.
4. Connect the positive terminal (+) of a voltage source to the VIN pad of the evaluation board. Set this voltage source to 3.0 V.
5. Connect the negative terminal (−) of the LDO input voltage source to one of the PGND pads on the evaluation board.
6. Connect the positive terminal (+) of the LDO input voltage source to Pin 2 of JP3.
7. Connect a load between the VOUT pad and the PGND pad.
8. Connect the negative terminal (−) of the voltmeter to the PGND pad.
9. Connect the positive terminal (+) of the voltmeter to the VOUT pad.
10. If the connection between the LDO input voltage source and Pin 2 of JP3 is longer than six inches, connect a 1 µF ceramic capacitor from PGND to Pin 2 of JP3.
11. Turn on the voltage source.

If the load current is large, connect the voltmeter as close as possible to the LDO output pad (TB5) to reduce the effects of IR drops.

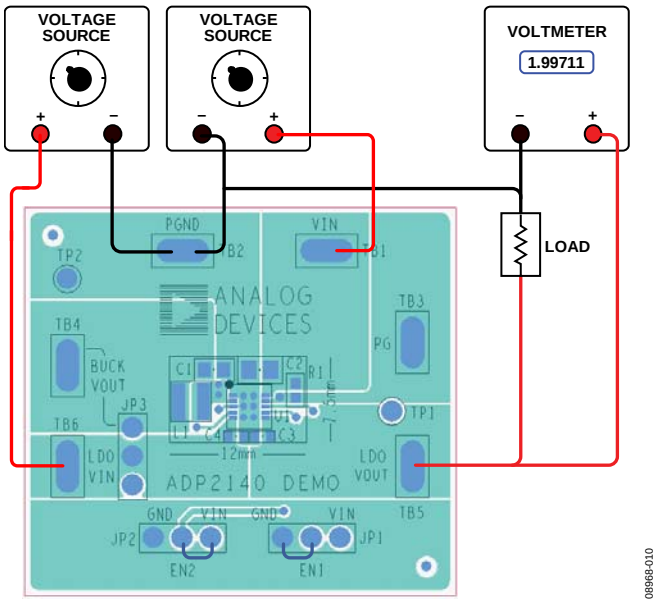

Figure 10. LDO Output Voltage Regulation Measurement Setup

LINE REGULATION—LDO REGULATOR

For line regulation measurements, the LDO output is monitored while its input voltage is varied. For good line regulation, the output must change as little as possible with varying input levels.

To ensure that the device is not in dropout mode during this measurement, the LDO input voltage must be varied between V_{OUTNOM} + 0.4 V (or +1.65 V, whichever is greater) and V_{INMAX}. For example, for an ADP2140 with a fixed 1.2 V output, the LDO input voltage needs to be varied between 1.65 V and 5.5 V. This measurement can be repeated under different load conditions. Figure 11 shows the typical line regulation performance of an ADP2140 with fixed 1.2 V output.

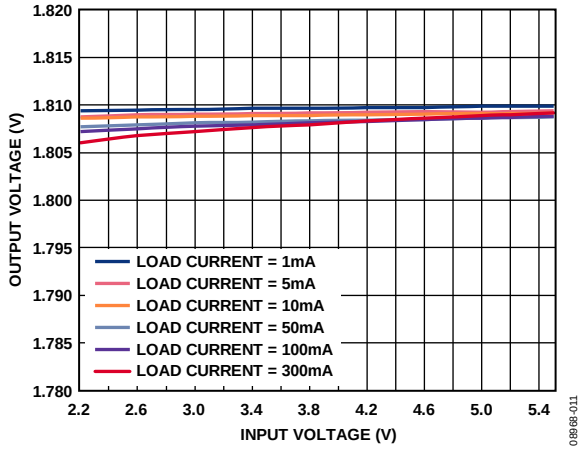

Figure 11. Output Voltage vs. Input Voltage

LOAD REGULATION—LDO REGULATOR

For load regulation measurements, the output of the regulator is monitored while the load is varied. For good load regulation, the output must change as little as possible with varying loads.

The LDO input voltage must be held constant during this measurement. The load current can be varied from 0 mA to 300 mA. Figure 12 shows the typical load regulation performance of an ADP2140 with a fixed 1.2 V output for an input voltage of 1.8 V.

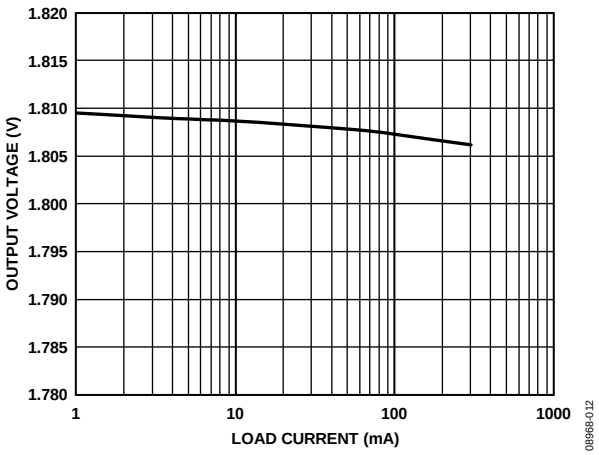

Figure 12. Output Voltage vs. Load Current

DROPOUT VOLTAGE

Dropout voltage can be measured using the configuration shown in Figure 10. Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 1.65 V. Dropout voltage increases with larger loads.

To obtain measurements that are more accurate, use a second voltmeter to monitor the LDO input voltage at Pin 2 of JP3. The input supply voltage may need to be adjusted to account for IR drops, especially if large load currents are used. Figure 13 shows a typical curve of dropout voltage measurements with different load currents for a 1.8 V output.

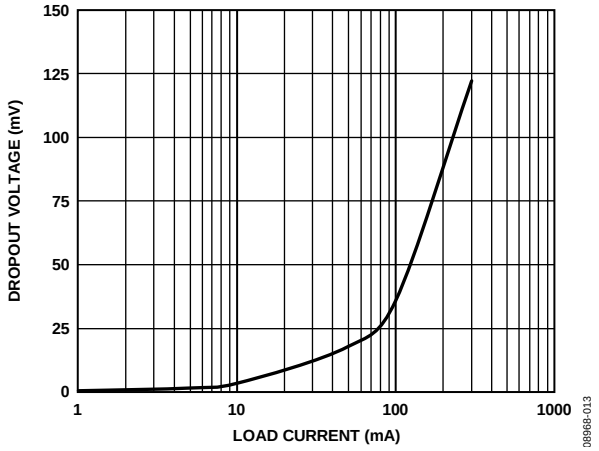

Figure 13. Dropout Voltage vs. Load Current

GROUND CURRENT MEASUREMENT

Figure 14 shows how to connect the evaluation board to a voltage source and an ammeter for ground current measurements. A resistor can be used as the load for the regulator. Ensure that the resistor has a power rating adequate to handle the power that is expected to dissipate across it or, as an alternative, use an electronic load. Ensure that the voltage source used can supply enough current for the expected load levels.

Follow these steps to connect to a voltage source and ammeter:

1. Connect a jumper between Pin 3 and Pin 2 of JP1 to disable the buck.
2. Connect a jumper between Pin 2 and Pin 1 of JP2 to enable the LDO.
3. Connect a jumper between Pin 1 and Pin 2 of JP3 to power the LDO from VIN.
4. Connect the positive terminal (+) of the voltage source to the VIN pad on the evaluation board.
5. Connect the positive terminal (+) of the ammeter to the PGND pad of the evaluation board.
6. Connect the negative terminal (−) of the ammeter to the negative (−) terminal of the voltage source.
7. Connect a load between the VOUT pad of the evaluation board and the negative (−) terminal of the voltage source.
8. Remove R3. Alternatively, R3 can remain in circuit but it increases the quiescent current by 100 kΩ/V_{IN}.
9. Turn on the voltage source.

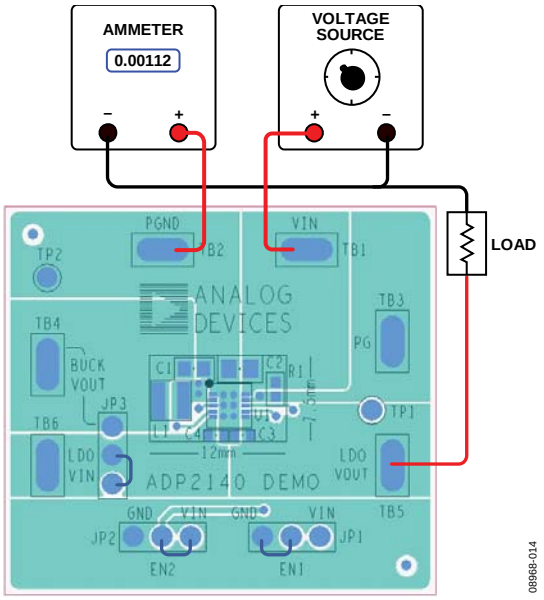

Figure 14. LDO Ground Current Measurement

GROUND CURRENT CONSUMPTION

Ground current measurements can determine how much current the internal circuits of the regulator are consuming while the circuits perform the regulation function. To be efficient, the regulator needs to consume as little current as possible. Typically, the regulator uses the maximum current when supplying its largest load level (300 mA). Figure 15 shows the typical ground current consumption for various load levels at V_{IN} = 2.5 V. When the device is disabled (EN2 = PGND), ground current drops to less than 2 µA.

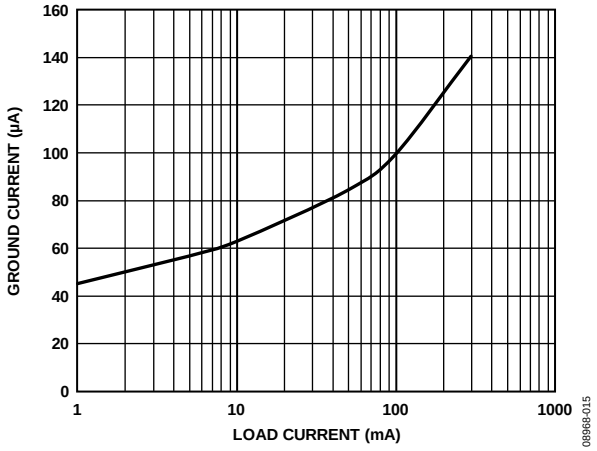

Figure 15. Ground Current vs. Load Current

POWER SEQUENCING

The ADP2140 has a flexible power sequencing system supporting two distinct activation modes, individual or autosequence, as follows:

- Individual activation control is where EN1 controls only the buck regulator and EN2 controls only the LDO regulator. A high level on the EN1 pin turns on the buck regulator and a high level on the EN2 pin turns on the LDO regulator. A logic low level turns off the respective regulator.
- Autosequence is where the two regulators are turned on in a specified order and delay after a low-to-high transition on the EN1 pin.

Select the activation mode (individual or autosequence) by decoding the state of Pin EN2. The individual activation mode is selected when the EN2 pin is driven externally or hard wired to a voltage level (VIN1, PGND). The autosequencing mode is selected when the EN2 pin remains unconnected (floating).

To minimize quiescent current consumption, mode selection is performed only after a low-to-high transition of the EN1 pin. The detection circuit then activates for the time needed to assess the EN2 state, after which time the circuit is disabled until the next EN1 low-to-high transition. The detection circuit has a 4 µs deglitch time to avoid false activations.

When EN2 is unconnected, the internal control circuit provides a termination resistor to ground to avoid false detection levels, which can occur when EN2 remains floating. The 100 kΩ termination resistor is low enough to guarantee insensitivity to noise and transients. The termination resistor is disabled in the event that the EN2 pin is driven externally to a logic level high (individual activation mode assumed) to reduce the quiescent current consumption. In addition, the termination resistor on the EN2 pin is enabled by default after power-up.

Upon ENx activation or deactivation, a 4 µs deglitch filter prevents unwanted changes in the regulator state due to line noise or perturbation.

When the autosequence mode is selected, the EN1 pin is used to start the on/off sequence of the regulators. A logic high sequences the regulators on whereas a logic low sequences the regulators off. The regulator activation order is associated with the voltage selected for the buck regulator and the LDO regulator.

When the turn on or turn off autosequence starts, the startup delay between the first and the second regulator is fixed to 5 ms (t_{REG12}, as shown in Figure 17 and Figure 18).

When the application requires activating and deactivating the regulators at the same time, the independent activation mode can be used, which connects the EN1 and EN2 pins together, as shown in Figure 21.

Table 2. Power Sequencing Modes

EN2[1]	EN1	Description
0	0	Individual mode: LDO and buck regulators are off.
0	1	Individual mode: buck regulator is on.
1	0	Individual mode: LDO regulator is on.
1	1	Individual mode: LDO and buck regulators are on.
NC	Rising edge	Autosequence: buck regulator turns on then the LDO regulator turns on. The LDO voltage is less than the buck voltage.
NC	Rising edge	Autosequence: LDO regulator turns on and then the buck regulator turns on. The LDO voltage is greater than the buck voltage.
NC	Rising edge	Autosequence: If the buck regulator = 1.875 V, the LDO regulator always turns on first, then the buck regulator turns on.
NC	Falling edge	Autosequence: the LDO and buck regulators turn off at the same time.

[1] NC means not connected.

Table 3 describes the symbols in Figure 16 through Figure 21.

Table 3. Symbol Descriptions

Symbol Name	Description	Typical Value
t_{START}	Time needed for the internal circuitry to activate the first regulator	60 µs
t_{SS}	Regulator soft start time	330 µs
t_{RESET}	Time delay from power-good (PG) condition to the release of PG	5 ms
t_{REG12}	Delay time between buck and LDO activation	5 ms

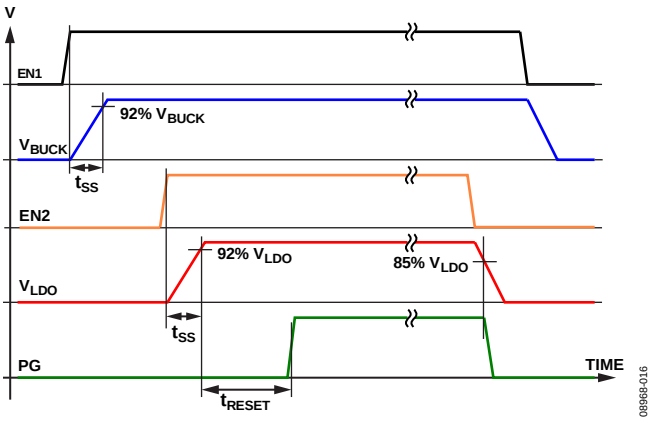

Figure 16. Individual Activation Mode

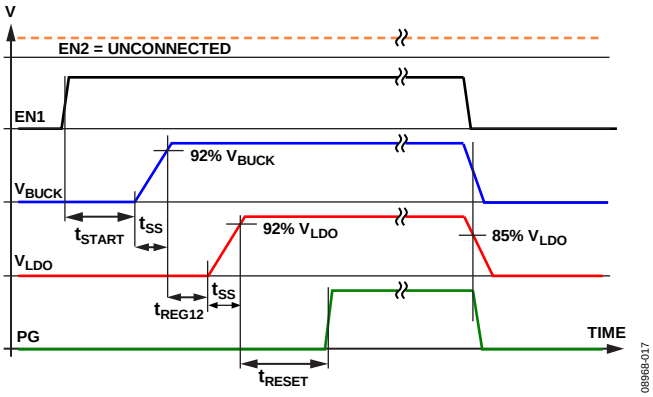

Figure 17. Auto Sequencing Mode, Buck First Then LDO

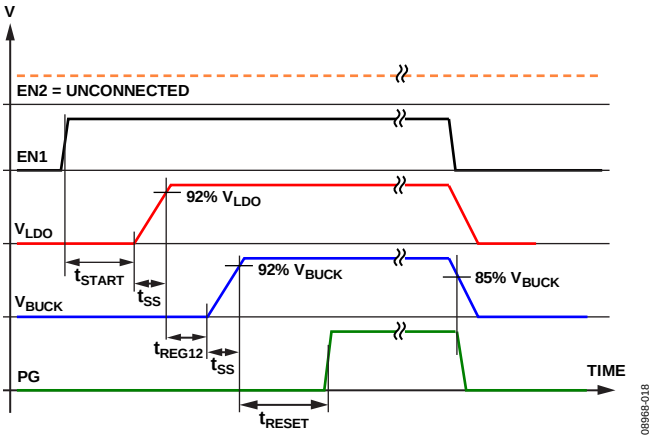

Figure 18. Auto Sequencing Mode, LDO First Then Buck

The PG pin responds to the last activated regulator. As described in the Power Sequencing section, the regulator order in the autosequence mode is defined by the voltage option combination. Therefore, if the sequence is buck regulator first, the LDO regulator and the PG signal are active low for t_{RESET} after V_{LDO} reaches 92% of the rated output voltage, at which time PG goes high and remains high for as long as V_{LDO} is above 85% of the rated output voltage. When the sequencing is LDO regulator first followed by the buck regulator, the PG pin is controlled by V_{BUCK}. This control scheme also applies when the individual activation mode is selected.

As soon as either the buck or the LDO regulator output voltage drops below 85% of the respective nominal level, the power-good (PG) pin is forced low.

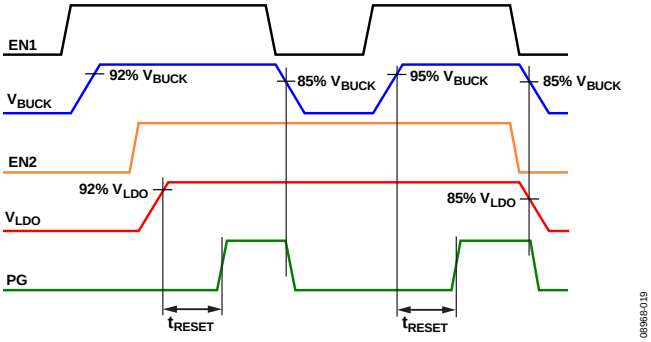

Figure 19. Individual Activation Mode, Both Regulators Sensed

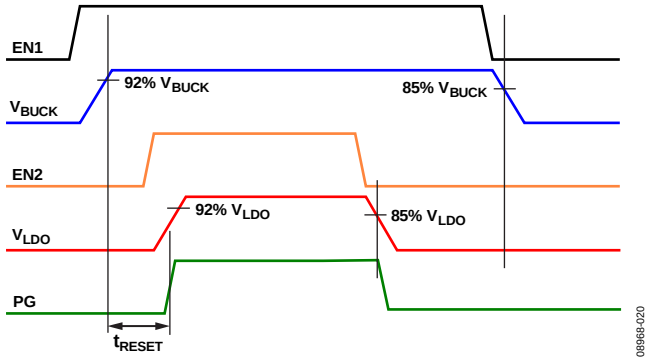

Figure 20. Individual Activation Mode, Only One Regulator (Buck) Sensed

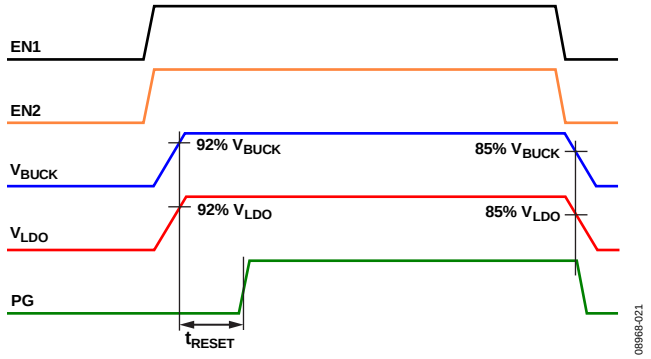

Figure 21. Individual Activation Mode, No Activation/Deactivation Delay Between Regulators, EN1 and EN2 Pins Tied Together

POWER GOOD PIN

The ADP2140 power-good (PG) pin indicates the state of the monitored output voltages. PG is an active low, open-drain output, requiring an external pull-up resistor typically supplied from the I/O supply rail, as shown in Figure 2. When the sensed output voltage is below 92% of its nominal voltage, the PG pin is held low. When the sensed output voltage rises above 92% of its nominal level, the PG line is pulled high after t_{RESET}. The PG pin remains high as long as the sensed output voltage is above 85% of the nominal output voltage level. A 4 µs deglitch filter ensures that noise or external perturbations do not trigger the PG line.

LDO AS A POST REGULATOR TO REDUCE BUCK OUTPUT NOISE

The output of the buck regulator may not be suitable for many noise sensitive applications because of its inherent switching noise. This is particularly true when the buck regulator is operating in PSM mode because the switching noise is in the audio range. The ADP2140 LDO regulator can greatly reduce the noise at the output of the buck regulator at high efficiency because of the load dropout voltage of the LDO regulator and the high PSRR of the LDO regulator. Figure 22 and Figure 23 show the noise reduction that is possible when the LDO is used as a post regulator.

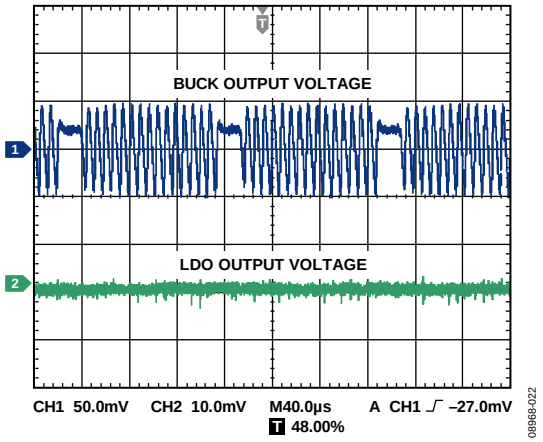

Figure 22. LDO as a Post Regulator, V_{OUT} = 1.8 V, Load Current = 50 mA, V_{OUT2} = 1.2 V, Load Current = 50 mA

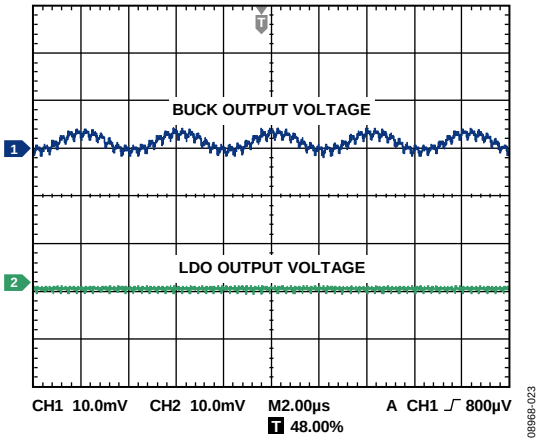

Figure 23. LDO as a Post Regulator, V_{OUT} = 1.8 V, Load Current = 500 mA, V_{OUT2} = 1.2 V, Load Current = 50 mA

PCB LAYOUT CONSIDERATIONS

Improve heat dissipation from the package by increasing the amount of copper attached to the pins of the ADP2140. However, as shown in Table 4, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Following are a few general tips when designing PCBs:

- Place the input capacitor as close as possible to the VINx and PGND pins.
- Place the input and output capacitors as close as possible to the VINx, VOUT2, and PGND pins.
- Connect the load as close as possible to VOUT.
- Use 0805-size inductor, and 0603- or 0402-size capacitors and resistors to achieve the smallest possible footprint solution on boards where area is limited.

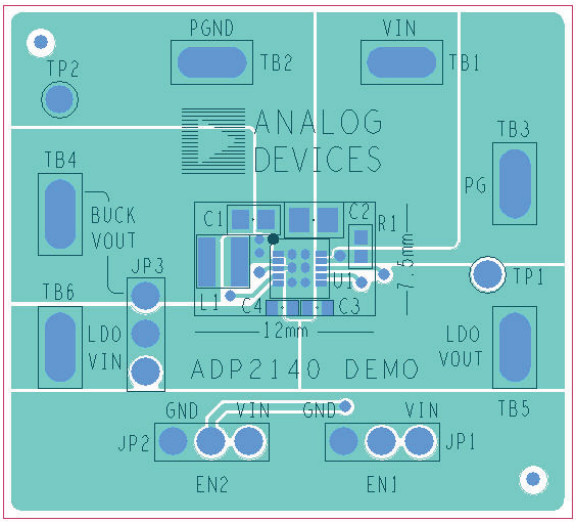

Figure 24. Typical Board Layout, Top Side

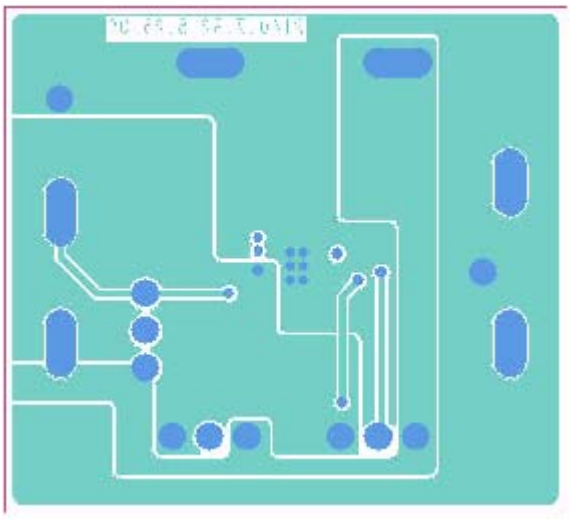

Figure 25. Typical Board Layout, Bottom Side

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP2140 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistance between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds that are used and the amount of copper on the PCB to which the PGND pins of the package are soldered. Table 4 shows typical θ_{JA} values of the 10-lead LFCSP for various PCB copper sizes. The typical Ψ_{JB} value of the 10-lead LFCSP is 16.9 °C/W.

Table 4. Typical θ_{JA} Values

Copper Size (mm²)	LFCSP θ_{JA} (°C/W)
0[1]	42.5
50	40
100	38.8
300	37.2
500	36.2

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADP2140 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = P_{LDO} + P_{BUCK}$$

where:

$$P_{LDO} = (V_{LDO\ IN} - V_{LDO\ OUT}) \times I_{LDO\ LOAD} \quad (2)$$

$$P_{BUCK} = V_{IN} \times I_{IN} - V_{OUT} \times I_{OUT} \quad (3)$$

where:
$V_{LDO\ IN}$, $V_{LDO\ OUT}$, V_{IN}, and V_{OUT} are the input and output voltages, respectively.
I_{OUT} and I_{LOAD} are the load currents.

Therefore, the junction temperature equation can be simplified as follows:

$$T_J = T_A + (P_{LDO} + P_{BUCK}) \times \theta_{JA} \quad (4)$$

As shown in Equation 4, for a given ambient temperature and continuous power dissipation, a minimum copper size requirement exists for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 26 through Figure 29 show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

In cases where the board temperature is known, the thermal characterization parameter, Ψ_{JB}, can be used to estimate the junction temperature rise. Calculate the maximum junction temperature (T_J) from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

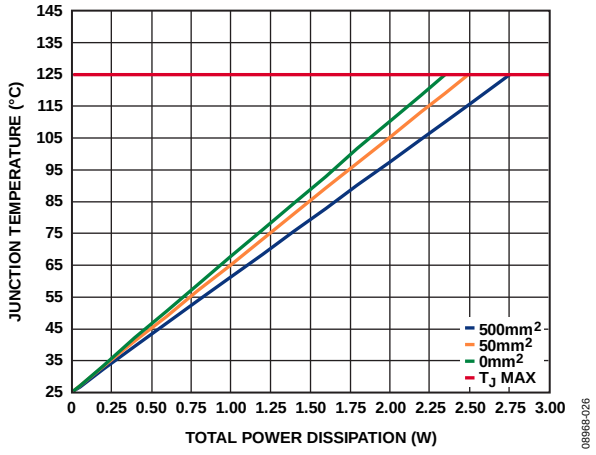

Figure 26. T_A = 25°C, LFCSP

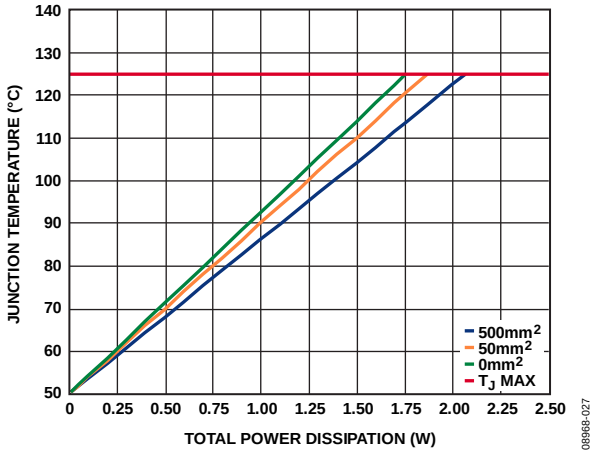

Figure 27. T_A = 50°C, LFCSP

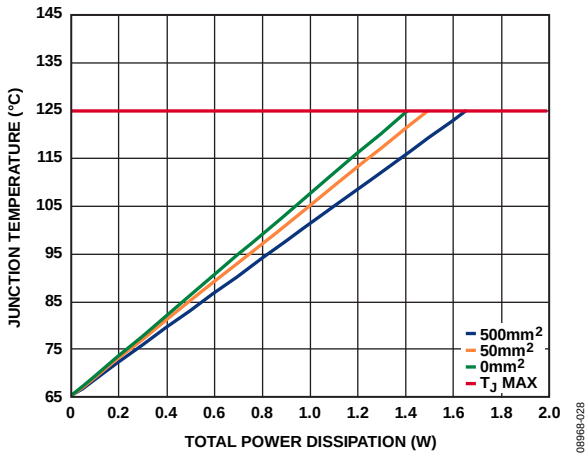

Figure 28. T_A = 65°C, LFCSP

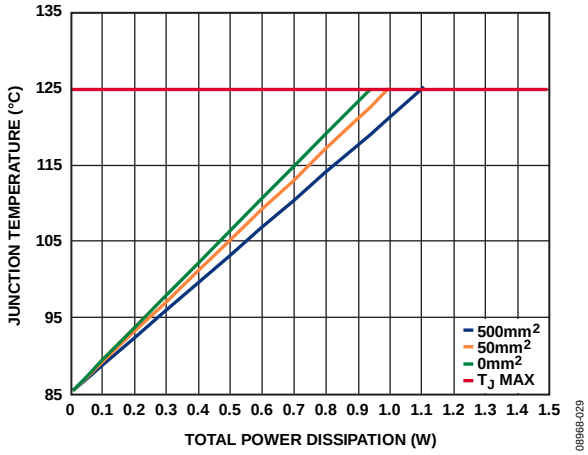

Figure 29. T_A = 85°C, LFCSP

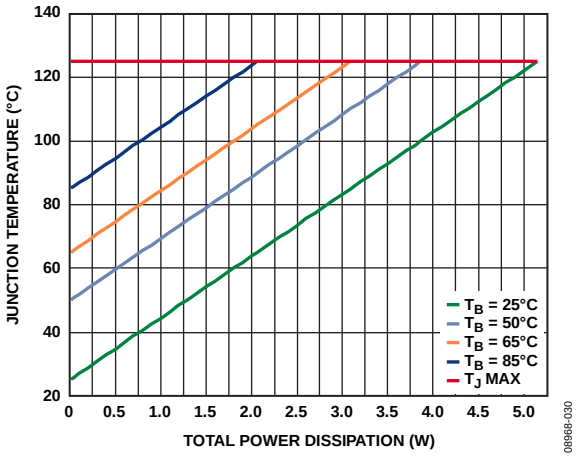

Figure 30. T_B = Various Temperatures, LFCSP

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. Components Listing

Qty.	Reference Designator	Description	Manufacturer/Vendor	Vendor Part No.
2	C1, C2	Capacitor, MLCC, 10 µF, 6.3 V, 0603, X5R	Murata or equivalent	GRM188R60J106ME47D
1	C3	Capacitor, MLCC, 1 µF, 6.3 V, 0402, X5R	Murata or equivalent	GRM155R60J105KE19D
3	JP1, JP2, JP3	Header, single, STR, three pins	Digi-Key Corp.	S1012E-03-ND
1	L1	Inductor, 1 µH, 0805	Murata or equivalent	LQM2HPN1R0MJ0L
1	R1	Resistor, 100 kΩ, 0.10 W, 0402	Vishay or equivalent	CRCW0402100KFKEA
1	U1	IC, buck LDO regulator	Analog Devices, Inc.	ADP2140ACPZ1812R7

RELATED LINKS

Resource	Description
ADP2140	Product Page
UG-089	*ADP2140 RedyKit™ User Guide*

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG08968-0-7/10(0)

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