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AD5686R/AD5685R/AD5684R Quick Start Guide

Quad, 16-/14-/12-Bit, Voltage Output DACs with a 2 ppm/ºC Reference, SPI Interface

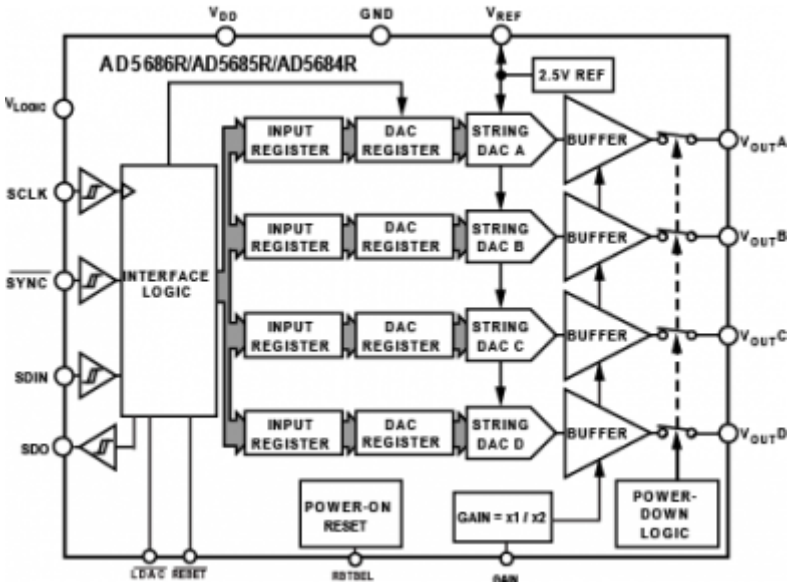

Figure 1. Functional Block Diagram

Features

- High relative accuracy (INL): ±2 LSB maximum (16-bit AD5686R)
- Low drift 2.5 V on-chip reference: 2 ppm/°C typical temperature coefficient
- Tiny 3 mm × 3 mm 16-lead LFCSP or 16-lead TSSOP package
- Total unadjusted error (TUE): 0.1 % of FSR maximum
- Offset error: 1.5 mV maximum
- Gain error: 0.1% of FSR maximum
- High drive capability: 20 mA, 0.5 V from supply rails
- User selectable gain of 1 or 2 (GAIN pin)
- Reset to zero scale or midscale (RSTSEL pin)
- 1.8 V logic compatibility
- 50 MHz SPI interface
- 2.7 V to 5.5 V power supply
- −40°C to +105°C temperature range

Pin Configurations

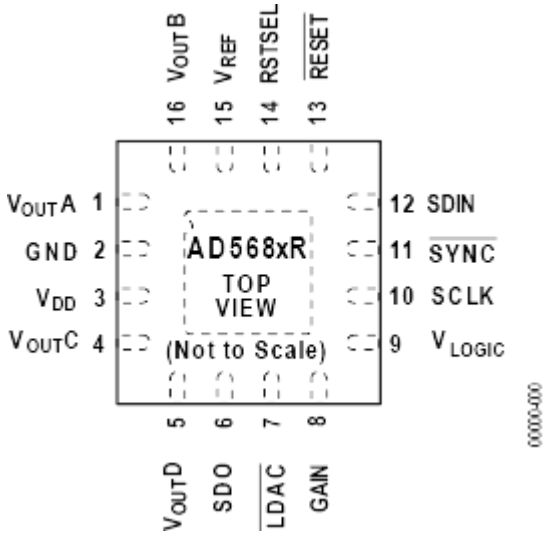

Figure 2. 16-Lead LFCSP

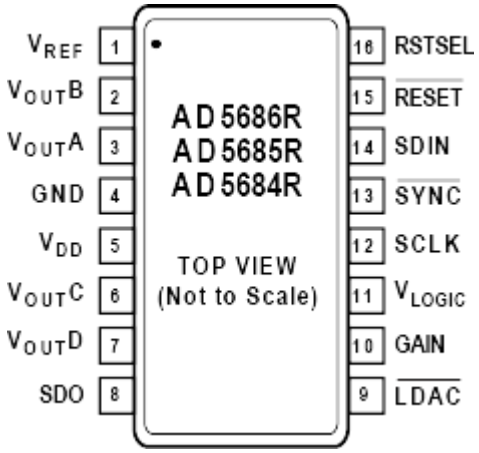

Figure 3. 16-Lead TSSOP

Table 1. Function Descriptions for Quick Start

Mnemonic	Description
$V_{OUT}A$	Analog output voltage from DAC A.
$V_{OUT}B$	Analog output voltage from DAC B.
$V_{OUT}C$	Analog output voltage from DAC C.
$V_{OUT}D$	Analog output voltage from DAC D.
$\overline{SYNC}$	Connect to serial interface.
SCLK	Connect to serial interface.
SDIN	Connect to serial interface.
SDO	No connect.
V_{REF}	No connect.
V_{DD}	Connect to 5 V supply. Decouple with 10 µF and 0.1 µF capacitors.
GND	Connect to ground.
$\overline{LDAC}$	Tie low.
RSTSEL	Tie to GND to power up to zero scale.
GAIN	Tie to GND. DAC outputs have a span from 0 V to V_{REF}.
$\overline{RESET}$	Tie high.
V_{LOGIC}	Connect to serial interface supply voltage.

Shift Register Contents

Figure 4. Shift Register Contents (AD5686R)

Table 2. Command Definitions

Command				
C3	**C2**	**C1**	**C0**	**Description**
0	0	0	0	No operation
0	0	0	1	Write to Input Register n (Dependent on LDAC)
0	0	1	0	Update DAC Register n with contents of Input Register n
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Hardware $\overline{LDAC}$ mask register
0	1	1	0	Software reset (power-on reset)
0	1	1	1	Internal reference setup register
1	0	0	0	Set up DCEN register (daisy-chain enable)
1	0	0	1	Set up readback register (readback enable)
1	0	1	0	Reserved
…	…	…	…	Reserved
1	1	1	1	Reserved

Transfer Function

$$V_{OUT} = V_{REF} \times Gain \left[\frac{D}{2^N} \right]$$

where:
D is the decimal equivalent.
N is the number of bits.

Simple Write: Example 1

To update Channel A, write the following over the serial interface: 0001 XXX1 1000000000000000 (four command bits, four address bits, 16 data bits for the AD5686R).
This updates Channel A to midscale. GAIN = 1, $V_{OUT}A$ = 1.25 V.

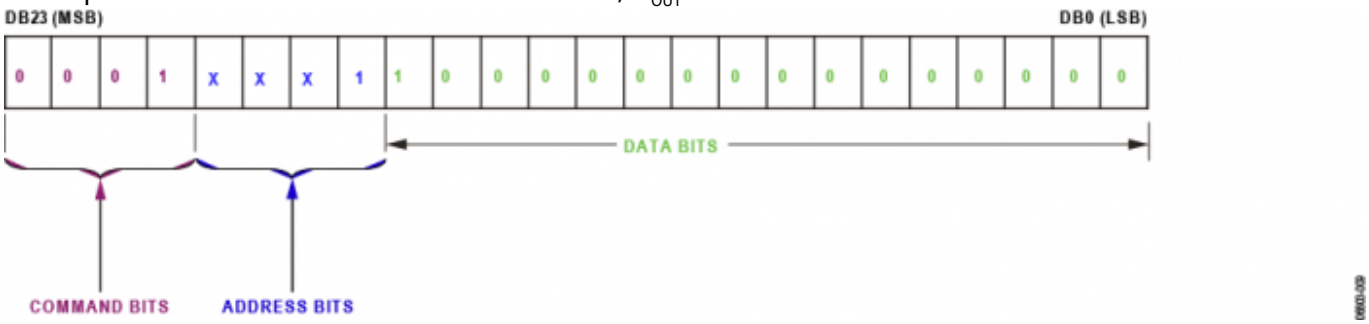

Figure 5. Simple Write—Update Channel A)

Simple Write: Example 2

To update Channel B, write the following over the serial interface: 0001 XX1X 1000000000000000.
This updates Channel B to midscale. GAIN = 1, $V_{OUT}B$ = 1.25 V.

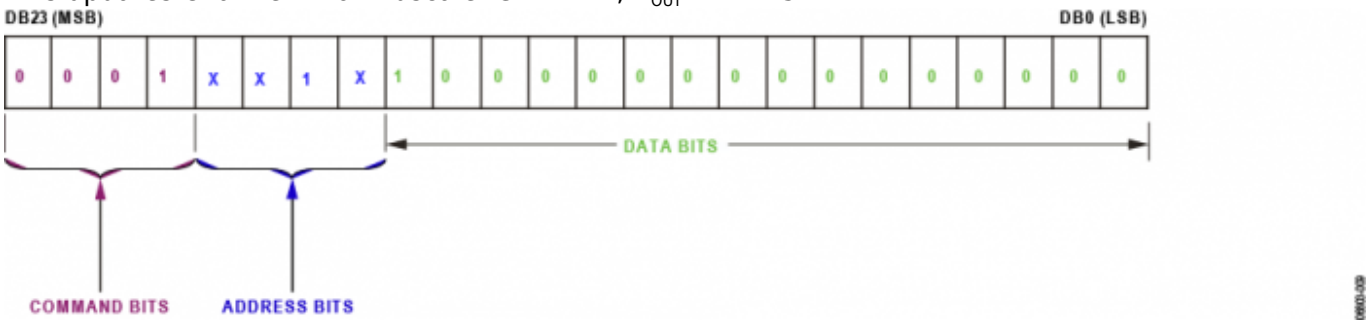

Figure 6. Simple Write—Update Channel B

Simple Write: Example 3

To update both Channel A and Channel B, write the following over the serial interface: 0001 XX11 1111111111111111. This updates both channels to full scale. GAIN = 1, $V_{OUT}B$ = 2.5 V, $V_{OUT}A$ = 2.5 V.

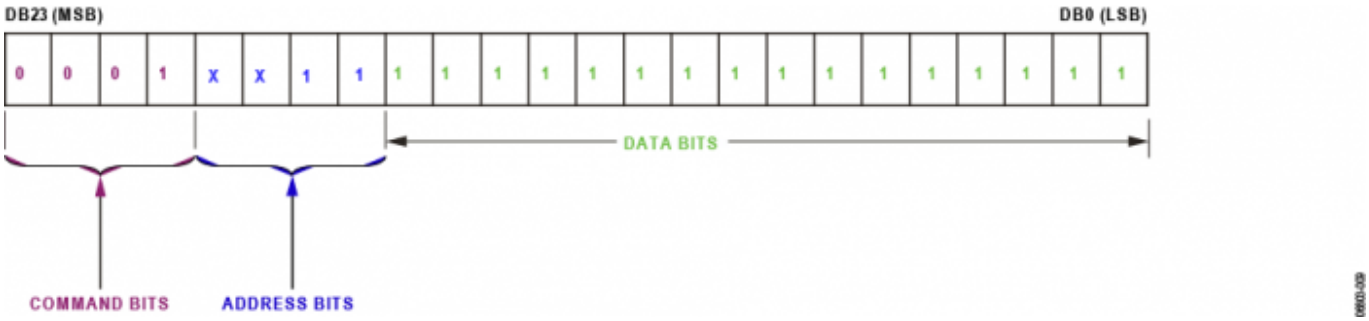

Figure 7. Simple Write—Update Channel A and Channel B