

## N-channel 40 V, 1.4 mΩ typ., 180 A STripFET™ F3 Power MOSFET in H<sup>2</sup>PAK-2 package

Datasheet – production data

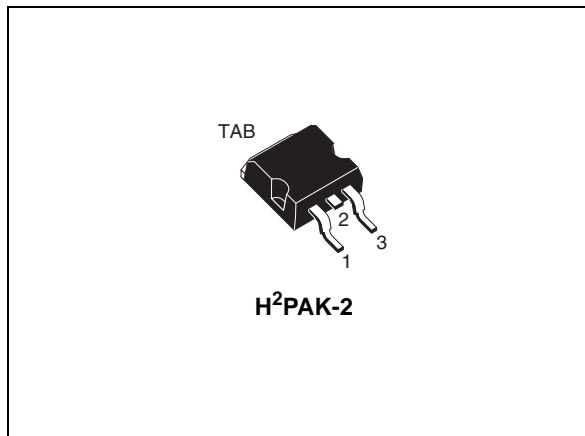
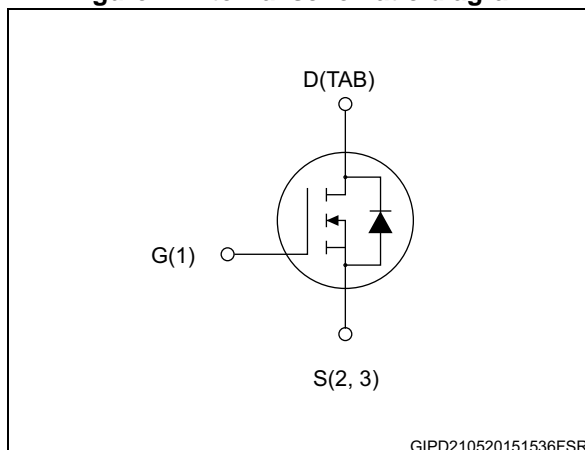


Figure 1. Internal schematic diagram



GIPD210520151536FSR

### Features

Order codes	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STH270N4F3-2	40 V	1.7 mΩ	180 A

- Conduction losses reduced
- Low profile, very low parasitic inductance, high current package

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1. Device summary

Order code	Marking	Package	Packaging
STH270N4F3-2	270N4F3	H <sup>2</sup> PAK-2	Tape and reel

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	180	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	1000	mJ
$T_{stg}$	Storage temperature	- 55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature		$^\circ\text{C}$

1. Current limited by package.
2. Pulse width limited by safe operating area
3. Starting  $T_J=25^\circ\text{C}$ ,  $I_D=80\text{ A}$ ,  $V_{DD}=32\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\ \mu\text{A}$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 40\ \text{V}$			10	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 40\ \text{V}, T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\ \text{V}$			$\pm 200$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}, I_D = 80\ \text{A}$		1.4	1.7	m $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\ \text{V}, f = 1\ \text{MHz}, V_{GS} = 0$	-	7400	-	pF
$C_{oss}$	Output capacitance		-	1800	-	pF
$C_{rss}$	Reverse transfer capacitance		-	50	-	pF
$Q_g$	Total gate charge	$V_{DD} = 20\ \text{V}, I_D = 160\ \text{A}, V_{GS} = 10\ \text{V}$ (see <a href="#">Figure 14</a> )	-	110	150	nC
$Q_{gs}$	Gate-source charge		-	30	-	nC
$Q_{gd}$	Gate-drain charge		-	25	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\ \text{V}, I_D = 80\ \text{A}, R_G = 4.7\ \Omega, V_{GS} = 10\ \text{V}$ (see <a href="#">Figure 2</a> )	-	25	-	ns
$t_r$	Rise time		-	180	-	ns
$t_{d(off)}$	Turn-off delay time		-	110	-	ns
$t_f$	Fall time		-	45	-	ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		180	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		720	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 180 \text{ A}, V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 160 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 32 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	70		ns
$Q_{rr}$	Reverse recovery charge		-	225		nC
$I_{RRM}$	Reverse recovery current		-	3.2		A

1. Current limited by package
2. Pulse width limited by safe operating area.
3. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

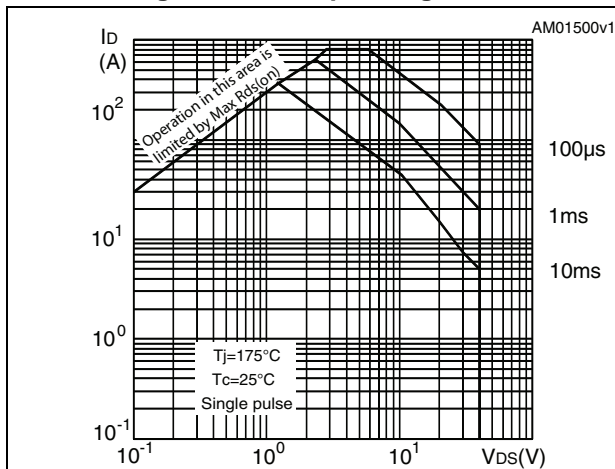


Figure 3. Thermal impedance

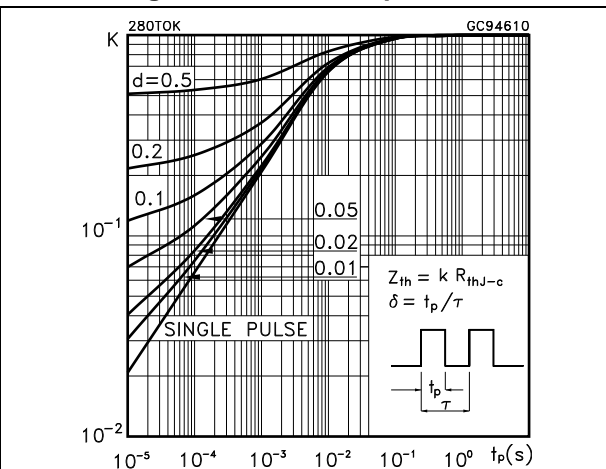


Figure 4. Output characteristics

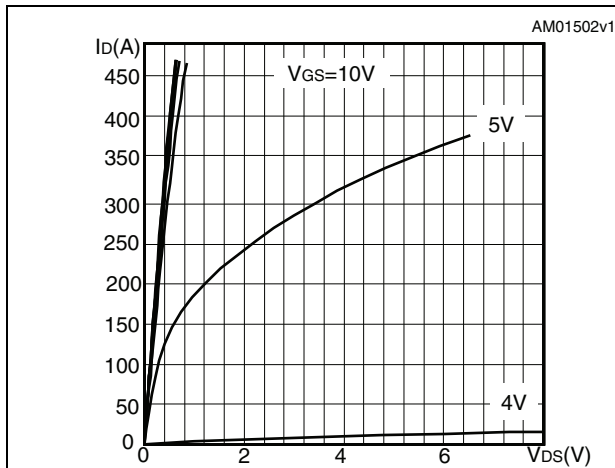


Figure 5. Transfer characteristics

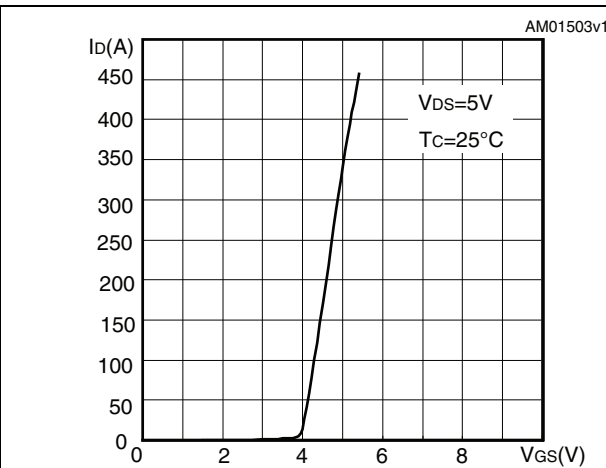


Figure 6. Gate charge vs gate-source voltage

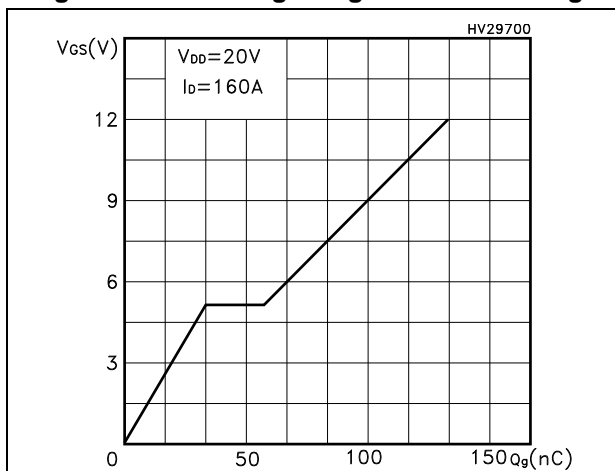


Figure 7. Static drain-source on-resistance

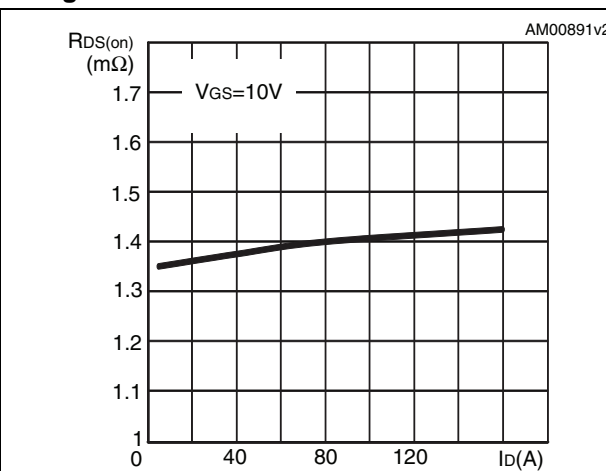


Figure 8. Capacitance variations

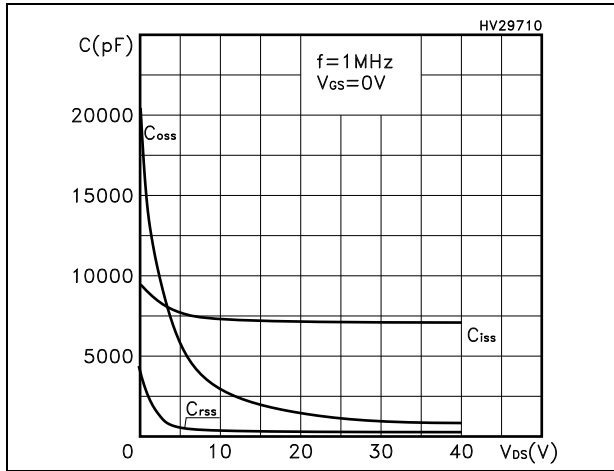


Figure 9. Normalized gate threshold voltage vs temperature

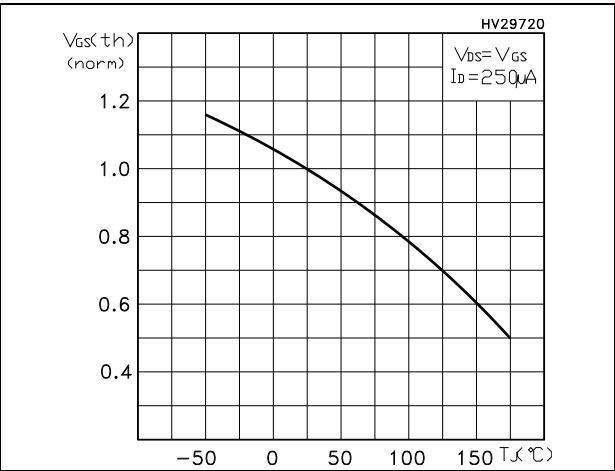


Figure 10. Normalized on-resistance vs temperature

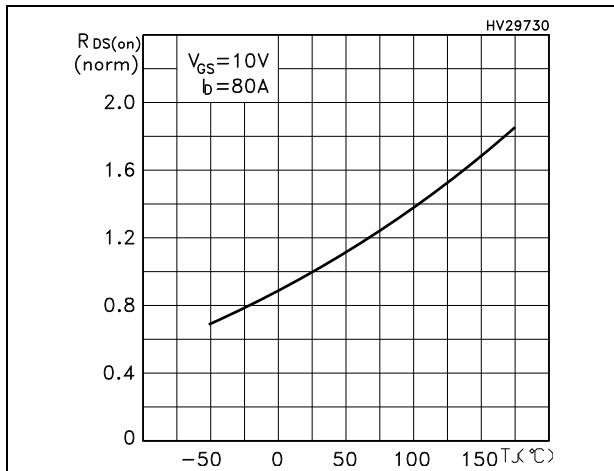


Figure 11. Normalized V<sub>(BR)DSS</sub> vs temperature

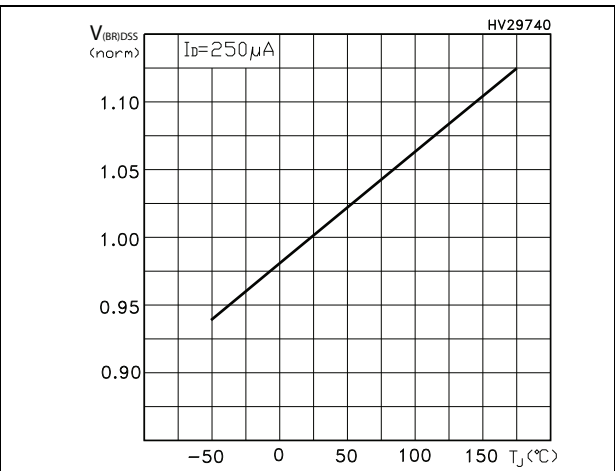
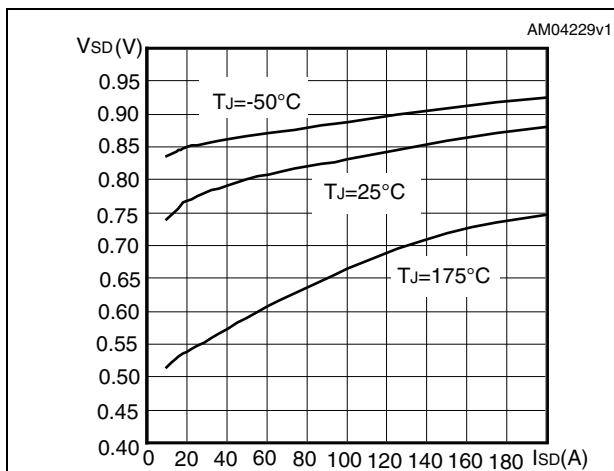


Figure 12. Drain-source diode forward characteristics



### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



AM01468v1

**Figure 14. Gate charge test circuit**



AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**



AM01470v1

**Figure 16. Unclamped inductive load test circuit**



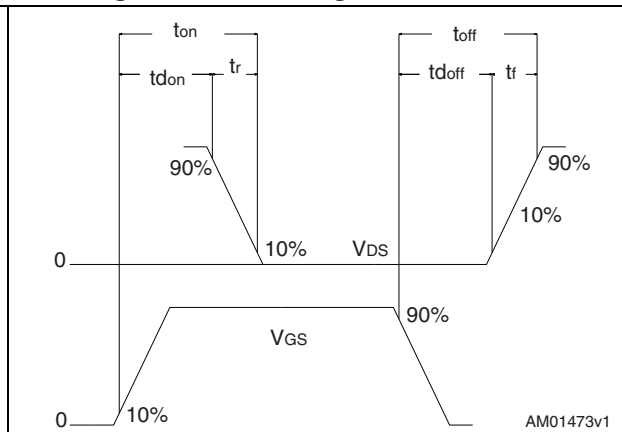
AM01471v1

**Figure 17. Unclamped inductive waveform**



AM01472v1

**Figure 18. Switching time waveform**



AM01473v1

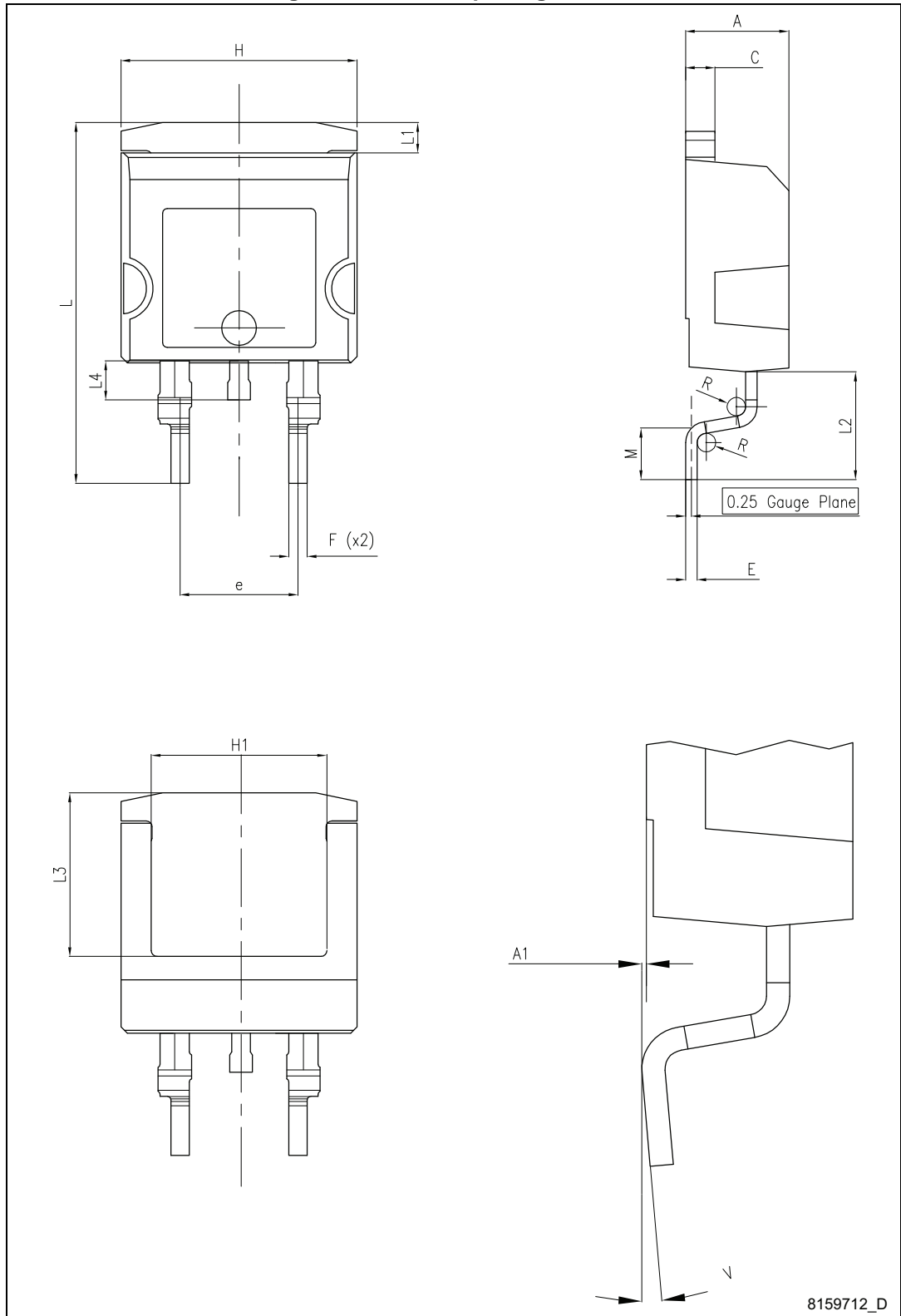


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 H<sup>2</sup>PAK-2 package information

Figure 19. H<sup>2</sup>PAK-2 package outline

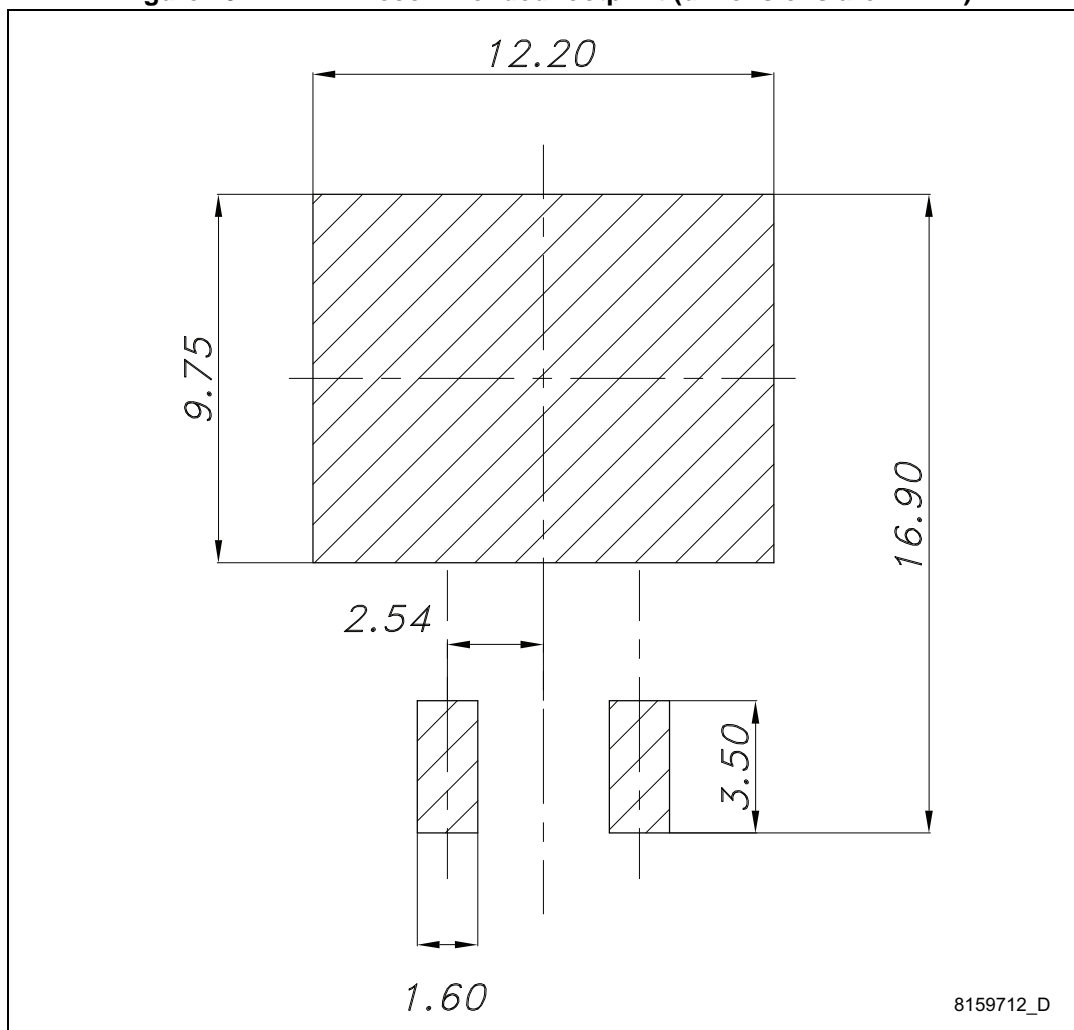


8159712\_D

Table 8. H<sup>2</sup>PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20. H<sup>2</sup>PAK-2 recommended footprint (dimensions are in mm)



# 5 Packing information

Figure 21. Tape

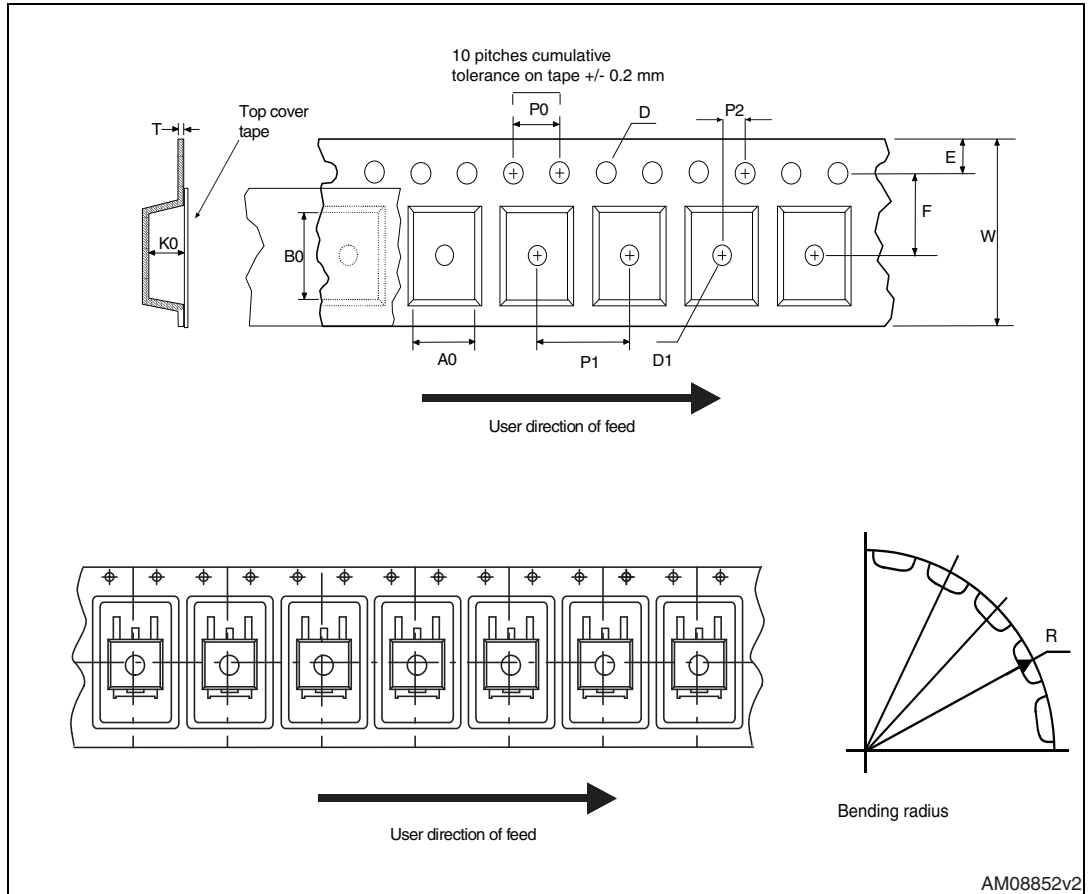


Figure 22. Reel

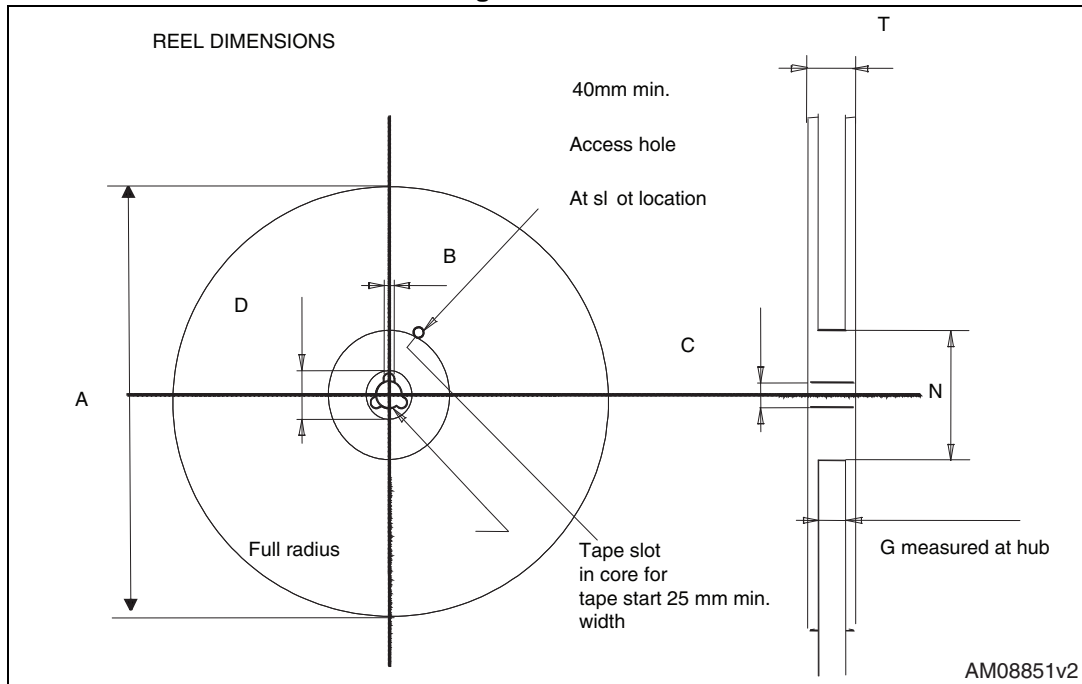


Table 9. H<sup>2</sup>PAK-2 and H<sup>2</sup>PAK-6 tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
15-Jan-2010	1	First release.
14-Mar-2013	2	<ul style="list-style-type: none"><li>– Added: H<sup>2</sup>PAK-2 package</li><li>– Updated: <a href="#">Section 4: Package information</a> and <a href="#">Section 5: Packing information</a></li><li>– Minor text changes</li></ul>
21-May-2015	3	<ul style="list-style-type: none"><li>– The part number STH270N4F3-6 has been moved to a separate datasheet.</li><li>– Updated title and description in cover page.</li><li>– Updated <a href="#">Section 4: Package information</a>.</li><li>– Minor text changes</li></ul>

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