# TSV6390, TSV6390A, TSV6391, TSV6391A

## Micropower (60 µA), wide bandwidth (2.4 MHz) CMOS operational amplifiers

Datasheet - production data



TSV6390ICT/ILT
SC70-6/SOT23-6



TSV6391ICT/ILT
SC70-5/SOT23-5
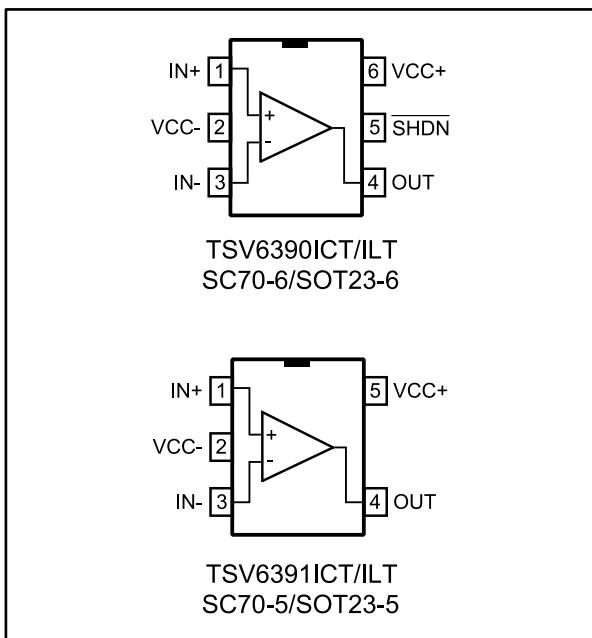
## Features

- Low offset voltage: 500 µV max (A version)
- Low power consumption: 60 µA typ at 5 V
- Low supply voltage: 1.5 V – 5.5 V
- Gain bandwidth product: 2.4 MHz typical
- Stable in gain configuration (-3 or 4)
- Low power shutdown mode: 5 nA typical
- High output current: 63 mA at $V_{CC}$ = 5 V
- Low input bias current: 1 pA typical
- Rail-to-rail input and output
- Extended temperature range:
  -40 °C to 125 °C
- 4 kV human body model

## Applications

- Battery-powered applications
- Portable devices

- Signal conditioning
- Active filtering
- Medical instrumentation

## Description

The TSV6390, TSV6391, and their "A" versions are single operational amplifiers (op amps) offering low voltage, low power operation, and rail-to-rail input and output.

With a very low input bias current and low offset voltage (500 µV maximum for the A version), the TSV6390 and TSV6391 are ideal for applications requiring precision. The devices can operate at power supplies ranging from 1.5 to 5.5 V, and are therefore ideal for battery-powered devices, extending battery life.

When used with a gain (above -3 or 4), these products feature an excellent speed/power consumption ratio, offering a 2.4 MHz gain bandwidth product while consuming only 60 µA at a 5 V supply voltage.

The TSV6390 comes with a shutdown function.

Both the TSV6390 and TSV6391 have a high tolerance to ESD, sustaining 4 kV for the human body model.

They are offered in micropackages, SC70-6 and SOT23-6 for the TSV6390 and SC70-5 and SOT23-5 for the TSV6391. They are guaranteed for industrial temperature ranges from -40 °C to 125 °C.

All these features combined make the TSV6390 and TSV6391 ideal for sensor interfaces, battery-supplied, and portable applications, as well as active filtering.

# Contents

# 1    Absolute maximum ratings and operating conditions

**Table 1: Absolute maximum ratings (AMR)**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage [1] | | 6 | V |
| $V_{id}$ | Differential input voltage [2] | | $\pm V_{CC}$ | |
| $V_{in}$ | Input voltage [3] | | $(V_{CC-})$ - 0.2 to $(V_{CC+})$ + 0.2 | |
| $I_{in}$ | Input current [4] | | 10 | mA |
| $\overline{SHDN}$ | Shutdown voltage [3] | | $(V_{CC-})$ - 0.2 to $(V_{CC+})$ + 0.2 | V |
| $T_{stg}$ | Storage temperature | | -65 to 150 | °C |
| $T_j$ | Maximum junction temperature | | 150 | |
| $R_{thja}$ | Thermal resistance junction to ambient [5][6] | SC70-6 | 232 | °C/W |
| | | SOT23-6 | 240 | |
| | | SC70-5 | 205 | |
| | | SOT23-5 | 250 | |
| ESD | HBM: human body model [7] | | 4 | kV |
| | MM: machine model [8] | | 300 | V |
| | CDM: charged device model [9] | | 1.5 | kV |
| | Latch-up immunity | | 200 | mA |

**Notes:**

[1]All voltage values, except the differential voltage, are with respect to network ground terminal.

[2]The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.

[3]$V_{CC}$- $V_{in}$ must not exceed 6 V, $V_{in}$ must not exceed 6 V.

[4]Input current must be limited by a resistor in series with the inputs.

[5]$R_{th}$ are typical values.

[6]Short-circuits can cause excessive heating and destructive dissipation.

[7]Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

[8]Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.

[9]Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

**Table 2: Operating conditions**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | 1.5 to 5.5 | V |
| $V_{icm}$ | Common mode input voltage range | $(V_{CC-})$ - 0.1 to $(V_{CC+})$ + 0.1 | |
| $T_{oper}$ | Operating free air temperature range | -40 to 125 | °C |

# 2 Electrical characteristics

**Table 3: Electrical characteristics at VCC+ = 1.8 V with VCC- = 0 V, Vicm = VCC/2,
Tamb = 25 °C and RL connected to VCC/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $V_{io}$ | Offset voltage | TSV6390 and TSV6391 | | | 3 | mV |
| | | TSV6390A and TSV6391A | | | 0.5 | |
| | | $T_{min} < T_{op} < T_{max}$, TSV6390 and TSV6391 | | | 4.5 | |
| | | $T_{min} < T_{op} < T_{max}$, TSV6390A and TSV6391A | | | 2 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | | | 2 | | µV/°C |
| $I_{io}$ | Input offset current, $V_{out} = V_{CC}/2$ [(1)] | | | 1 | 10 | pA |
| | | $T_{min} < T_{op} < T_{max}$ | | 1 | 100 | |
| $I_{ib}$ | Input bias current, $(V_{out} = V_{CC}/2)$ [(1)] | | | 1 | 10 | |
| | | $T_{min} < T_{op} < T_{max}$ | | 1 | 100 | |
| CMR | Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$) | 0 V to 1.8 V, $V_{out} = 0.9$ V | 53 | 74 | | dB |
| | | $T_{min} < T_{op} < T_{max}$ | 51 | | | |
| $A_{vd}$ | Large signal voltage gain | $R_L = 10$ kΩ, $V_{out} = 0.5$ V to 1.3 V | 85 | 95 | | |
| | | $T_{min} < T_{op} < T_{max}$ | 80 | | | |
| $V_{OH}$ | High-level output voltage | $R_L = 10$ kΩ | | 5 | 35 | mV |
| | | $T_{min} < T_{op} < T_{max}$ | | | 50 | |
| $V_{OL}$ | Low-level output voltage | $R_L = 10$ kΩ | | 4 | 35 | |
| | | $T_{min} < T_{op} < T_{max}$ | | | 50 | |
| $I_{out}$ | $I_{sink}$ | $V_{out} = 1.8$ V | 6 | 12 | | mA |
| | | $T_{min} < T_{op} < T_{max}$ | 4 | | | |
| | $I_{source}$ | $V_{out} = 0$ V | 6 | 10 | | |
| | | $T_{min} < T_{op} < T_{max}$ | 4 | | | |
| $I_{CC}$ | Supply current, $\overline{SHDN} = V_{CC}$ | No load, $V_{out} = V_{CC}/2$ | 40 | 50 | 60 | µA |
| | | $T_{min} < T_{op} < T_{max}$ | | | 62 | |
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L = 10$ kΩ, $C_L = 100$ pF | | 2 | | MHz |
| Gain | Minimum gain for stability | Phase margin = 60°, $R_f = 10$ kΩ, $R_L = 10$ kΩ, $C_L = 20$ pF | | 4 | | V/V |
| | | | | -3 | | |
| SR | Slew rate | $R_L = 10$ kΩ, $C_L = 100$ pF, $V_{out} = 0.5$ V to 1.3 V | | 0.7 | | V/µs |
| $e_n$ | Equivalent input noise voltage | f = 1 kHz | | 60 | | nV/√Hz |
| | | f = 10 kHz | | 33 | | |

**Notes:**

[(1)]Guaranteed by design.

**Table 4: Shutdown characteristics VCC = 1.8 V (TSV6390)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|------------|------|------|------|------|
| **DC performance** | | | | | | |
| $I_{CC}$ | Supply current in shutdown mode (all operators) | $\overline{SHDN}$ = $V_{CC-}$ | | 2.5 | 50 | nA |
| | | $T_{min} < T_{op} < 85\ °C$ | | | 200 | |
| | | $T_{min} < T_{op} < 125\ °C$ | | | 1.5 | µA |
| $t_{on}$ | Amplifier turn-on time | $R_L$ = 2 kΩ, $V_{out}$ = ($V_{CC-}$) to ($V_{CC-}$) + 0.2 V | | 300 | | ns |
| $t_{off}$ | Amplifier turn-off time | $R_L$ = 2 kΩ, Vout = ($V_{CC+}$) - 0.5 V to ($V_{CC+}$) - 0.7 V | | 20 | | |
| $V_{IH}$ | $\overline{SHDN}$ logic high | | 1.3 | | | V |
| $V_{IL}$ | $\overline{SHDN}$ logic low | | | | 0.5 | |
| $I_{IH}$ | $\overline{SHDN}$ current high | $\overline{SHDN}$ = $V_{CC+}$ | | 10 | | pA |
| $I_{IL}$ | $\overline{SHDN}$ current low | $\overline{SHDN}$ = $V_{CC-}$ | | 10 | | |
| $I_{OLeak}$ | Output leakage in shutdown mode | $\overline{SHDN}$ = $V_{CC-}$ | | 50 | | |
| | | $T_{min} < T_{op} < T_{max}$ | | 1 | | nA |

**Table 5: VCC+ = 3.3 V, VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C, RL connected to VCC/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|------------|------|------|------|------|
| **DC performance** | | | | | | |
| $V_{io}$ | Offset voltage | TSV6390 and TSV6391 | | | 3 | mV |
| | | TSV6390A and TSV6391A | | | 0.5 | |
| | | $T_{min} < T_{op} < T_{max,}$ TSV6390 and TSV6391 | | | 4.5 | |
| | | $T_{min} < T_{op} < T_{max,}$ TSV6390A and TSV6391A | | | 2 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | | | 2 | | µV/°C |
| $I_{io}$ | Input offset current [(1)] | | | 1 | 10 | pA |
| | | $T_{min} < T_{op} < T_{max}$ | | 1 | 100 | |
| $I_{ib}$ | Input bias current [(1)] | | | 1 | 10 | |
| | | $T_{min} < T_{op} < T_{max}$ | | 1 | 100 | |
| CMR | Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$) | 0 V to 3.3 V, $V_{out}$ = 1.65 V | 57 | 79 | | dB |
| | | $T_{min} < T_{op} < T_{max}$ | 53 | | | |
| $A_{vd}$ | Large signal voltage gain | $R_L$ = 10 kΩ, $V_{out}$ = 0.5 V to 2.8 V | 88 | 98 | | |
| | | $T_{min} < T_{op} < T_{max}$ | 83 | | | |
| $V_{OH}$ | High-level output voltage | $R_L$ = 10 kΩ | | 6 | 35 | mV |
| | | $T_{min.} < T_{op} < T_{max}$ | | | 50 | |
| $V_{OL}$ | Low-level output voltage | $R_L$ = 10 kΩ | | 7 | 35 | |
| | | $T_{min} < T_{op} < T_{max}$ | | | 50 | |
| $I_{out}$ | $I_{sink}$ | $V_{out}$ = 3.3 V | 23 | 45 | | mA |
| | | $T_{min} < T_{op} < T_{max}$ | 20 | 42 | | |
| | $I_{source}$ | $V_{out}$ = 0 V | 23 | 38 | | |
| | | $T_{min} < T_{op} < T_{max}$ | 20 | | | |
| $I_{CC}$ | Supply current, $\overline{SHDN}$ = $V_{CC}$ | No load, $V_{out}$ = $V_{CC}$/2 | 43 | 55 | 64 | µA |
| | | $T_{min} < T_{op} < T_{max}$ | | | 66 | |
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 2.2 | | MHz |
| Gain | Minimum gain for stability | Phase margin = 60°, $R_f$ = 10 kΩ, $R_L$ = 10 kΩ, $C_L$ = 20 pF, | | 4 | | V/V |
| | | | | -3 | | |
| SR | Slew rate | $R_L$ = 10 kΩ, $C_L$ = 100 pF, $V_{out}$ = 0.5 V to 2.8 V | | 0.9 | | V/µs |
| $e_n$ | Equivalent input noise voltage | f = 1 kHz | | 65 | | nV/√Hz |

**Notes:**

[(1)]Guaranteed by design.

**Table 6: Electrical characteristics at VCC+ = 5 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25 °C and RL connected to VCC/2 (unless otherwise specified)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------|------|------|------|------|
| **DC performance** | | | | | | |
| $V_{io}$ | Offset voltage | TSV6390 and TSV6391 | | | 3 | mV |
| | | TSV6390A and TSV6391A | | | 0.5 | |
| | | $T_{min} < T_{op} < T_{max,}$ TSV6390 and TSV6391 | | | 4.5 | |
| | | $T_{min} < T_{op} < T_{max,}$ TSV6390A and TSV6391A | | | 2 | |
| $\Delta V_{io}/\Delta T$ | Input offset voltage drift | | | 2 | | µV/°C |
| $I_{io}$ | Input offset current, $V_{out} = V_{CC}/2$ [(1)] | | | 1 | 10 | pA |
| | | $T_{min} < T_{op} < T_{max}$ | | 1 | 100 | |
| $I_{ib}$ | Input bias current, $V_{out} = V_{CC}/2$ [(1)] | | | 1 | 10 | pA |
| | | $T_{min} < T_{op} < T_{max}$ | | 1 | 100 | |
| CMR | Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$) | 0 V to 5 V, $V_{out}$ = 2.5 V | 60 | 80 | | dB |
| | | $T_{min} < T_{op} < T_{max}$ | 55 | | | |
| SVR | Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$) | $V_{CC}$ = 1.8 to 5 V | 75 | 93 | | dB |
| | | $T_{min} < T_{op} < T_{max}$ | 73 | | | |
| $A_{vd}$ | Large signal voltage gain | $R_L$= 10 kΩ, $V_{out}$ = 0.5 V to 4.5 V | 89 | 98 | | dB |
| | | $T_{min} < T_{op} < T_{max}$ | 84 | | | |
| $V_{OH}$ | High-level output voltage | $R_L$ = 10 kΩ | | 7 | 35 | mV |
| | | $T_{min} < T_{op} < T_{max}$ | | | 50 | |
| $V_{OL}$ | Low-level output voltage | $R_L$ = 10 kΩ | | 6 | 35 | mV |
| | | $T_{min} < T_{op} < T_{max}$ | | | 50 | |
| $I_{out}$ | $I_{sink}$ | $V_{out}$ = 5 V | 40 | 65 | | mA |
| | | $T_{min} < T_{op} < T_{max}$ | 35 | | | |
| | $I_{source}$ | $V_{out}$ = 0 V | 40 | 72 | | |
| | | $T_{min} < T_{op} < T_{max}$ | 35 | | | |
| $I_{CC}$ | Supply current, $\overline{SHDN}$ = $V_{CC}$ | No load, $V_{out} = V_{CC}/2$ | 50 | 60 | 69 | µA |
| | | $T_{min} < T_{op} < T_{max}$ | | | 72 | |
| **AC performance** | | | | | | |
| GBP | Gain bandwidth product | $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 2.4 | | MHz |
| Gain | Minimum gain for stability | Phase margin = 60°, $R_f$ = 10 kΩ, $R_L$ = 10 kΩ, $C_L$ = 20 pF, | | 4 | | V/V |
| | | | | -3 | | |
| SR | Slew rate | $R_L$ = 10 kΩ, $C_L$ = 100 pF | | 1.1 | | V/µs |
| $e_n$ | Equivalent input noise voltage | f = 1 kHz | | 60 | | nV/√Hz |
| | | f = 10 kHz | | 33 | | |
| THD+N | Total harmonic distortion + noise | Av = -10, $f_{in}$ = 1 kHz, R = 100 kΩ, $V_{icm}$ = Vcc/2, $V_{in}$ = 40 mVpp | | 0.11 | | % |

**Notes:**

[(1)]Guaranteed by design.

**Table 7: Shutdown characteristics VCC = 5 V (TSV6390)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC performance** | | | | | | |
| $I_{CC}$ | Supply current in shutdown mode (all operators) | $\overline{SHDN}$ = $V_{CC-}$ | | 5 | 50 | nA |
| | | $T_{min} < T_{op} < 85$ °C | | | 200 | |
| | | $T_{min} < T_{op} < 125$ °C | | | 1.5 | µA |
| $t_{on}$ | Amplifier turn-on time | $R_L = 2$ kΩ, $V_{out}$ = ($V_{CC-}$) to ($V_{CC-}$) + 0.2 V | | 300 | | ns |
| $t_{off}$ | Amplifier turn-off time | $R_L = 2$ kΩ, Vout = ($V_{CC+}$) - 0.5 V to ($V_{CC+}$) - 0.7 V | | 30 | | |
| $V_{IH}$ | $\overline{SHDN}$ logic high | | 4.5 | | | V |
| $V_{IL}$ | $\overline{SHDN}$ logic low | | | | 0.5 | |
| $I_{IH}$ | $\overline{SHDN}$ current high | $\overline{SHDN}$ = $V_{CC+}$ | | 10 | | pA |
| $I_{IL}$ | $\overline{SHDN}$ current low | $\overline{SHDN}$ = $V_{CC-}$ | | 10 | | |
| $I_{OLeak}$ | Output leakage in shutdown mode | $\overline{SHDN}$ = $V_{CC-}$ | | 50 | | |
| | | $T_{min} < T_{op} < T_{max}$ | | 1 | | nA |

# 3      Electrical characteristics curves



Figure 1: Supply current vs. supply voltage at Vicm = VCC/2
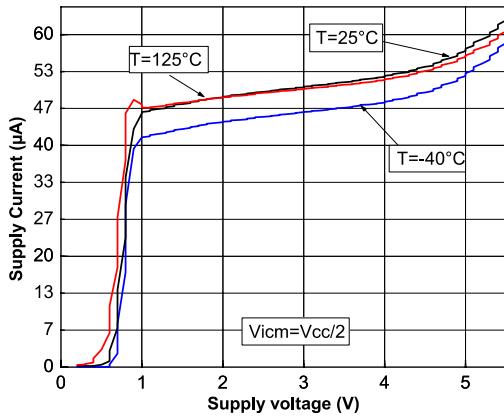


Figure 2: Output current vs. output voltage at VCC = 1.5 V
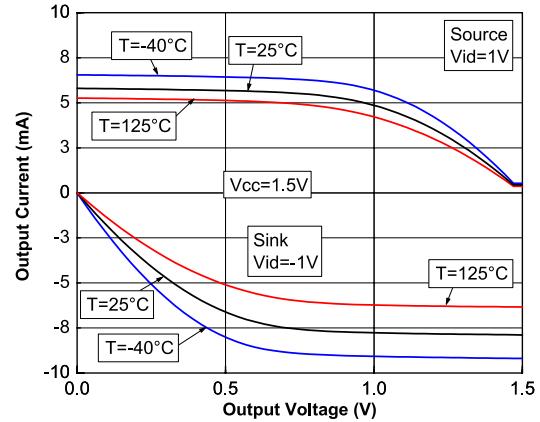


Figure 3: Output current vs. output voltage at VCC = 5 V
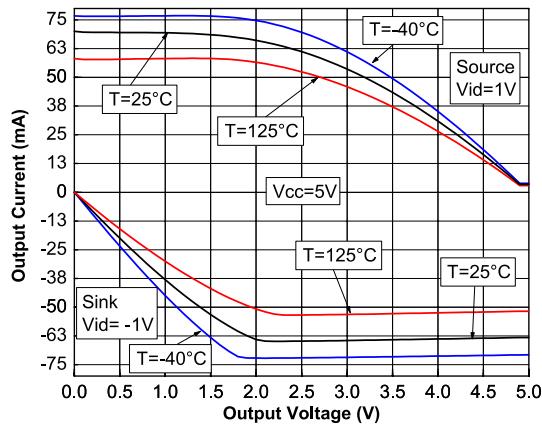


Figure 4: Peaking at closed loop gain = -10
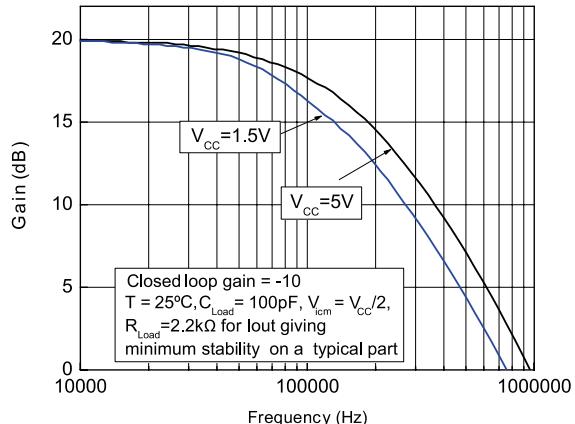


Figure 5: Peaking at closed loop gain = -3 at VCC = 1.5 V
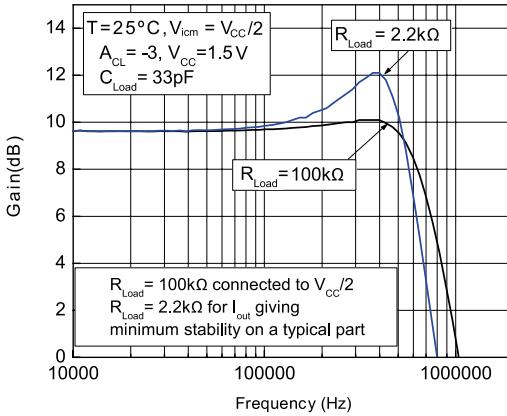


Figure 6: Peaking at closed loop gain = -3 at VCC = 5 V

Figure 7: Positive slew rate vs. supply voltage

$R_{Load}$ = 2 kΩ, $C_{Load}$ = 100 pF, $A_{CL}$ = -10
$V_{in}$: from 0.5 V to ($V_{CC+}$) - 0.5 V
SR calculated from 10 % to 90 %

T= 25°C
T= 125°C
T= −40°C

Slew rate (V/µs) vs. Supply voltage (V)
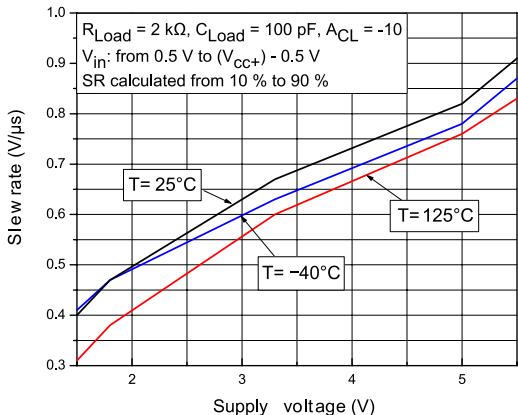
Figure 8: Negative slew rate vs. supply voltage

$R_{Load}$ = 2kΩ, $C_{Load}$ = 100pF, $A_{CL}$ = −10
$V_{in}$: from $V_{CC+}$ − 0.5V to 0.5V
SR calculated from 10% to 90%
$V_{icm}$ = $V_{CC}$ /2

T=125°C
T=−40°C
T=25°C

Slew rate (V/µs) vs. Supply voltage (V)
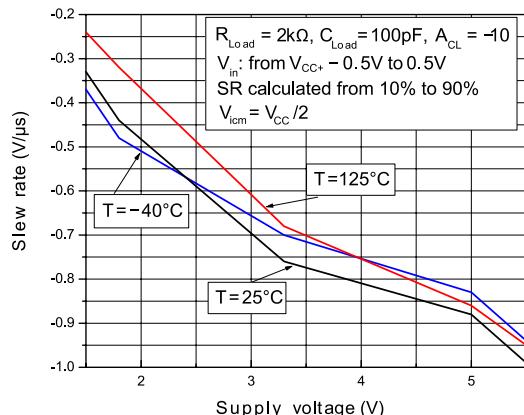
Figure 9: Distortion + noise vs. output voltage at VCC = 1.8 V

$V_{CC}$ = 1.8 V, T = 25 °C
$V_{icm}$ = $V_{CC}$/2, $A_{CL}$ = -10
$F_{in}$ = 1 kHz, $C_{Load}$ = 100 pF

$R_{Load}$ = 2 kΩ
$R_{Load}$ = 100 kΩ

THD + N (%) vs. Output voltage (Vrms)
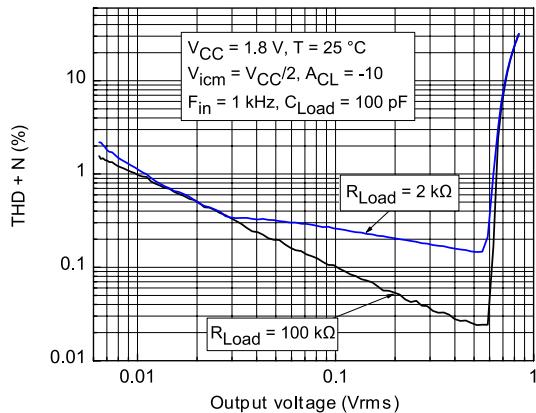
Figure 10: Distortion + noise vs. output voltage at VCC = 5 V

$V_{CC}$ = 5 V, T = 25 °C
$V_{icm}$ = $V_{CC}$/2, $A_{CL}$ = -10
$F_{in}$ = 1 kHz, $C_{Load}$ = 100 pF

$R_{Load}$ = 2 kΩ
$R_{Load}$ = 100 kΩ

THD + N (%) vs. Ouput voltage ($V_{rms}$)
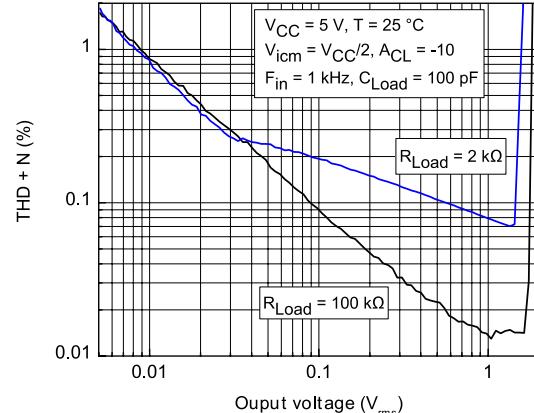
Figure 11: Slew rate timing

$R_{Load}$ = 2 kΩ, $C_{Load}$ = 100 pF
$V_{icm}$ = $V_{CC}$ /2, $A_{CL}$ = -10
T = 25 °C, $V_{CC}$ = 5 V

$V_{out}$
$V_{in}$

Amplitude (V) vs. Time (µs)
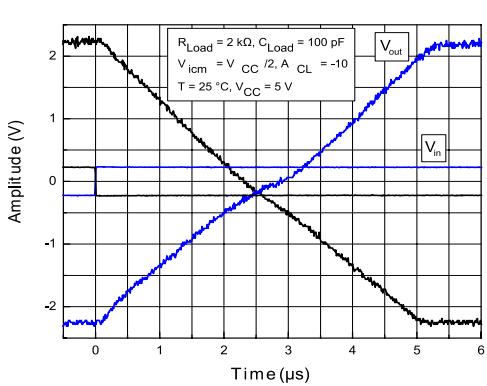
Figure 12: Noise vs. frequency at VCC = 5 V

Vicm = 2.5 V
Vicm = 4.5 V
Vcc = 5 V
Tamb = 25 °C

Equivalent Input Voltage Noise (nV/√Hz) vs. Frequency (Hz)
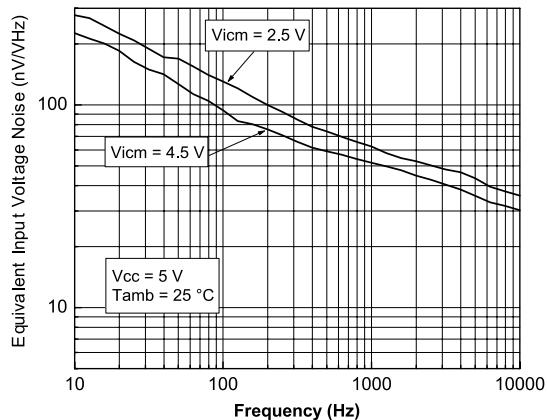
# 4 Application information

## 4.1 Operating voltages

The TSV6390 and TSV6391 can operate from 1.5 to 5.5 V. Their parameters are fully specified for 1.8, 3.3 and 5 V power supplies. However, the parameters are very stable in the full $V_{CC}$ range and several characterization curves show the TSV639x characteristics at 1.5 V. Additionally, the main specifications are guaranteed in extended temperature ranges from -40 °C to 125 °C.

## 4.2 Rail-to-rail input

The TSV6390 and TSV6391 are built with two complementary PMOS and NMOS input differential pairs. The devices have a rail-to-rail input, and the input common mode range is extended from $(V_{CC-})$ - 0.1 V to $(V_{CC+})$ + 0.1 V. The transition between the two pairs appears at $(V_{CC+})$ - 0.7 V. In the transition region, the performance of CMRR, PSRR, $V_{io}$, and THD is slightly degraded (as shown in *Figure 13* and *Figure 14* for $V_{io}$ vs. $V_{icm}$).



Figure 13: Input offset voltage vs input common-mode at VCC = 1.5 V
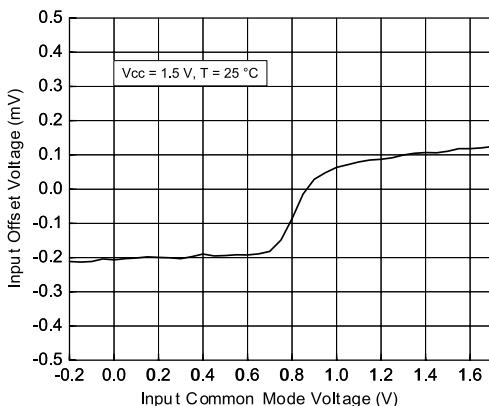


Figure 14: Input offset voltage vs input common-mode at VCC = 5 V
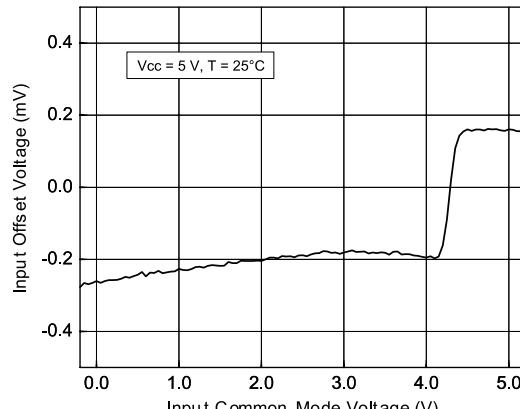
The devices are guaranteed without phase reversal.

## 4.3 Rail-to-rail output

The operational amplifiers' output levels can go close to the rails: 35 mV maximum above and below the rail when connected to a 10 kΩ resistive load to $V_{CC}/2$.

## 4.4 Shutdown function (TSV6390)

The operational amplifier is enabled when the $\overline{\text{SHDN}}$ pin is pulled high. To disable the amplifier, the $\overline{\text{SHDN}}$ must be pulled down to $V_{CC-}$. When in shutdown mode, the amplifier's output is in a high impedance state. The $\overline{\text{SHDN}}$ pin must never be left floating, but kept tied to $V_{CC+}$ or $V_{CC-}$.

The turn-on and turn-off times are calculated for an output variation of ±200 mV (*Figure 15* and *Figure 16* show the test configurations).



Figure 15: Test configuration for turn-on time (Vout pulled down)
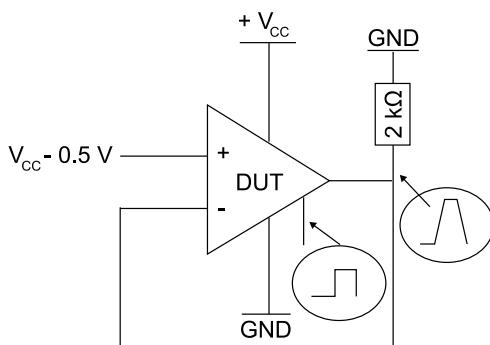


Figure 16: Test configuration for turn-off time (Vout pulled down)
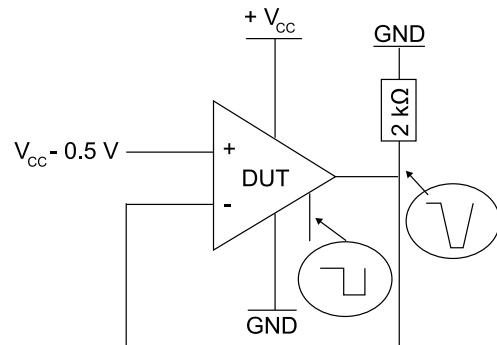


Figure 17: Turn-on time, VCC = 5 V, Vout pulled down, T = 25 °C
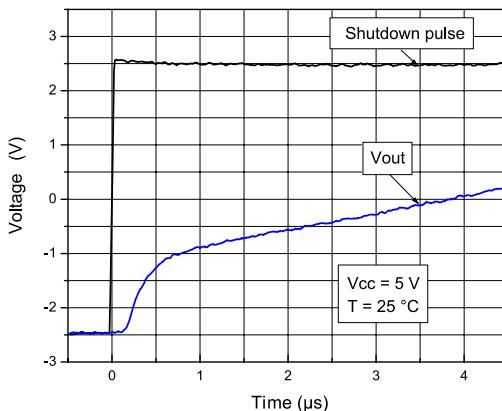


Figure 18: Turn-off time, VCC = 5 V, Vout pulled down, T = 25 °C
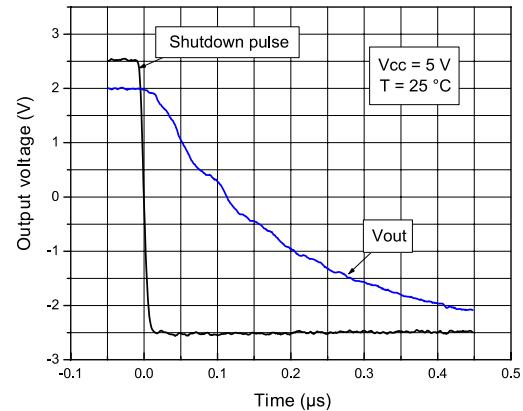
## 4.5 Optimization of DC and AC parameters

These devices use an innovative approach to reduce the spread of the main DC and AC parameters. An internal adjustment achieves a very narrow spread of the current consumption (60 µA typical, min/max at ±17 %). Parameters linked to the current consumption value, such as GBP, SR, and $A_{Vd}$, benefit from this narrow dispersion.

## 4.6 Driving resistive and capacitive loads

These products are micropower, low-voltage operational amplifiers optimized to drive rather large resistive loads, above 2 kΩ. For lower resistive loads, the THD level may significantly increase.

These operational amplifiers have a relatively low internal compensation capacitor, making them very fast while consuming very little. They are ideal when used in a non-inverting configuration or in an inverting configuration in the following conditions.

- |Gain| ≥ 3 in an inverting configuration ($C_L$ = 20 pF, $R_L$ = 100 kΩ) or |gain| ≥ 10, ($C_L$ = 100 pF, $R_L$ = 100 kΩ)
- Gain ≥ 4 in a non-inverting configuration ($C_L$ = 20 pF, $R_L$ = 100 kΩ) or gain ≥ 11, ($C_L$ = 100 pF, $R_L$ = 100 kΩ)

As these operational amplifiers are not unity gain stable, for a low closed-loop gain it is recommended to use the TSV62x (29 µA, 420 kHz) or TSV63x (60 µA, 880 kHz) which are unity gain stable.

**Table 8: Related products**

| Part # | Icc (µA) at 5 V | GBP (MHz) | SR (V/µs) | Minimum gain for stability ($C_{Load}$ = 100 pF) |
|---|---|---|---|---|
| TSV620-1 | 29 | 0.42 | 0.14 | 1 |
| TSV6290-1 | 29 | 1.3 | 0.5 | 11 |
| TSV630-1 | 60 | 0.88 | 0.34 | 1 |
| TSV6390-1 | 60 | 2.4 | 1.1 | 11 |

## 4.7 PCB layouts

For correct operation, it is advised to add 10 nF decoupling capacitors as close as possible to the power supply pins.

## 4.8 Macromodel

An accurate macromodel of the TSV6390 and TSV6391 is available on STMicroelectronics' web site at: **www.st.com**. This model is a trade-off between accuracy and complexity (that is, time simulation) of the TSV639x operational amplifiers. It emulates the nominal performances of a typical device within the specified operating conditions mentioned in the datasheet. It also helps to validate a design approach and to select the right operational amplifier, *but it does not replace on-board measurements*.

# 5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 5.1 SC70-6 (or SOT323-6) package information

**Figure 19: SC70-6 (or SOT323-6) package outline**
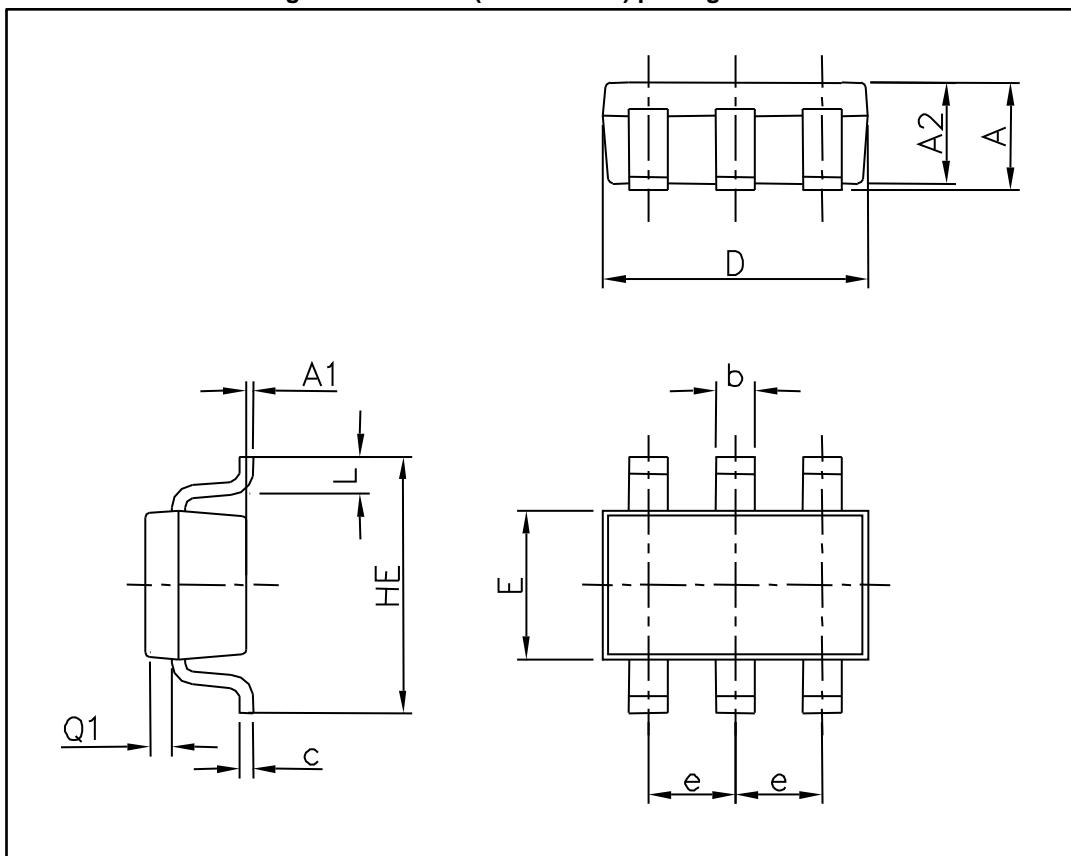


**Table 9: SC70-6 (or SOT323-6) mechanical data**

| Ref | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.80 | | 1.10 | 0.031 | | 0.043 |
| A1 | | | 0.10 | | | 0.004 |
| A2 | 0.80 | | 1.00 | 0.031 | | 0.039 |
| b | 0.15 | | 0.30 | 0.006 | | 0.012 |
| c | 0.10 | | 0.18 | 0.004 | | 0.007 |
| D | 1.80 | | 2.20 | 0.071 | | 0.086 |
| E | 1.15 | | 1.35 | 0.045 | | 0.053 |
| e | | 0.65 | | | 0.026 | |
| HE | 1.80 | | 2.40 | 0.071 | | 0.094 |
| L | 0.10 | | 0.40 | 0.004 | | 0.016 |
| Q1 | 0.10 | | 0.40 | 0.004 | | 0.016 |

**Figure 20: SC70-6 (or SOT323-6) recommended footprint**
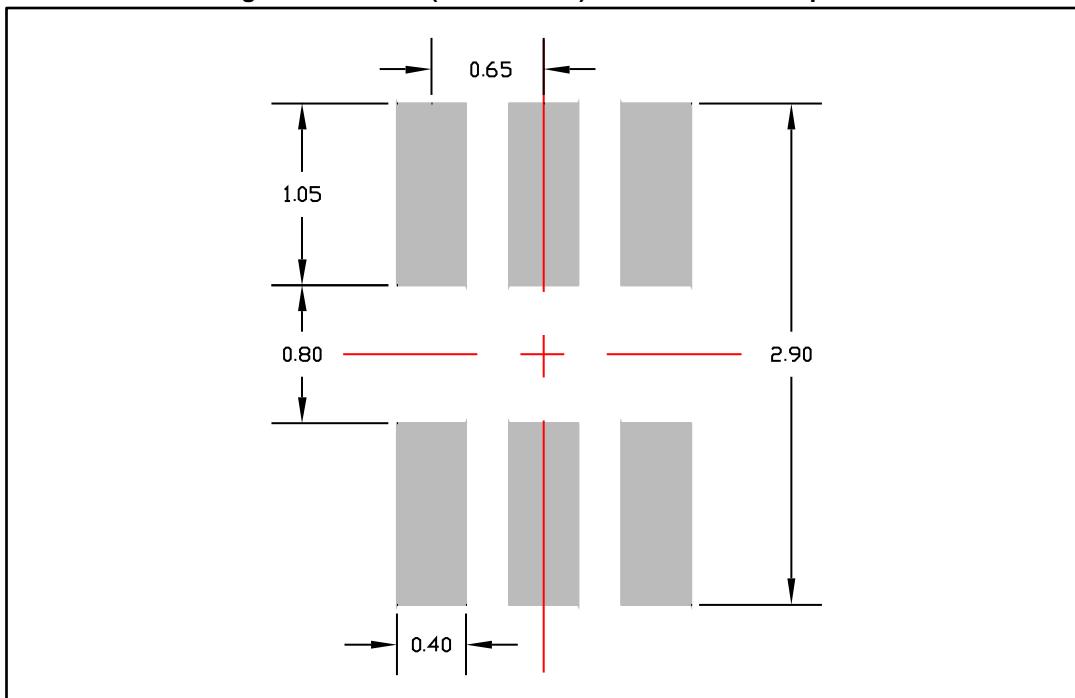
## 5.2 SOT23-6 package information

**Figure 21: SOT23-6 package outline**
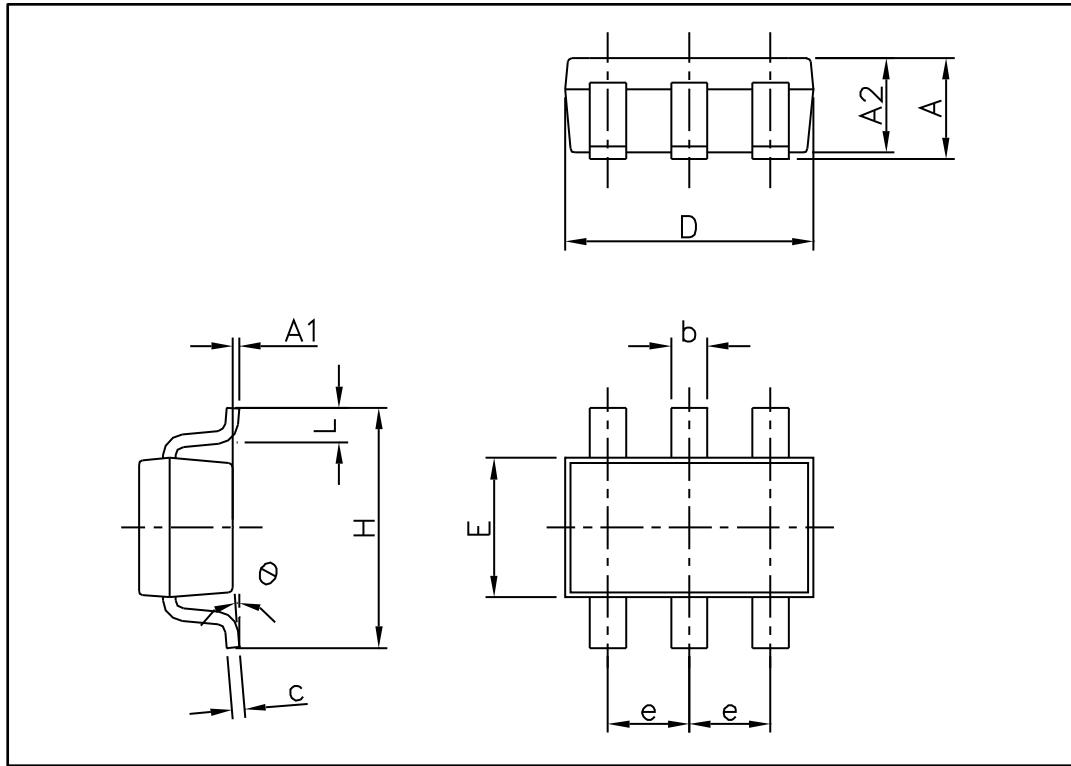


**Table 10: SOT23-6 mechanical data**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.90 | | 1.45 | 0.035 | | 0.057 |
| A1 | | | 0.10 | | | 0.004 |
| A2 | 0.90 | | 1.30 | 0.035 | | 0.051 |
| b | 0.35 | | 0.50 | 0.013 | | 0.019 |
| c | 0.09 | | 0.20 | 0.003 | | 0.008 |
| D | 2.80 | | 3.05 | 0.110 | | 0.120 |
| E | 1.50 | | 1.75 | 0.060 | | 0.069 |
| e | | 0.95 | | | 0.037 | |
| H | 2.60 | | 3.00 | 0.102 | | 0.118 |
| L | 0.10 | | 0.60 | 0.004 | | 0.024 |
| θ | 0 ° | | 10 ° | 0 ° | | 10 ° |

## 5.3 SC70-5 (or SOT323-5) package information

**Figure 22: SC70-5 (or SOT323-5) package outline**
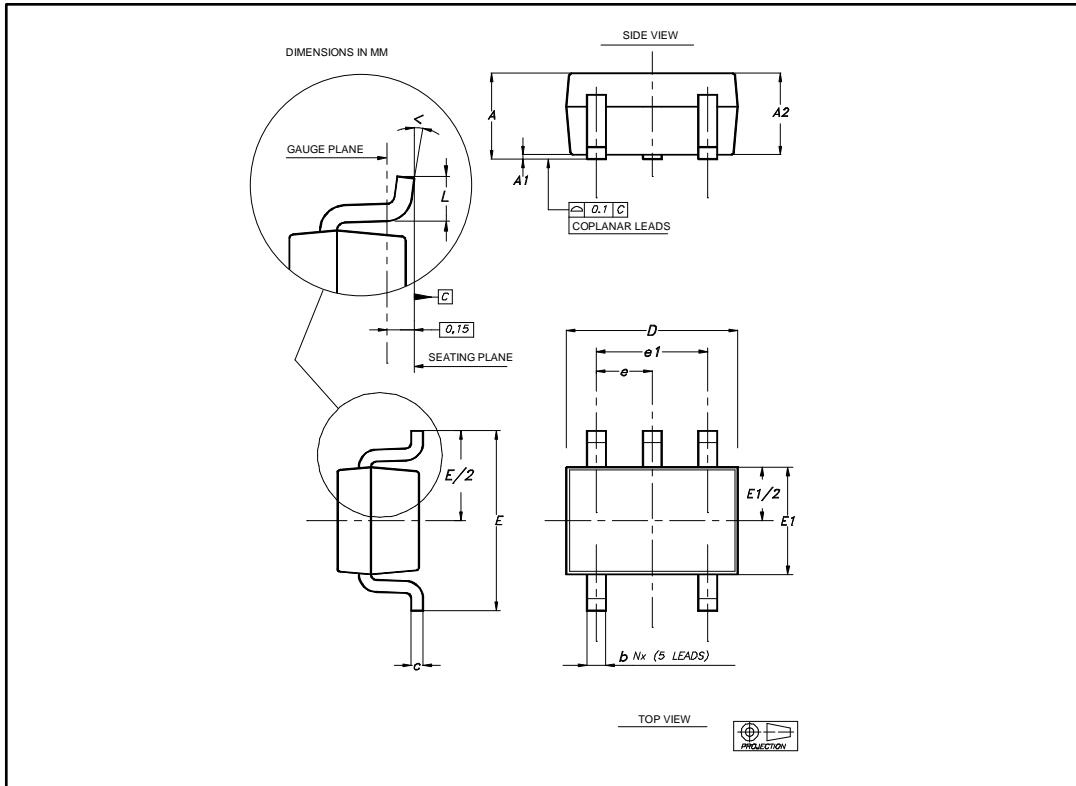


**Table 11: SC70-5 (or SOT323-5) mechanical data**

| Ref. | Dimensions | | | | | |
|------|-----------|-----|-----|-----|-----|-----|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.80 | | 1.10 | 0.315 | | 0.043 |
| A1 | | | 0.10 | | | 0.004 |
| A2 | 0.80 | 0.90 | 1.00 | 0.315 | 0.035 | 0.039 |
| b | 0.15 | | 0.30 | 0.006 | | 0.012 |
| c | 0.10 | | 0.22 | 0.004 | | 0.009 |
| D | 1.80 | 2.00 | 2.20 | 0.071 | 0.079 | 0.087 |
| E | 1.80 | 2.10 | 2.40 | 0.071 | 0.083 | 0.094 |
| E1 | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | | 0.65 | | | 0.025 | |
| e1 | | 1.30 | | | 0.051 | |
| L | 0.26 | 0.36 | 0.46 | 0.010 | 0.014 | 0.018 |
| < | 0° | | 8° | 0° | | 8° |

## 5.4 SOT23-5 package information

**Figure 23: SOT23-5 package outline**
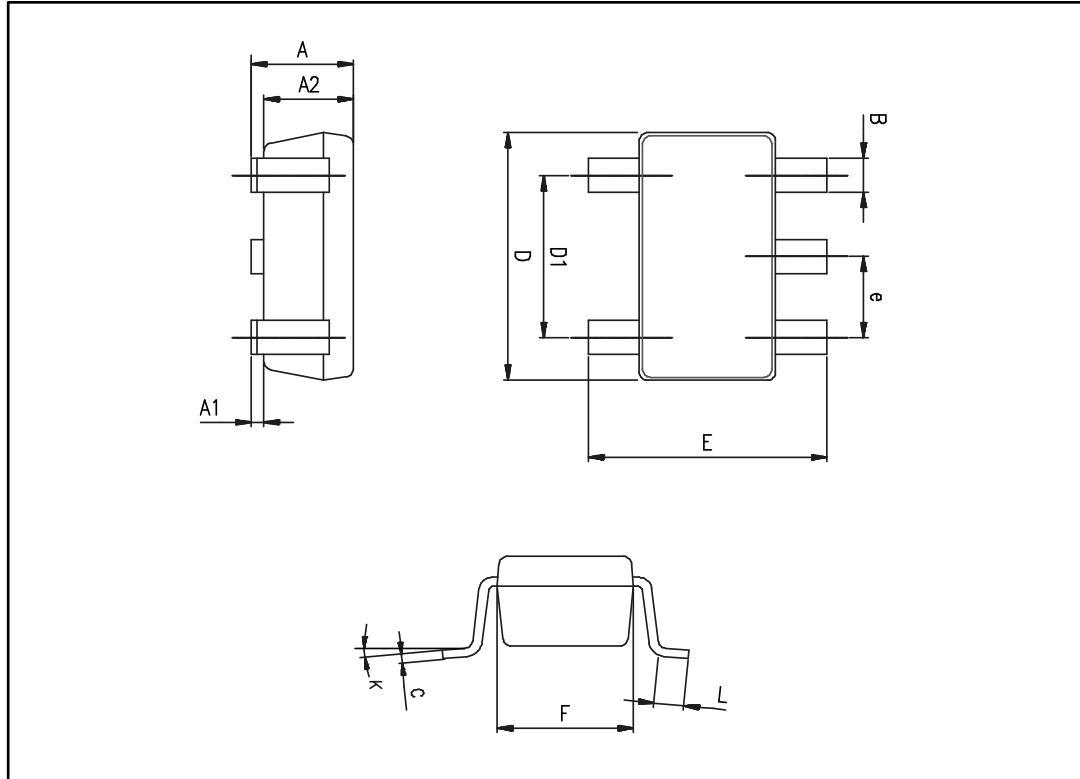


**Table 12: SOT23-5 mechanical data**

| Ref. | Dimensions | | | | | |
|------|------------|--|--|--|--|--|
|      | **Millimeters** | | | **Inches** | | |
|      | **Min.** | **Typ.** | **Max.** | **Min.** | **Typ.** | **Max.** |
| A    | 0.90 | 1.20 | 1.45 | 0.035 | 0.047 | 0.057 |
| A1   |      |      | 0.15 |       |       | 0.006 |
| A2   | 0.90 | 1.05 | 1.30 | 0.035 | 0.041 | 0.051 |
| B    | 0.35 | 0.40 | 0.50 | 0.014 | 0.016 | 0.020 |
| C    | 0.09 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D    | 2.80 | 2.90 | 3.00 | 0.110 | 0.114 | 0.118 |
| D1   |      | 1.90 |      |       | 0.075 |       |
| e    |      | 0.95 |      |       | 0.037 |       |
| E    | 2.60 | 2.80 | 3.00 | 0.102 | 0.110 | 0.118 |
| F    | 1.50 | 1.60 | 1.75 | 0.059 | 0.063 | 0.069 |
| L    | 0.10 | 0.35 | 0.60 | 0.004 | 0.014 | 0.024 |
| K    | 0 degrees |  | 10 degrees | 0 degrees |  | 10 degrees |

# 6 Ordering information

**Table 13: Order codes**

| Part number | Temperature range | Package | Packing | Marking |
|---|---|---|---|---|
| TSV6390ILT | -40 °C to 125 °C | SOT23-6 | Tape and reel | K109 |
| TSV6390ICT | | SC70-6 | | K19 |
| TSV6390AILT | | SOT23-6 | | K142 |
| TSV6390AICT | | SC70-6 | | K42 |
| TSV6391ILT | | SOT23-5 | | K108 |
| TSV6391ICT | | SC70-5 | | K20 |
| TSV6391AILT | | SOT23-5 | | K141 |
| TSV6391AICT | | SC70-5 | | K41 |

# 7     Revision history

**Table 14: Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 09-Mar-2010 | 1 | Initial release. |
| 04-Dec-2015 | 2 | Updated layout<br><br>*Section 2: "Electrical characteristics"*: replaced $DV_{io}$ by $\Delta V_{io}/\Delta T$ and updated $V_{OH}$ values. In *Table 7*, updated $t_{off}$ conditions.<br><br>*Electrical characteristic curves*: updated Y-axes of *Figure 7* and *Figure 8*.<br><br>*Shutdown function (TSV6390)*: updated X-axes of *Figure 17* and *Figure 18*.<br><br>*Table 10*: replaced ° with θ |

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