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**EVB-LAN88730
Evaluation Board
User's Guide**

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Object of Declaration: EVB-LAN88730 Evaluation Board

EU Declaration of Conformity

Manufacturer: Microchip Technology Inc.
2355 W. Chandler Blvd.
Chandler, Arizona, 85224-6199
USA

This declaration of conformity is issued by the manufacturer.

The development/evaluation tool is designed to be used for research and development in a laboratory environment. This development/evaluation tool is not intended to be a finished appliance, nor is it intended for incorporation into finished appliances that are made commercially available as single functional units to end users. This development/evaluation tool complies with EU EMC Directive 2004/108/EC and as supported by the European Commission's Guide for the EMC Directive 2004/108/EC (8th February 2010).

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This development/evaluation tool, when incorporating wireless and radio-telecom functionality, is in compliance with the essential requirement and other relevant provisions of the R&TTE Directive 1999/5/EC and the FCC rules as stated in the declaration of conformity provided in the module datasheet and the module product page available at www.microchip.com.

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Signed for and on behalf of Microchip Technology Inc. at Chandler, Arizona, USA


Derek Carlson
VP Development Tools

12-Sep-14
Date

EVB-LAN88730 User's Guide

NOTES:

Table of Contents

Preface	7
Introduction.....	7
Document Layout	7
Recommended Reading.....	8
The Microchip Web Site	8
Development Systems Customer Change Notification Service	8
Customer Support	9
Document Revision History	9
Chapter 1. Introduction	11
Chapter 2. Board Details	
2.1 Power	13
2.1.1 +5 V Power	13
2.1.2 VDDIO Power	13
2.1.3 +1.2 V Power	13
2.2 Configuration	14
2.2.1 MII/RMII Mode and Clocking Configuration (RMIISEL)	15
2.2.2 PHY Address Configuration	16
2.2.3 Mode Configuration	17
2.2.4 nINT/TXER/TXD4 Pin Configuration (nINTSEL)	18
2.2.5 Internal +1.2 V Regulator Configuration (REGOFF)	18
2.2.6 LEDs	19
2.2.7 Test Points	19
2.2.8 System Connections	19
2.2.9 Switches	21
2.3 Mechanicals	21
Appendix A. Evaluation Board	23
Appendix B. Schematics	25
Appendix C. Bill of Materials	29
Appendix D. Silk Screens	33
Worldwide Sales and Service	36

EVB-LAN88730 User's Guide

NOTES:

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXA”, where “XXXX” is the document number and “A” is the revision level of the document.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN88730 Evaluation Board. Topics discussed in this chapter include:

- [Document Layout](#)
- [Recommended Reading](#)
- [The Microchip Web Site](#)
- [Development Systems Customer Change Notification Service](#)
- [Customer Support](#)

DOCUMENT LAYOUT

This user's guide describes how to use the EVB-LAN88730 Evaluation Board. The document is organized as follows:

- [Chapter 1, Introduction](#) – This chapter provides an overview of the EVB-LAN88730 Evaluation Board and shows a simplified block diagram.
- [Chapter 2, Board Details](#) – This chapter describes the board details of the EVB-LAN88730 Evaluation Board including [Power](#), [Configuration](#) and [Mechanicals](#).
- [Appendix A, Evaluation Board](#) – This appendix shows the EVB-LAN88730 Evaluation Board.
- [Appendix B, Schematics](#) – This appendix shows the EVB-LAN88730 Evaluation Board schematics.
- [Appendix C, Bill of Materials](#) – This appendix includes the EVB-LAN88730 Evaluation Board Bill of Material (BOM).
- [Appendix D, Silk Screens](#) – This appendix includes the EVB-LAN88730 Evaluation Board silk screens.

EVB-LAN88730 User's Guide

RECOMMENDED READING

This user's guide describes how to use the EVB-LAN88730 Evaluation Board. Other useful documents are listed below.

- [1] LAN88730 Datasheet,
Microchip. www.microchip.com
- [2] AN8-13 Suggested Magnetics
Microchip. www.microchip.com

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- **Compilers** – The latest information on Microchip C compilers, assemblers, linkers and other language tools. These include all MPLAB C compilers; all MPLAB assemblers (including MPASM assembler); all MPLAB linkers (including MPLINK object linker); and all MPLAB librarians (including MPLIB object librarian).
- **Emulators** – The latest information on Microchip in-circuit emulators. This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICKit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PICKit 2 and 3.

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- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at: <http://support.microchip.com>.

DOCUMENT REVISION HISTORY

Revision A (February 2014)

- Replaces the previous SMSC version Rev. 1.0

Revision B (November 2015)

- Added 'Declaration of Conformity'
- Added [Appendix A, Evaluation Board](#)
- Added [Appendix B, Schematics](#)
- Added [Appendix C, Bill of Materials](#)
- Added [Appendix D, Silk Screens](#)

EVB-LAN88730 User's Guide

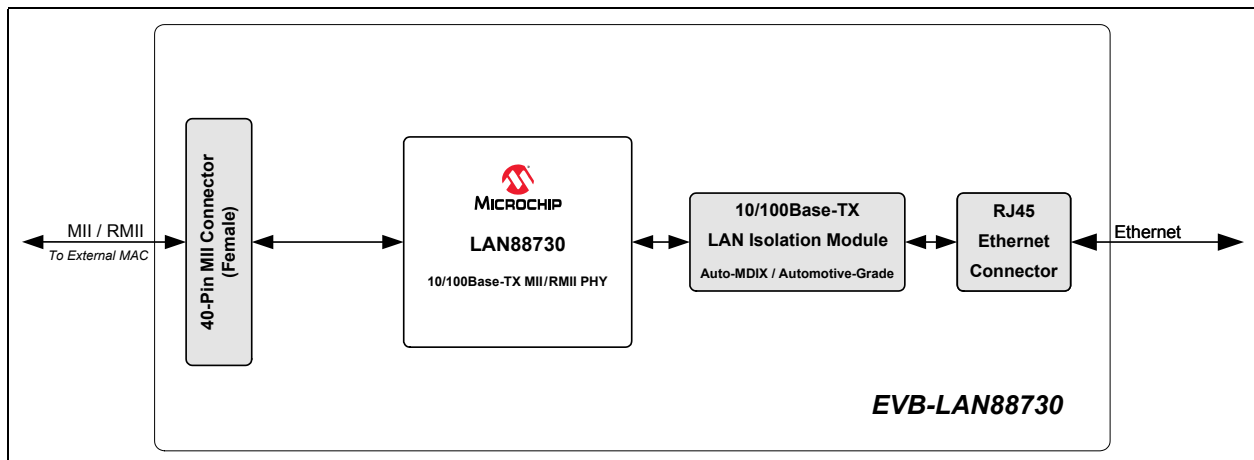
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Chapter 1. Introduction

The LAN88730 is a low-power, small form factor, highly integrated analog interface IC for high-performance embedded automotive Ethernet applications. The LAN88730 requires only a single +3.3 V supply and provides an integrated +1.2 V supply to run the core digital logic.

The EVB-LAN88730 is a PHY Evaluation Board (EVB) that interfaces a Media Independent Interface (MII) or Reduced Media Independent Interface (RMII™) MAC controller to the LAN88730 Ethernet MII/RMII PHY via a 40-pin MII/RMII connector. The LAN88730 is connected to automotive grade Ethernet magnetics and an RJ45 Ethernet jack for 10/100 connectivity. A simplified block diagram of the EVB-LAN88730 can be seen in [Figure 1-1](#).

FIGURE 1-1: EVB-LAN88730 BLOCK DIAGRAM



EVB-LAN88730 User's Guide

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Chapter 2. Board Details

2.1 POWER

2.1.1 +5 V Power

Power is normally supplied to the EVB-LAN88730's +3.3 V regulator externally via the +5 V power pins of the 40-pin connector. If desired, the EVB-LAN88730 can be powered without +5 V present on the 40-pin connector by supplying +5 V to the TP2 (red, see [Figure 2-1](#)) test point with ground connected to pin 20 of the J1 header.

Note: Before connecting an external power supply to TP2, ensure power is not present on the 40-pin connector's +5 V pins. Connecting +5 V simultaneously via the 40-pin connector and TP2 may result in permanent damage to the board.

2.1.2 VDDIO Power

The LAN88730's VDDIO power may be supplied at a voltage other than +3.3 V by depopulating resistor R12 and supplying +1.6 V to +3.6 V externally via test point TP5 (purple, see [Figure 2-1](#)), with ground connected to pin 20 of the J1 header.

Note: Before connecting an external power supply to TP5, ensure that resistor R12 has been removed. Connecting an external power supply to TP5 while resistor R12 is populated may result in permanent damage to the board.

2.1.3 +1.2 V Power

The LAN88730's internal +1.2 V regulator can be optionally disabled. Refer to [Section 2.2.5, "Internal +1.2 V Regulator Configuration \(REGOFF\)"](#) for additional information.

EVB-LAN88730 User's Guide

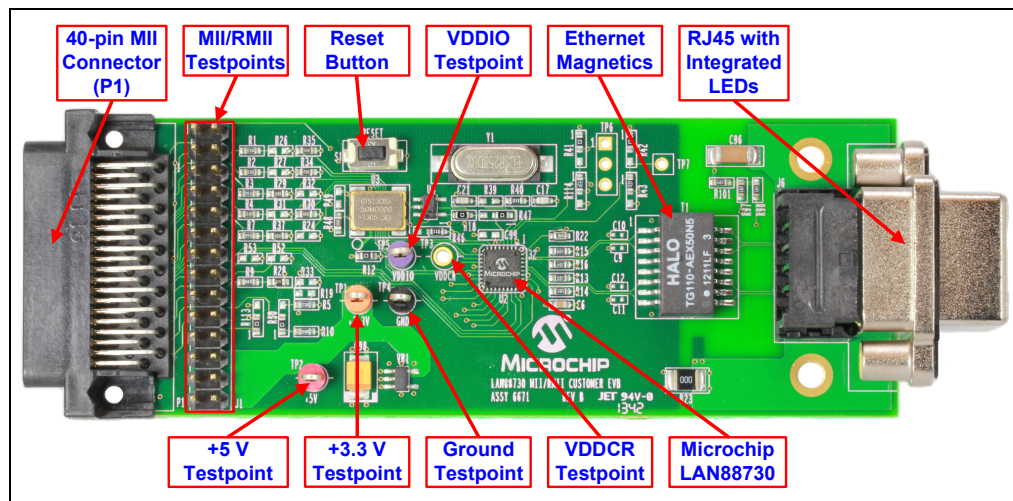
2.2 CONFIGURATION

The following sub-sections describe the various board features and configuration settings:

- MII/RMII Mode and Clocking Configuration (RMIISEL)
- PHY Address Configuration
- Mode Configuration
- nINT/TXER/TXD4 Pin Configuration (nINTSEL)
- Internal +1.2 V Regulator Configuration (REGOFF)
- LEDs
- Test Points
- System Connections
- Switches

A top view of the EVB-LAN88730 is shown in Figure 2-1.

FIGURE 2-1: TOP VIEW OF THE EVB88730

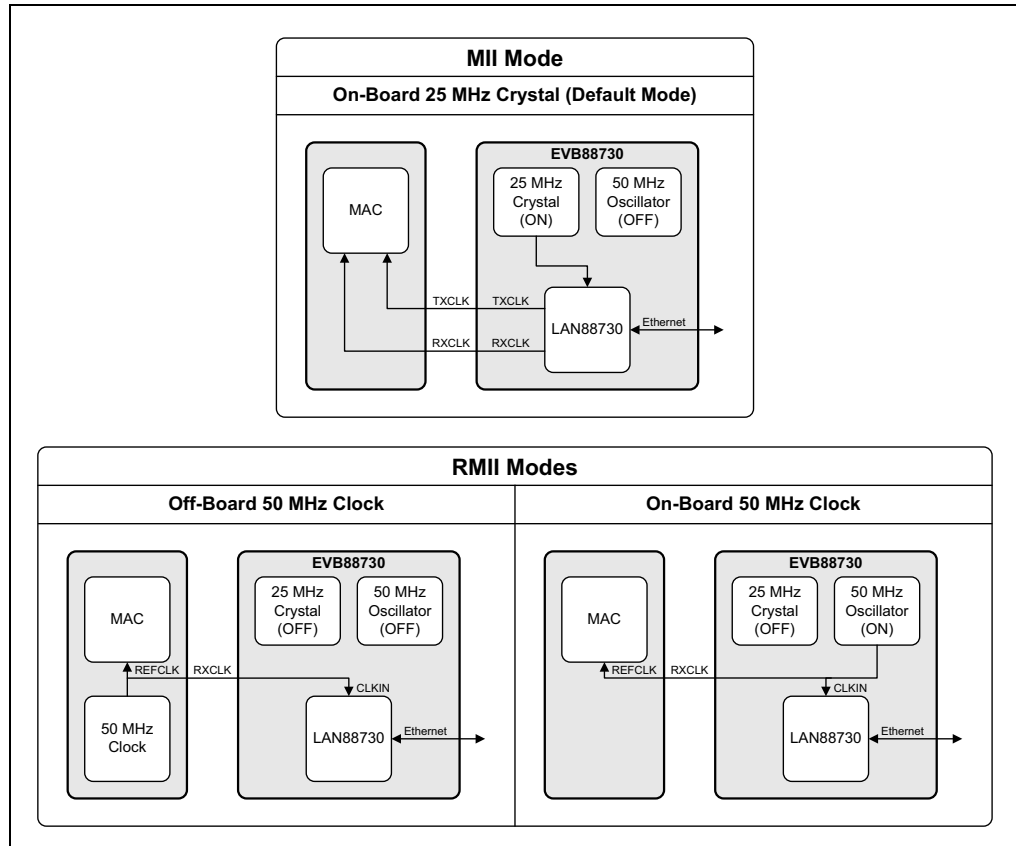


2.2.1 MII/RMII Mode and Clocking Configuration (RMIISEL)

The EVB-LAN88730 can operate in two functional modes: MII Mode or RMII Mode. The RMIISEL configuration strap is used to select one of these two modes. In MII Mode, the on-board 25 MHz crystal is used for clocking. In RMII Mode, the 50 MHz clock can be sourced by either the on-board 50 MHz oscillator or an off-board clock source.

Figure 2-2 summarizes the EVB-LAN88730 modes of operation. The EVB-LAN88730 must be properly configured for each mode as shown in Table 2-1. By default, the EVB-LAN88730 is configured to MII Mode. Refer to the LAN88730 Datasheet [1] for additional information on MII and RMII modes of operation.

FIGURE 2-2: EVB-LAN88730 MODES OF OPERATION



EVB-LAN88730 User's Guide

TABLE 2-1: MII/RMII MODE RESISTOR CONFIGURATION

Mode	Mode Configuration Resistors						
	R5, R9, R34, R40	R18	R19, R27, R52, R53	R46, R47	R48	R49	R50
MII Mode On-board 25 MHz Crystal (Default)	Populate	Populate	Depopulate	Populate 1-2 Depopulate 2-3	Populate	Depopulate	Populate 1-2 Depopulate 2-3
RMII Mode On-board 50 MHz Clock	Depopulate	Populate	Populate	Depopulate 1-2 Populate 2-3	Depopulate	Populate	Depopulate 1-2 Depopulate 2-3
RMII Mode Off-board 50 MHz Clock	Depopulate	Depopulate	Populate	Depopulate 1-2 Populate 2-3	Populate	Depopulate	Depopulate 1-2 Depopulate 2-3

2.2.2 PHY Address Configuration

The EVB-LAN88730 allows the user to configure the default PHY address at power-up via the PHYAD[2:0] configuration straps. [Table 2-2](#) details the proper configuration required for each PHY address value. By default, all EVB-LAN88730 PHY address straps are configured to a value of “0”.

TABLE 2-2: PHYAD[2:0] RESISTOR CONFIGURATION

PHYAD[2:0]	PHYAD[2:0] Pull-Up/Down Resistors					
	PHYAD2		PHYAD1		PHYAD0	
	R26	R35	R25	R36	R24	R37
000 (Default)	Depopulate	Populate	Depopulate	Populate	Depopulate	Populate
001	Depopulate	Populate	Depopulate	Populate	Populate	Depopulate
010	Depopulate	Populate	Populate	Depopulate	Depopulate	Populate
011	Depopulate	Populate	Populate	Depopulate	Populate	Depopulate
100	Populate	Depopulate	Depopulate	Populate	Depopulate	Populate
101	Populate	Depopulate	Depopulate	Populate	Populate	Depopulate
110	Populate	Depopulate	Populate	Depopulate	Depopulate	Populate
111	Populate	Depopulate	Populate	Depopulate	Populate	Depopulate

2.2.3 Mode Configuration

The EVB-LAN88730 can be configured into a specific mode of operation at power-up via the MODE[2:0] configuration straps. [Table 2-3](#) details the proper configuration required for each mode. By default, all EVB-LAN88730 MODE[2:0] straps are configured to a value of “1”.

Note: For additional details on each mode of operation, refer to the LAN88730 Datasheet [1].

TABLE 2-3: MODE[2:0] RESISTOR CONFIGURATION

MODE[2:0]	MODE[2:0] Pull-Up/Down Resistors					
	MODE2		MODE1		MODE0	
	R28	R33	R29	R32	R30	R31
000 10BASE-T Half Duplex Auto-neg disabled	<i>Depopulate</i>	Populate	<i>Depopulate</i>	Populate	<i>Depopulate</i>	Populate
001 10BASE-T Full Duplex Auto-neg disabled	<i>Depopulate</i>	Populate	<i>Depopulate</i>	Populate	Populate	<i>Depopulate</i>
010 100BASE-TX Half Duplex Auto-neg disabled	<i>Depopulate</i>	Populate	Populate	<i>Depopulate</i>	<i>Depopulate</i>	Populate
011 100BASE-TX Full Duplex Auto-neg disabled	<i>Depopulate</i>	Populate	Populate	<i>Depopulate</i>	Populate	<i>Depopulate</i>
100 100BASE-TX Half Duplex Auto-neg enabled	Populate	<i>Depopulate</i>	<i>Depopulate</i>	Populate	<i>Depopulate</i>	Populate
101 Repeater mode	Populate	<i>Depopulate</i>	<i>Depopulate</i>	Populate	Populate	<i>Depopulate</i>
110 Power Down mode	Populate	<i>Depopulate</i>	Populate	<i>Depopulate</i>	<i>Depopulate</i>	Populate
111 (Default) All capable. Auto-neg enabled	Populate	<i>Depopulate</i>	Populate	<i>Depopulate</i>	Populate	<i>Depopulate</i>

2.2.4 nINT/TXER/TXD4 Pin Configuration (nINTSEL)

The nINT, TXER and TXD4 functions share a common LAN88730 pin. This pin can operate in two functional modes: nINT (Interrupt) Mode and TXER/TXD4 Mode. The nINTSEL configuration strap is used to select one of these two modes. The EVB-LAN88730 must be properly configured for each mode as detailed in [Table 2-4](#).

TABLE 2-4: nINT/TXER/TXD4 MODE RESISTOR CONFIGURATION

Mode	Mode Configuration Resistors		
	R42	R43	R113
nINT Mode (Default)	Populate 1-2 <i>Depopulate 2-3</i>	Populate 1-2 <i>Depopulate 2-3</i>	Populate 1-2 <i>Depopulate 2-3</i>
TXER/TXD4 Mode	<i>Depopulate 1-2</i> Populate 2-3	<i>Depopulate 1-2</i> Populate 2-3	<i>Depopulate 1-2</i> Populate 2-3

Note: The nINTSEL configuration strap shares functionality with LED2. Therefore, LED2 may function active-high or active-low depending on the nINTSEL configuration. For additional information on the functionality of the nINT/TXER/TXD4 and LED2/nINTSEL pins, refer to the LAN88730 Datasheet [1] and EVB-LAN88730 [Schematics](#).

2.2.5 Internal +1.2 V Regulator Configuration (REGOFF)

The LAN88730 provides the ability to disable the internal +1.2 V regulator. When the regulator is disabled, an external +1.2 V must be supplied to the VDDCR pin (via TP3). Configuration of the internal regulator is controlled by the REGOFF configuration strap. The EVB-LAN88730 must be properly configured for each mode as follows:

Internal +1.2 V Regulator Enabled (Default Mode)

- Populate the 1-2 positions of R114 and R41 to pull-down the REGOFF strap (enable regulator).
- Depopulate the 2-3 positions of R114 and R41.

Internal +1.2 V Regulator Disabled

- Populate the 2-3 positions of R114 and R41 to pull-up the REGOFF strap (disable regulator).
- Depopulate the 1-2 positions of R114 and R41.

Note: The REGOFF configuration strap shares functionality with LED1. Therefore, LED1 may function active-high or active-low depending on the REGOFF configuration. For additional information on the LED1/REGOFF pin and the disabling of the internal 1.2 V regulator (power sequencing requirements, etc.), refer to the LAN88730 Datasheet [1] and EVB-LAN88730 [Schematics](#).

2.2.6 LEDs

TABLE 2-5: LEDS

Reference	Color	Indication
LED1	Green	Link/Activity Active when the PHY has established a valid link with a link partner and blinks when activity is detected.
LED2	Yellow	Speed Active when a 100BASE-TX link has been established. Inactive when a 10BASE-T link has been established or during line isolation.

Note: LED1 and LED2 are located inside the RJ45 connector. LED1 and LED2 may function active-high or active-low depending on the configuration of the REGOFF and nINTSEL straps, respectively. Refer to the LAN88730 Datasheet [1] and EVB-LAN88730 [Schematics](#) for additional information.

2.2.7 Test Points

TABLE 2-6: TEST POINTS

Test Point	Description	Connection
TP1	+3.3 V Test Point (Orange)	+3.3 V
TP2	+5.0 V Test Point (Red)	+5.0 V
TP3	+1.2 V VDDCR Test Point (Unpopulated) (Note 1)	+1.2 V
TP4	Ground Test Point (Black)	Ground
TP5	VDDIO Test Point (Purple)	+3.3 V (Note 2)

Note 1: VDDCR is the internal +1.2 V regulated output. When REGOFF is enabled, the internal 1.2 V regulator is disabled. In this case, an external 1.2 V regulator must be supplied to test point TP3.

Note 2: The LAN88730's VDDIO power may be supplied externally at a voltage other than +3.3 V as described in [Section 2.1, "Power"](#).

2.2.8 System Connections

TABLE 2-7: SYSTEM CONNECTIONS

PLUG/HEADER	DESCRIPTION	PART
J1	2x14 MII Header Note: Refer to Table 2-8 for a full pin list.	Adam Tech PH2-28-U-A
J6	RJ45 with Integrated LEDs	Amphenol MRJ-5381-01
P1	40-pin Female MII Connector Note: Refer to Table 2-9 for a full pin list.	Tyco 5173278-2

EVB-LAN88730 User's Guide

TABLE 2-8: J1 - 2x14 MII HEADER PINOUT

Header Pin	Description	Header Pin	Description
1	nRST	15	TXD1
2	MDIO (Note 3)	16	TXD2
3	MDC	17	TXD3
4	RXD3/ PHYAD2	18	CRS_DV/COL/ MODE2
5	RXD2/ RMIISEL	19	CRS/RXDV (Note 6)
6	RXD1/ MODE1	20	Ground
7	RXD0/ MODE0	21	nINT (Note 5)
8	RXDV	22	VDDIO
9	RXCLK (Note 4)	23	+3.3 V
10	RXER/RXD4/ PHYAD0	24	Ground
11	TXER/TXD4 (Note 5)	25	Ground
12	TXCLK	26	Ground
13	TXEN	27	Ground
14	TXD0	28	Ground

- Note 3:** Resistor R11 acts as a pull-up on the MDIO pin. In most situations, the MAC circuitry provides this pull-up and R11 is not required.
- Note 4:** In MII Mode, this pin connects to the RXCLK/[PHYAD1](#) pin of the LAN88730. In RMII Mode, this pin is used to route the 50 MHz clock source between the EVB-LAN88730 and the connected MAC. Refer to [Section 2.2.1, “MII/RMII Mode and Clocking Configuration \(RMIISEL\)”](#) and the EVB-LAN88730 [Schematics](#) for additional information.
- Note 5:** The nINT/TXER/TXD4 configuration determines the functionality of this pin. When in nINT (Interrupt) Mode, pin 21 of J1 is connected to pin 18 (nINT) of the LAN88730 and pin 11 of J1 is not connected. When in TXER/TXD4 Mode, pin 11 of J1 is connected to pin 18 (TXER/TXD4) of the LAN88730 and pin 21 of J1 is not connected. Refer to [Section 2.2.4, “nINT/TXER/TXD4 Pin Configuration \(nINT-SEL\)”](#) for additional information.
- Note 6:** The configuration of the R50 resistor determines the functionality of this pin. In MII Mode, this pin connects to the CRS pin of the LAN88730. In RMII Mode, this pin is not connected. Refer to [Section 2.2.1, “MII/RMII Mode and Clocking Configuration \(RMIISEL\)”](#) and the EVB-LAN88730 [Schematics](#) for additional information.

TABLE 2-9: P1 - 40-PIN FEMALE CONNECTOR PINOUT

Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	+5 V	11	TXER (Note 7)	21	+5 V	31	GND
2	MDIO (Note 3)	12	TXCLK	22	GND	32	GND
3	MDC	13	TXEN	23	GND	33	GND
4	RXD3	14	TXD0	24	GND	34	GND
5	RXD2	15	TXD1	25	GND	35	GND
6	RXD1	16	TXD2	26	GND	36	GND
7	RXD0	17	TXD3	27	GND	37	GND
8	RXDV	18	COL	28	GND	38	GND
9	RXCLK (Note 4)	19	CRS (Note 6)	29	GND	39	GND
10	RXER	20	+5 V	30	GND	40	+5 V

Note 7: The nINT/TXER/TXD4 configuration determines the functionality of this pin. When in nINT (Interrupt) Mode, this pin is not connected. When in TXER/TXD4 Mode, this pin is connected to pin 18 (TXER/TXD4) of the LAN88730. Refer to [Section 2.2.4, “nINT/TXER/TXD4 Pin Configuration \(nINTSEL\)”](#) for additional information.

2.2.9 Switches

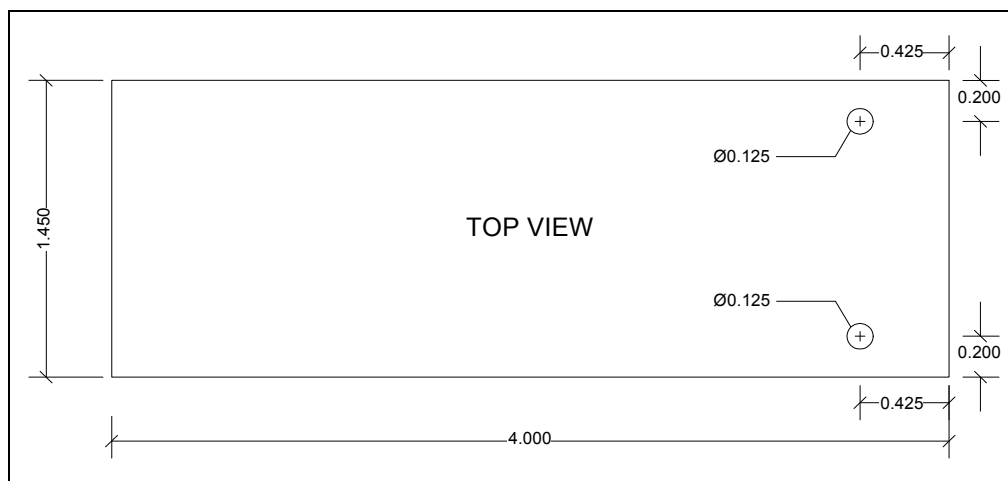
TABLE 2-10: SWITCHES

Switch	Description	Function
S1	Reset switch	When pressed, triggers a board reset.

2.3 MECHANICALS

[Figure 2-3](#) details the EVB-LAN88730 mechanical dimensions [inch].

FIGURE 2-3: EVB-LAN88730 MECHANICAL DIMENSIONS



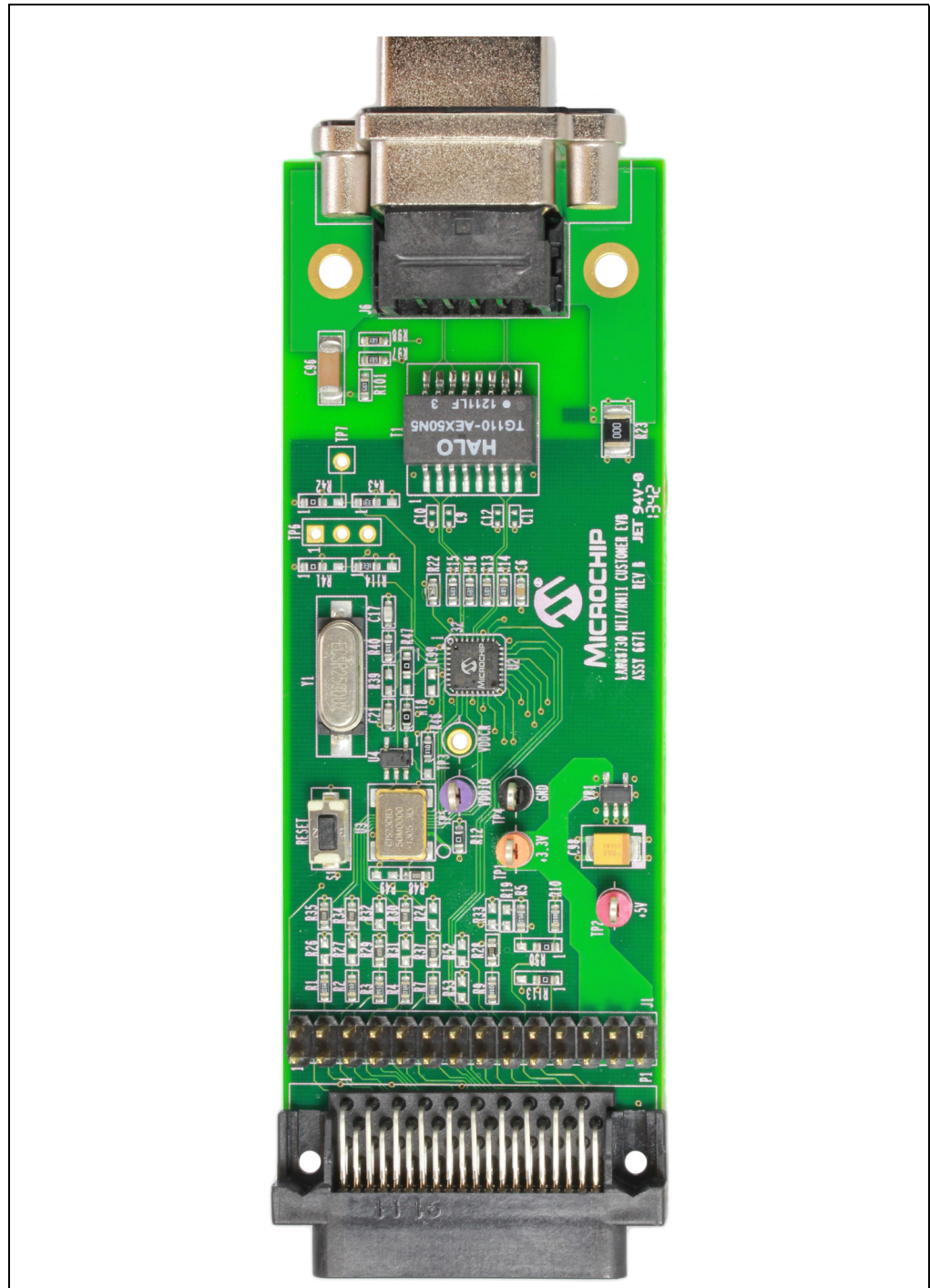
EVB-LAN88730 User's Guide

NOTES:

Appendix A. Evaluation Board

This appendix shows the EVB-LAN88730 Evaluation Board.

FIGURE A-1: EVB-LAN88730 EVALUATION BOARD



EVB-LAN88730 User's Guide

NOTES:

Appendix B. Schematics

This appendix shows the EVB-LAN88730 Evaluation Board schematics.

TABLE B-1: EVB-LAN88730 EVALUATION BOARD SCHEMATIC 1

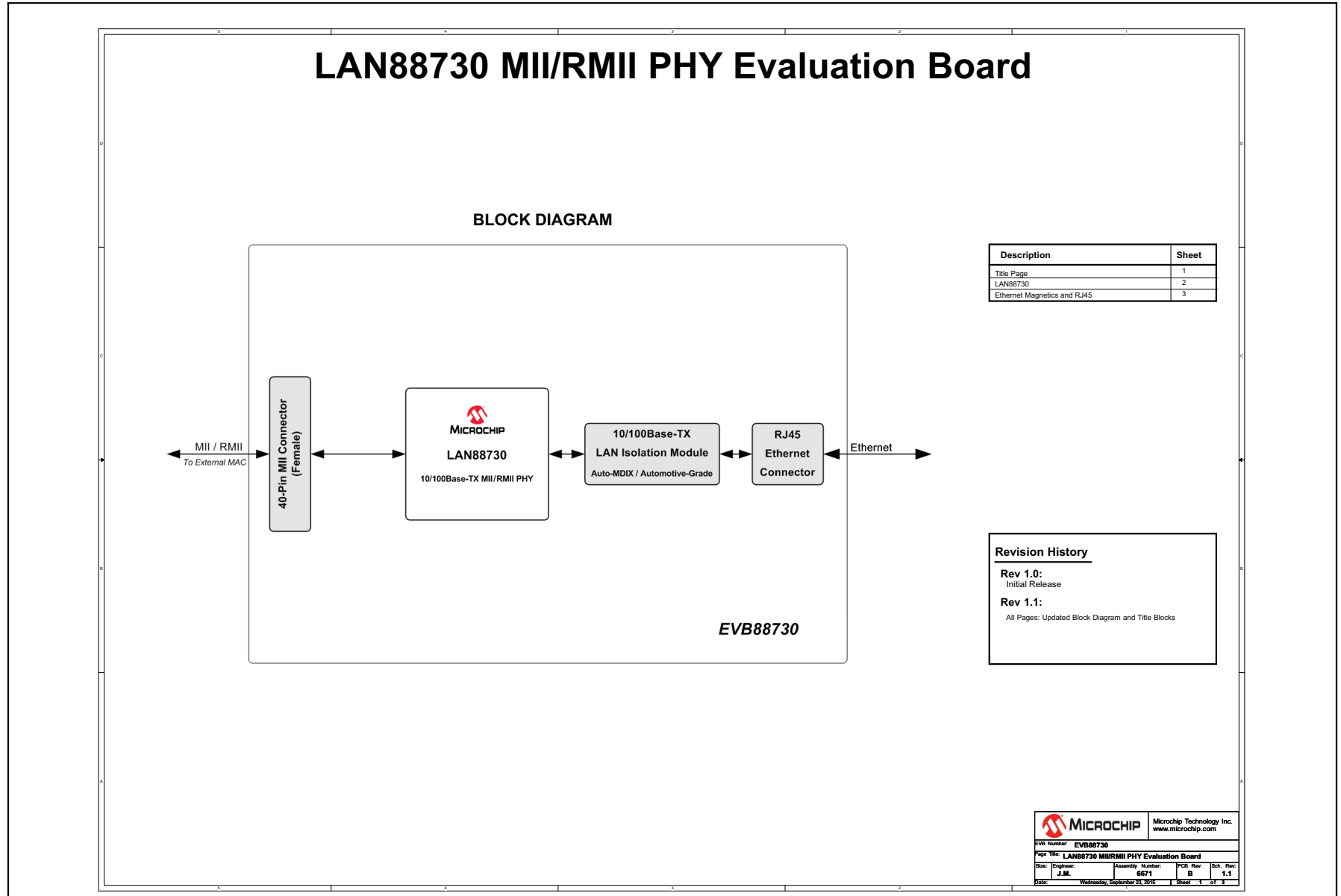
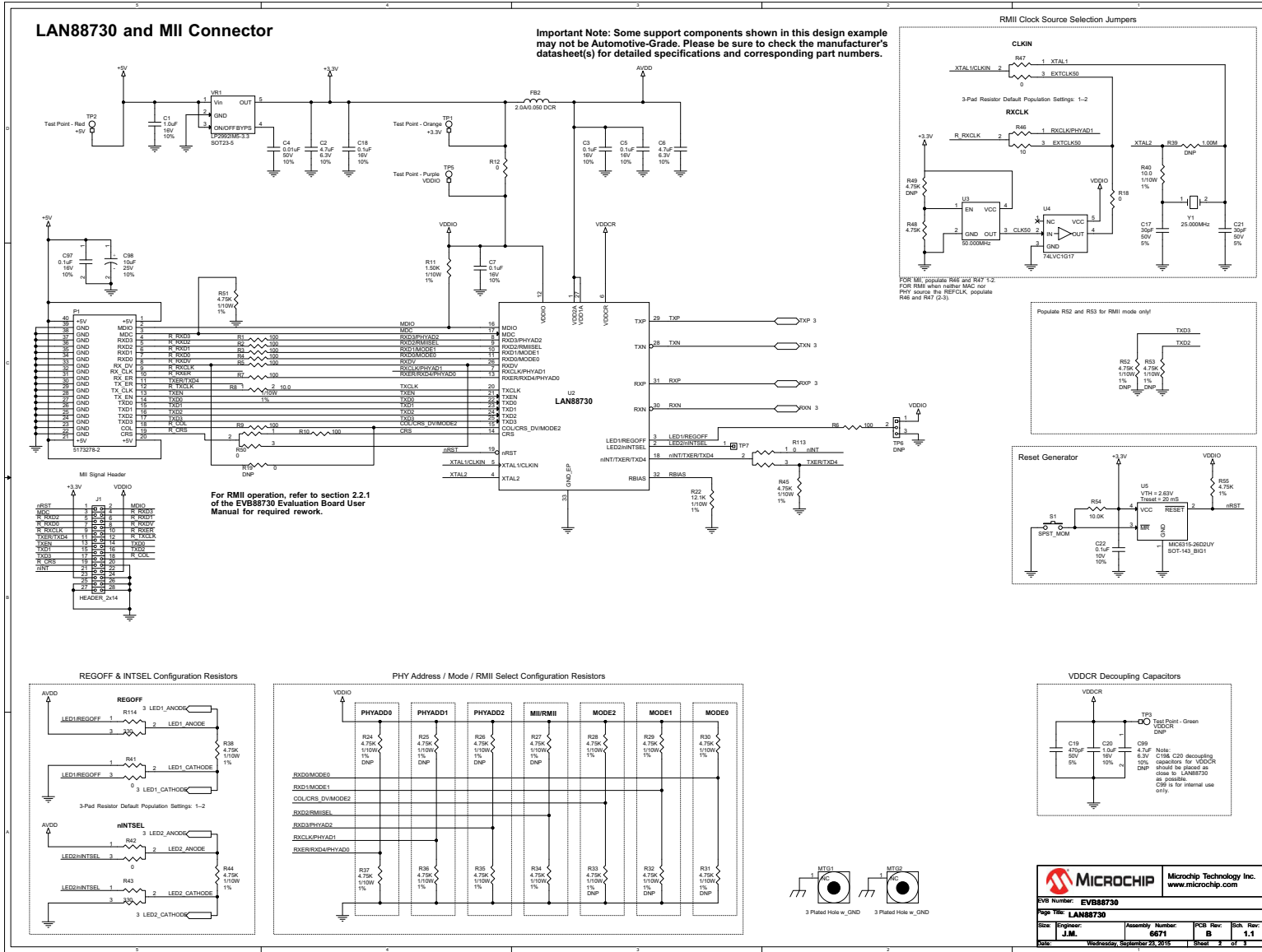
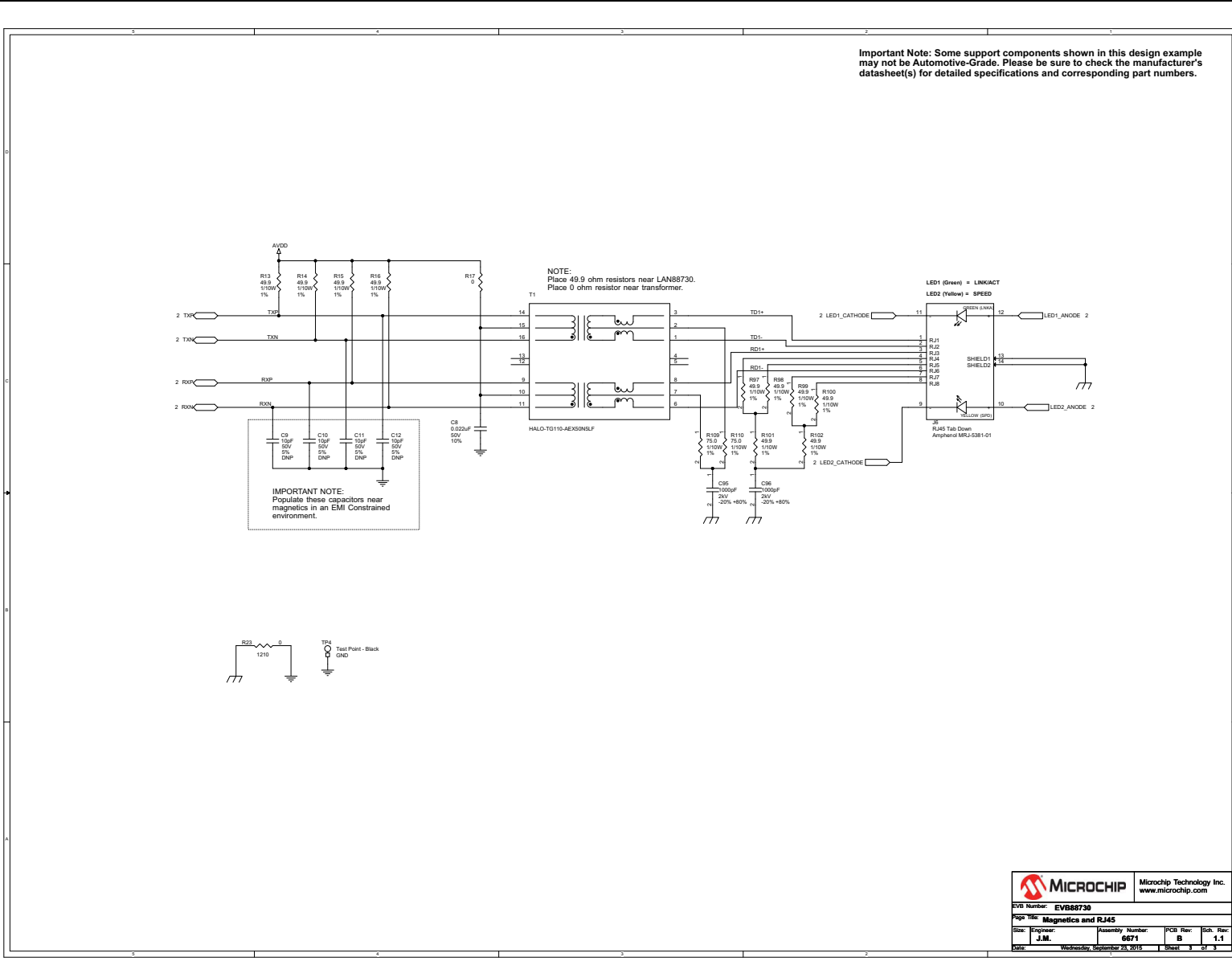


TABLE B-2: EVB-LAN88730 EVALUATION BOARD SCHEMATIC 2



MICROCHIP		Microchip Technology Inc.	
www.microchip.com			
Part Number: EVB88730 Part Name: LAN88730			
Size: J.M. Date:	Engineer: J.M. Wednesday, September 23, 2015	Assembly Number: 6671 PCB Rev: B	Rev: 1.1 Sheet 2 of 3

TABLE B-3: EVB-LAN88730 EVALUATION BOARD SCHEMATIC 3



		Microchip Technology Inc. www.microchip.com	
EVB Number: EVB88730			
Page No: Magnetics and RJ45			
Doc. Engineer:	Assembly Number:	PCB Rev:	Rev:
J.M.	6671	B	1.1
Date:	Wednesday, September 23, 2015	Sheet	3 of 3



Appendix C. Bill of Materials

This appendix shows the EVB-LAN88730 Evaluation Board Bill of Materials (BOM).

TABLE C-1: EVB-LAN88730 EVALUATION BOARD BILL OF MATERIALS

EVB88730

LAN88730 10/100 Ethernet MII / RMII PHY Evaluation Bd.

PCB ASSY 6671

REVISED: Sept. 23, 2015

PCB Revision: B

Schematic Revision: 1.1

Bill of Materials

Item	Qty	Reference	Part	PCB Footprint	Part #
1	2	C1,C20	1.0uF 16V	0603	Kemet C0603C105K4PACTU
2	2	C2,C6	4.7uF 6.3V	0603	Panasonic ECJ-1VB0J475K
3	5	C3,C5,C7,C18,C97	0.1uF 16V	0603	Kemet C0603C104K4RACTU
4	1	C4	0.01uF 50V	0603	Kemet C0603C103K5RACTU
5	1	C8	0.022uF 50V	0603	Kemet C0603C223K5RACTU
6	DNP 4	C9,C10,C11,C12	10pF 50V	0402	Kemet C0402C100J5GACTU
7	2	C17,C21	30pF 50V	0603	Kemet C0603C300J5GACTU
8	1	C19	470pF 50V	0603	Murata GCM1885C1H471JA16D
9	1	C22	0.1uF 10V	0603	Kemet C0603C104K8RAC
10	2	C95,C96	1000pF 2kV	1808	AVX 1808GC102ZAT1A
11	1	C98	10uF 25V	SMD_B	Kemet T491B106K025AT
12	DNP 1	C99	4.7uF 6.3V	0603	Panasonic ECJ-1VB0J475K
13	1	FB2	2.0A/0.050 DCR	0603	Murata BLM18PG121SN1D
14	1	J1	HEADER_2x14	HEAD2x14	Adam Tech PH2-28-U-A
15	1	J6	RJ45 Tab Down	RJ45LED-MRJ-5381	Amphenol MRJ-5381-01
16	2	MTG1,MTG2	3 Plated Hole w_GND	MTG_NUM3_GND	
17	1	P1	5173278-2	AMP_174218-2	Tyco 5173278-2
18	9	R1,R2,R3,R4,R5,R6,R7,R9, R10	100	0603	Rohm MCR03EZPFX1000
19	2	R8,R40	10	0603	Rohm MCR03EZPFX10R0
20	1	R11	1.50K	0603	Rohm MCR03EZPFX1501
21	3	R12,R17,R18	0	0603	Rohm MCR03EZPJ000
22	4	R13,R14,R15,R16	49.9	0603	Rohm MCR03EZPFX49R9
23	DNP 1	R19	0	0603	Rohm MCR03EZPJ000
24	1	R22	12.1K	0603	Rohm MCR03EZPFX1212
25	1	R23	0	1210	Vishay CRCW12100000Z0EA
26	DNP 10	R24,R25,R26,R27,R31,R32, R33,R49,R52,R53	4.75K	0603	Rohm MCR03EZPFX1002

TABLE C-1: EVB-LAN88730 EVALUATION BOARD BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Part	PCB Footprint	Part #
27	13	R28,R29,R30,R34,R35,R36, R37,R38,R44,R45,R48,R51, R55	4.75K	0603	Rohm MCR03EZPFX1002
28	DNP 1	R39	1.00M	0603	Rohm MCR03EZPFX1004
29	4	R41,R42,R50,R113	0	3PIN_0603	ROHM - MCR03EZPJ000
30	2	R43,R114	330	3PIN_0603	ROHM - MCR03EZPFX3300
31	1	R46	10	3PIN_0603	Rohm MCR03EZPFX10R0
32	1	R47	0	3PIN_0603	Rohm MCR03EZPJ000
33	1	R54	10.0K	0603	Rohm MCR03EZPFX1002
34	6	R97,R98,R99,R100,R101, R102	49.9	0603	Rohm-MCR03EZPFX49R9
35	2	R109,R110	75	0603	Rohm-MCR03EZPFX75R0
36	1	S1	SPST_MOM	SW_MOM_PB	Panasonic EVQ-PJU04K
37	1	TP1	Test Point - Orange +3.3V	TP_THRU_93x63P	Keystone 5008
38	1	TP2	Test Point - Red +5V	TP_THRU_93x63P	Keystone 5005
39	DNP 1	TP3	Test Point - Green PWR	TP_THRU_93x63P	Keystone 5121
40	1	TP4	Test Point - Black GND	TP_THRU_93x63P	Keystone 5006
41	1	TP5	Test Point - Purple VDDIO	TP_THRU_93x63P	Keystone 5124
42	DNP 1	TP6	1x3	Head1x3	Adam Tech PH1-03-U-A
43	1	TP7	Test Point-1x1	HEAD1X1	AdamTech - PH1-01-U-A
44	1	T1	HALO-TG110-AEX50N5LF	HALO_TG110_S050P2	HALO-TG110-AEX50N5LF
45	1	U2	LAN88730	QFN32_5X5MM_EP3P3MM	Microchip LAN88730
46	1	U3	50.000MHz	SMD_5mmx7mm_OSC	CTS Freq. CB3LV-3I-50M0000
47	1	U4	74LVC1G17	SOT23-5	TI SN74LVC1G17DBV
48	1	U5	MIC6315-26D2UY	SOT-143_BIG1	Micrel MIC6315-29D2UY
49	1	VR1	LP2992IM5-3.3	SOT23-5	National Semi. LP2992IM5-3.3/NOPB
50	1	Y1	25.000MHz	XTAL_11P4X4P8MM	ECS-250-20-5PXDU

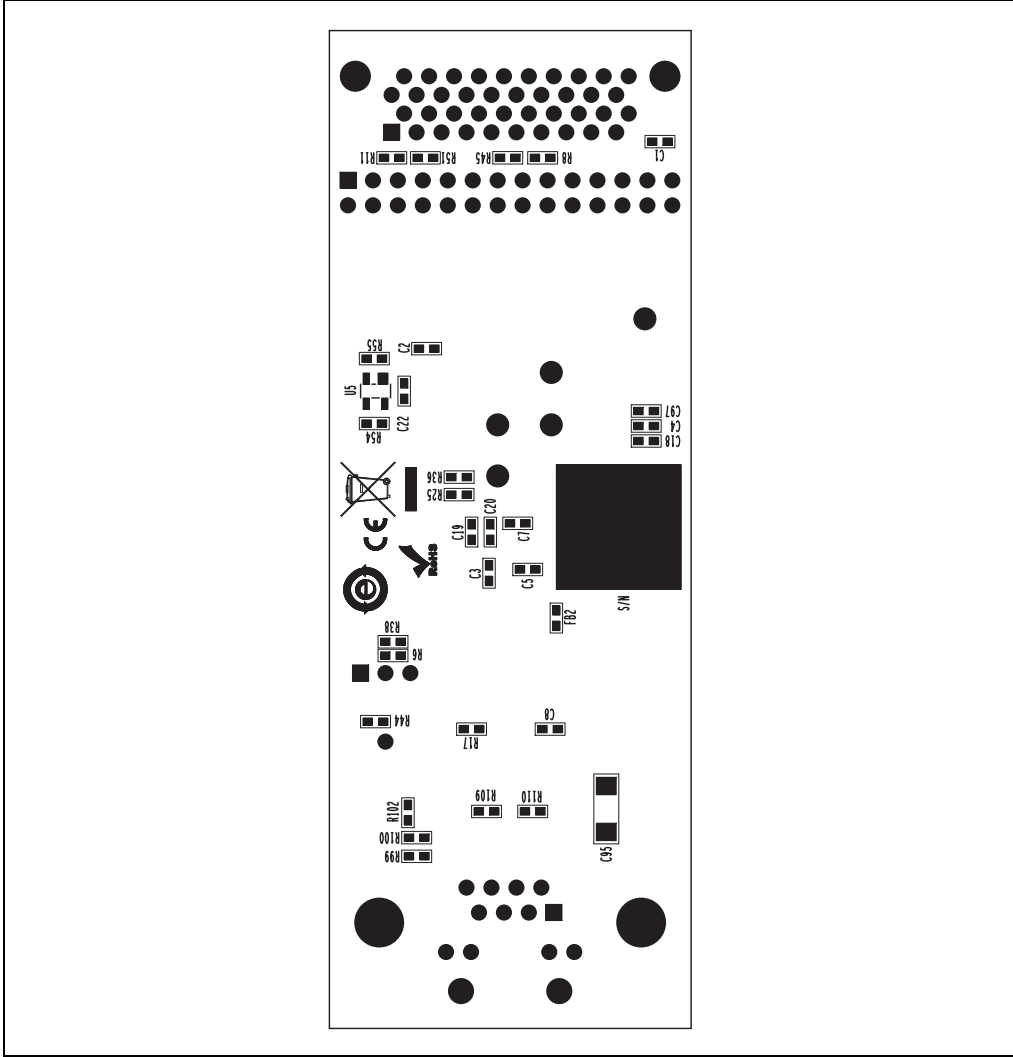
Note: Some support components shown in this design example may not be Automotive-Grade.
Please be sure to check the manufacturer's datasheet(s) for detailed specifications and corresponding part numbers.

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NOTES:

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FIGURE D-2: EVB-LAN88730 BOTTOM SILK SCREEN



NOTES:



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Corporate Office
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