



Triple High-Voltage Scan Driver for TFT LCD

MAX17120

General Description

The MAX17120 includes three high-voltage level-shifting scan drivers for TFT panel integrated gate logic. Each scan driver has two channels that switch complementarily. The scan-driver outputs swing from +40V to -30V and can swiftly drive capacitive loads. To save power, the scan-driver's complementary outputs share the charge of their capacitive load before they change states.

The MAX17120 is available in a 32-pin, 5mm x 5mm thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panels.

Applications

- Notebook Computer Displays
- LCD Monitor and Small TV Panels

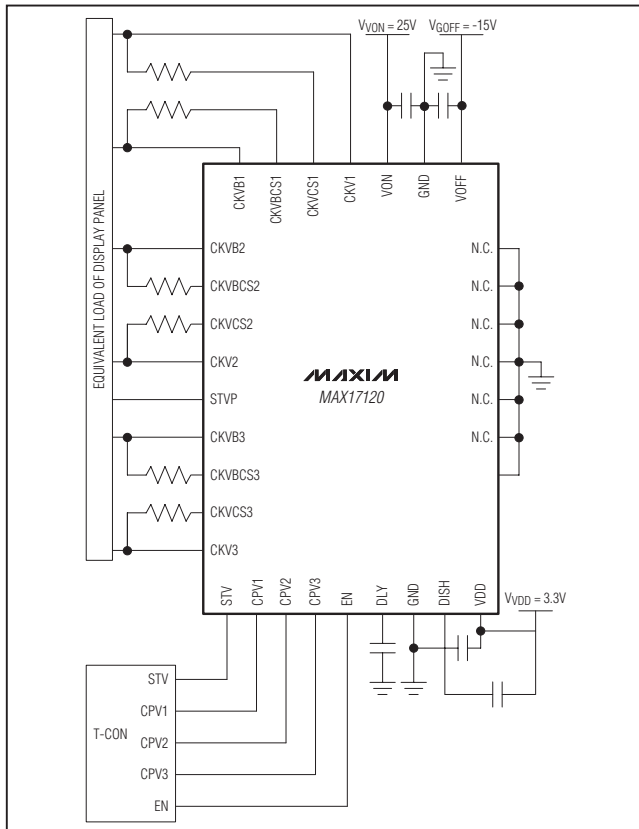
Features

- ◆ +40V to -30V Output Swing Range
- ◆ Fast Slew Rate for High Capacitive Load
- ◆ Load Charge Sharing for Power Saving
- ◆ 32-Pin, 5mm x 5mm Thin QFN Package

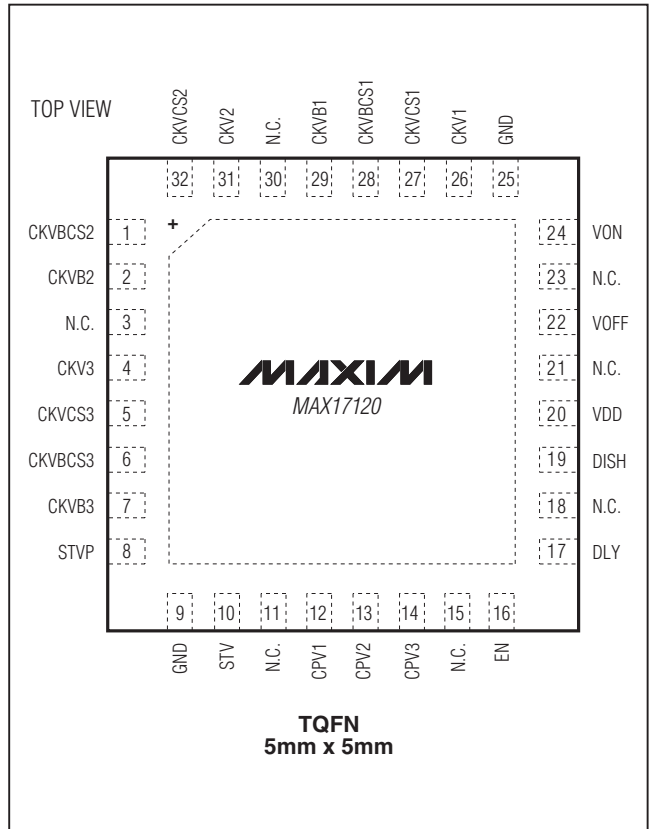
Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|--------------|----------------|-------------|
| MAX17120ETJ+ | -40°C to +85°C | 32 TQFN |

Simplified Operating Circuit



Pin Configuration



Triple High-Voltage Scan Driver for TFT LCD

ABSOLUTE MAXIMUM RATINGS

| | | | |
|---------------------------------------|------------------------------------|---|------------------------------------|
| VDD to GND | -0.3V to +4V | CKVCS1, CKVCS2, CKVCS3 to VOFF ... | -0.3V to (V _{VON} + 0.3V) |
| CPV1, CPV2, CPV3, STV, EN to GND..... | -0.3V to +4V | CKVBCS1, CKVBCS2, | |
| DLY to GND..... | -0.3V to (V _{VDD} + 0.3V) | CKVBCS3 to VOFF..... | -0.3V to (V _{VON} + 0.3V) |
| DISH to GND..... | -6V to (V _{VDD} + 0.3V) | Continuous Power Dissipation (T _A = +70°C) | |
| VON to GND..... | -0.3V to +45V | 32-Pin 5mm x 5mm Thin QFN | |
| VOFF to GND | -35V to +0.3V | (derate 34.5mW/°C above +70°C) | 2758.6mW |
| VON to VOFF..... | +65V | Operating Temperature Range | -40°C to +85°C |
| CKV1, CKV2, CKV3, CKVB1, CKVB2, | | Junction Temperature | +150°C |
| CKVB3 to VOFF | -0.3V to (V _{VON} + 0.3V) | Storage Temperature Range..... | -65°C to +150°C |
| STVP to VOFF..... | -0.3V to (V _{VON} + 0.3V) | Lead Temperature (soldering, 10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{VDD} = V_{EN} = +3.3V, V_{VON} = 25V, V_{VOFF} = -15V, STV = CPV1 = CPV2 = CPV3 = GND, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|--|-----|-----|------|-------|
| VDD Input-Voltage Range | | 2.2 | | 3.6 | V |
| VDD UV Lockout | Rising, hysteresis = 150mV | | 2 | 2.15 | V |
| VDD Quiescent Current | V _{EN} = 3.3V | | 500 | 750 | μA |
| | EN = GND | | 500 | 750 | |
| Thermal Shutdown | Rising edge, hysteresis = 15°C | | 160 | | °C |
| VON Input-Voltage Range | | 15 | | 40 | V |
| VON Supply Current | V _{EN} = 3.3V | | 300 | 600 | μA |
| | EN = GND | | 300 | 600 | |
| VOFF Input-Voltage Range | | -30 | | -3 | V |
| VOFF Supply Current | V _{EN} = 3.3V | | 200 | 350 | μA |
| | EN = GND | | 200 | 350 | |
| VON-to-VOFF Voltage Range | | | | 65 | V |
| VON UV Lockout | VON rising | | 12 | 13 | V |
| | VON falling | 10 | 11 | | |
| CKV_, CKVB_ Output Low | I(CKV_) = -20mA | | 5 | 10 | Ω |
| CKV_, CKVB_ Output High | I(CKV_) = 20mA | | 9 | 18 | Ω |
| CPV_ Rising to CKV_ Rising | t _R , Figure 4, V _{STV} = 0V | | 100 | 150 | ns |
| CPV_ Rising to CKV_ Falling | t _F , Figure 4, V _{STV} = 0V | | 100 | 150 | ns |
| CPV_ Rising to CKVB_ Rising | t _R , Figure 4, V _{STV} = 0V | | 100 | 150 | ns |
| CPV_ Rising to CKVB_ Falling | t _F , Figure 4, V _{STV} = 0V | | 100 | 150 | ns |
| CPV_ Falling to CKVCS_ Rising | t _{CSR} , Figure 4, V _{STV} = 0V | | 130 | 180 | ns |
| CPV_ Falling to CKVCS_ Falling | t _{CSF} , Figure 4, V _{STV} = 0V | | 130 | 180 | ns |
| CPV_ Falling to CKVCBS_ Rising | t _{CSR} , Figure 4, V _{STV} = 0V | | 130 | 180 | ns |
| CPV_ Falling to CKVBCS_ Falling | t _{CSF} , Figure 4, V _{STV} = 0V | | 130 | 180 | ns |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = V_{EN} = +3.3V$, $V_{ON} = 25V$, $V_{OFF} = -15V$, $STV = CPV1 = CPV2 = CPV3 = GND$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|---|------|------|------|------------|
| CKV_, CKVB_ Slew Rate Rising | STV = GND, $C_{LOAD} = 15nF$, $R_{LOAD} = 100\Omega$, 15% to 85% (Note 1) | 100 | 1000 | | V/ μs |
| | STV = GND, $C_{LOAD} = 4.7nF$, 20% to 80% | 100 | 160 | | |
| CKV_, CKVB_ Slew Rate Falling | STV = GND, $C_{LOAD} = 15nF$, $R_{LOAD} = 100\Omega$, 85% to 15% (Note 1) | 100 | 1000 | | V/ μs |
| | STV = GND, $C_{LOAD} = 4.7nF$, 80% to 20% | 100 | 160 | | |
| CKV_, CKVB_ Slew Rate Rising | STV = VDD, $C_{LOAD} = 15nF$, $R_{LOAD} = 100\Omega$, 15% to 85% (Note 1) | 100 | 1000 | | V/ μs |
| | STV = VDD, $C_{LOAD} = 4.7nF$, 20% to 80% | 100 | 160 | | |
| CKV_, CKVB_ Slew Rate Falling | STV = VDD, $C_{LOAD} = 15nF$, $R_{LOAD} = 100\Omega$, 85% to 15% (Note 1) | 100 | 1000 | | V/ μs |
| | STV = VDD, $C_{LOAD} = 4.7nF$, 80% to 20% | 100 | 160 | | |
| Three-State Output Current | CKV = midsupply | -1 | | +1 | μA |
| CKVCS-to-CKVBCS_ Resistance | $I(CKVCS \text{ to } CKVCSB) = 10mA$ | | 40 | 100 | Ω |
| STVP Output Low | $I(STVP) = -20mA$ | | 17 | 35 | Ω |
| STVP Output High | $I(STVP) = 20mA$ | | 40 | 70 | Ω |
| STV Rising to STVP Rising | t_{PR} | | 120 | 200 | ns |
| STV Falling to STVP Falling | t_{PF} | | 120 | 200 | ns |
| STVP Slew Rate Rising | $C_{LOAD} = 4.7nF$ | 20 | 30 | | V/ μs |
| STVP Slew Rate Falling | $C_{LOAD} = 4.7nF$ | 20 | 30 | | V/ μs |
| CPV_ Input Frequency | | | | 85 | kHz |
| Input Low Voltage | CPV_, STV, EN, $2.2V < V_{DD} < 3.6V$ | | | 0.8 | V |
| Input High Voltage | CPV_, STV, EN, $2.2V < V_{DD} < 3.6V$ | 2 | | | V |
| Input Hysteresis | CPV_, STV, EN | | 250 | | mV |
| Input Bias Current | $V_{STV_} = 0V$ or V_{DD} ; $V_{CPV_} = 0V$ or V_{DD} | -1 | | +1 | μA |
| DISH Low Voltage | | | | -1.5 | V |
| DISH High Voltage | | -0.5 | | | V |
| DISH Input Impedance | $V_{DISH} = -2V$ | | 300 | 600 | k Ω |
| DISH Switch Resistance | $V_{DISH} = -2V$ | | 200 | 500 | Ω |
| | $V_{DISH} = 0V$ | | 1 | | M Ω |
| DLY Output Current | DLY = GND | 3 | 4 | 5 | μA |
| DLY Sink Current | EN = GND, $V_{DLY} = 0.4V$ | 5 | 8 | | mA |
| DLY Enable Threshold | Rising | 1.60 | 1.65 | 1.70 | V |
| Startup Delay | $C(DLY) = 0.1\mu F$ | | 40 | | ms |

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ELECTRICAL CHARACTERISTICS

($V_{DD} = V_{EN} = +3.3V$, $V_{VON} = 25V$, $V_{VOFF} = -15V$, $STV = CPV1 = CPV2 = CPV3 = GND$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.) (Note 2)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|--|-----|-----|------|------------|
| VDD Input-Voltage Range | | 2.2 | | 3.6 | V |
| VDD UV Lockout | Rising, hysteresis = 150mV | | | 2.15 | V |
| VDD Quiescent Current | $V_{EN} = 3.3V$ | | | 750 | μA |
| | $EN = GND$ | | | 750 | |
| VON Input-Voltage Range | | 15 | | 40 | V |
| VON Supply Current | $V_{EN} = 3.3V$ | | | 600 | μA |
| | $EN = GND$ | | | 600 | |
| VOFF Input-Voltage Range | | -30 | | -3 | V |
| VOFF Supply Current | $V_{EN} = 3.3V$ | | | 350 | μA |
| | $EN = GND$ | | | 350 | |
| VON-to-VOFF Voltage Range | | | | 65 | V |
| VON UV Lockout | VON rising | | | 13 | V |
| | VON falling | 10 | | | |
| CKV_, CKVB_ Output Low | $I(CKV_) = -20mA$ | | | 10 | Ω |
| CKV_, CKVB_ Output High | $I(CKV_) = 20mA$ | | | 18 | Ω |
| CPV_ Rising to CKV_ Rising | t_R , Figure 4, $V_{STV} = 0V$ | | | 150 | ns |
| CPV_ Rising to CKV_ Falling | t_F , Figure 4, $V_{STV} = 0V$ | | | 150 | ns |
| CPV_ Rising to CKVB_ Rising | t_R , Figure 4, $V_{STV} = 0V$ | | | 150 | ns |
| CPV_ Rising to CKVB_ Falling | t_F , Figure 4, $V_{STV} = 0V$ | | | 150 | ns |
| CPV_ Falling to CKVCS_ Rising | t_{CSR} , Figure 4, $V_{STV} = 0V$ | | | 180 | ns |
| CPV_ Falling to CKVCS_ Falling | t_{CSF} , Figure 4, $V_{STV} = 0V$ | | | 180 | ns |
| CPV_ Falling to CKVCBS_ Rising | t_{CSR} , Figure 4, $V_{STV} = 0V$ | | | 180 | ns |
| CPV_ Falling to CKVBCS_ Falling | t_{CSF} , Figure 4, $V_{STV} = 0V$ | | | 180 | ns |
| CKV_, CKVB_ Slew Rate Rising | $STV = GND$, $C_{LOAD} = 15nF$, $R_{LOAD} = 100\Omega$, 15% to 85% (Note 2) | 100 | | | V/ μs |
| | $STV = GND$, $C_{LOAD} = 4.7nF$, 20% to 80% | 100 | | | |
| CKV_, CKVB_ Slew Rate Falling | $STV = GND$, $C_{LOAD} = 15nF$, $R_{LOAD} = 100\Omega$, 85% to 15% (Note 2) | 100 | | | V/ μs |
| | $STV = GND$, $C_{LOAD} = 4.7nF$, 80% to 20% | 100 | | | |
| CKV_, CKVB_ Slew Rate Rising | $STV = VDD$, $C_{LOAD} = 15nF$, $R_{LOAD} = 100\Omega$, 15% to 85% (Note 2) | 100 | | | V/ μs |
| | $STV = VDD$, $C_{LOAD} = 4.7nF$, 20% to 80% | 100 | | | |

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ELECTRICAL CHARACTERISTICS (continued)

(V_{VDD} = V_{EN} = +3.3V, V_{VON} = 25V, V_{VOFF} = -15V, STV = CPV1 = CPV2 = CPV3 = GND, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--|------|-----|------|-------|
| CKV_ ₋ , CKVB_ ₋ Slew Rate Falling | STV = VDD, C _{LOAD} = 15nF, R _{LOAD} = 100Ω, 85% to 15% (Note 2) | 100 | | | V/μs |
| | STV = VDD, C _{LOAD} = 4.7nF, 80% to 20% | 100 | | | |
| CKVCS-to-CKVBCS_ ₋ Resistance | I(CKVCS to CKVCSB_ ₋) = 10mA | | | 100 | Ω |
| STVP Output Low | I(STVP) = -20mA | | | 35 | Ω |
| STVP Output High | I(STVP) = 20mA | | | 70 | Ω |
| STV Rising to STVP Rising | t _{PR} | | | 200 | ns |
| STV Falling to STVP Falling | t _{PF} | | | 200 | ns |
| STVP Slew Rate Rising | C _{LOAD} = 4.7nF | 20 | | | V/μs |
| STVP Slew Rate Falling | C _{LOAD} = 4.7nF | 20 | | | V/μs |
| CPV_ ₋ Input Frequency | | | | 85 | kHz |
| Input Low Voltage | CPV_ ₋ , STV, EN, 2.2V < V _{VDD} < 3.6V | | | 0.8 | V |
| Input High Voltage | CPV_ ₋ , STV, EN, 2.2V < V _{VDD} < 3.6V | 2 | | | V |
| DISH Low Voltage | | | | -1.5 | V |
| DISH High Voltage | | -0.5 | | | V |
| DISH Input Impedance | V _{DISH} = -2V | | | 600 | kΩ |
| DISH Switch Resistance | V _{DISH} = -2V | | | 500 | Ω |
| DLY Output Current | DLY = GND | 3 | | 5 | μA |
| DLY Sink Current | EN = GND, V _{DLY} = 0.4V | 5 | | | mA |
| DLY Enable Threshold | Rising | 1.60 | | 1.70 | V |

Note 1: Guaranteed by design, not production tested.

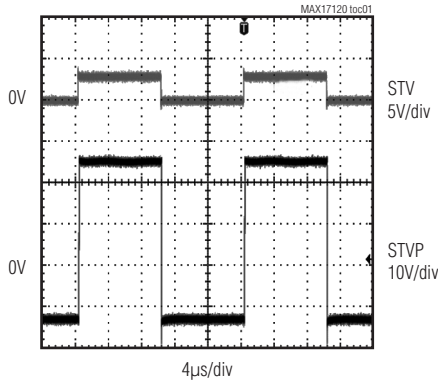
Note 2: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.

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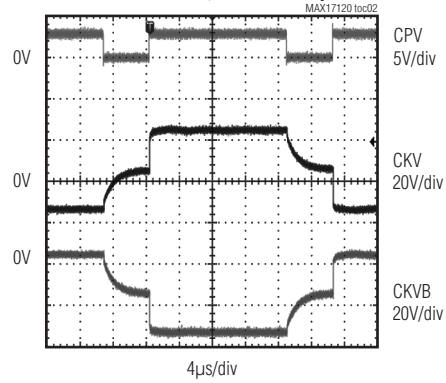
Typical Operating Characteristics

(Circuit of Figure 1, $V_{DD} = V_{EN} = 3.3V$, $V_{ON} = 25V$, $V_{OFF} = -15V$, $T_A = +25^\circ C$, unless otherwise noted.)

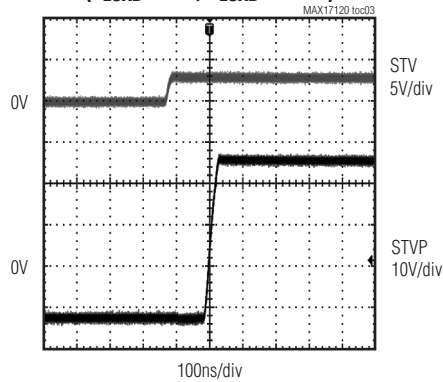
STV/STVP INPUT/OUTPUT WAVEFORMS WITH LOGIC INPUT



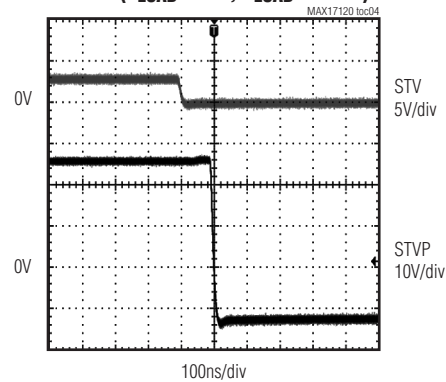
CPV, CKV, AND CKVB INPUT/OUTPUT WAVEFORMS WITH LOGIC INPUT (STV = 0V, $C_{LOAD} = 5nF$, $R_{LOAD} = 50\Omega$, $R_{CS} = 200\Omega$)



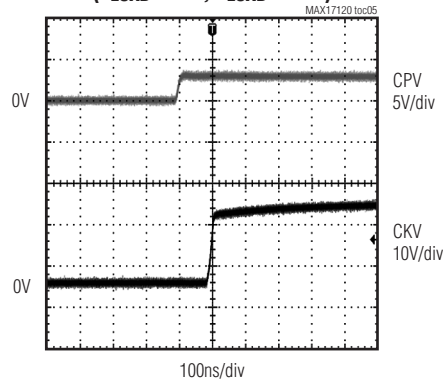
STV RISING EDGE PROPAGATION DELAY ($C_{LOAD} = 5nF$, $R_{LOAD} = 200\Omega$)



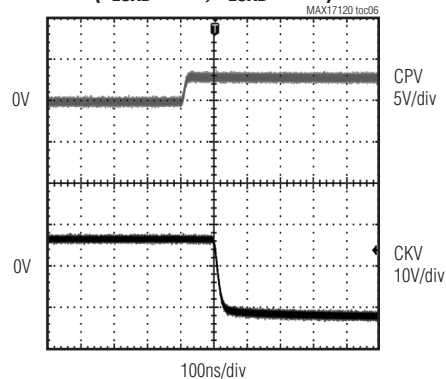
STV FALLING EDGE PROPAGATION DELAY ($C_{LOAD} = 5nF$, $R_{LOAD} = 200\Omega$)



CPV/CKV RISING EDGE PROPAGATION DELAY ($C_{LOAD} = 5nF$, $R_{LOAD} = 50\Omega$)



CPV/CKV FALLING EDGE PROPAGATION DELAY ($C_{LOAD} = 5nF$, $R_{LOAD} = 50\Omega$)



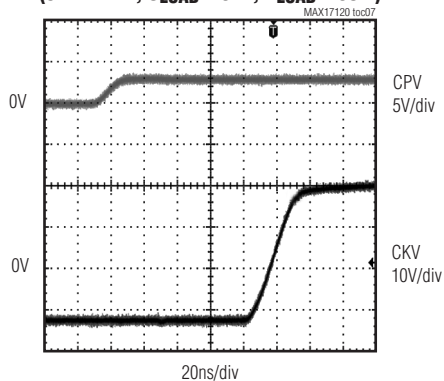
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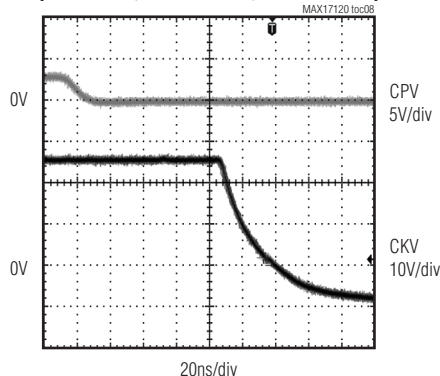
Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{DD} = V_{EN} = 3.3V$, $V_{ON} = 25V$, $V_{OFF} = -15V$, $T_A = +25^\circ C$, unless otherwise noted.)

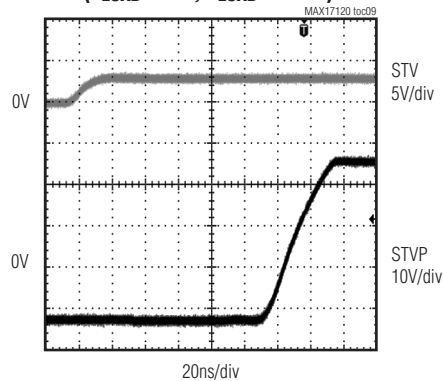
CKV SLEW RATE ON RISING EDGE
(STV = VDD, C_{LOAD} = 5nF, R_{LOAD} = 50Ω)



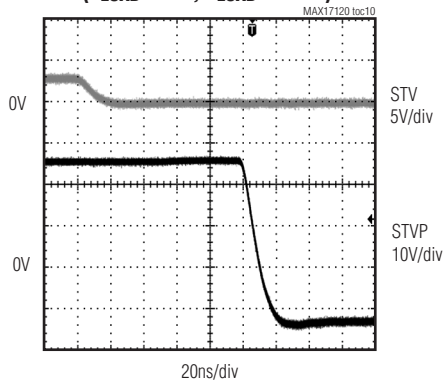
CKV SLEW RATE ON FALLING EDGE
(STV = VDD, C_{LOAD} = 5nF, R_{LOAD} = 50Ω)



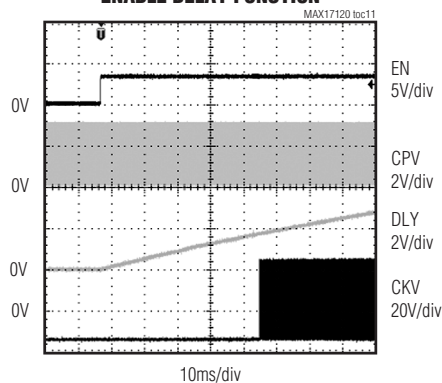
STVP SLEW RATE ON RISING EDGE
(C_{LOAD} = 5nF, R_{LOAD} = 200Ω)



STVP SLEW RATE ON FALLING EDGE
(C_{LOAD} = 5nF, R_{LOAD} = 200Ω)



ENABLE DELAY FUNCTION



Triple High-Voltage Scan Driver for TFT LCD

Pin Description

| PIN | NAME | FUNCTION |
|---------------------------|------------------|--|
| 1 | CKVBCS2 | CKVB2 Charge-Sharing Connection. CKVBCS2 connects to CKVCS2 whenever CPV2 and STV are both low (to make CKV2 and CKVB2 high impedance) to allow CKV2 to connect to CKVB2, sharing charge between the capacitive loads on these two outputs. |
| 2 | CKVB2 | High-Voltage Scan-Drive Output. CKVB2 is the inverse of CKV2 during active states and is high impedance whenever CKV2 is high impedance. |
| 3, 11, 15, 18, 21, 23, 30 | N.C. | Not connected |
| 4 | CKV3 | High-Voltage Scan-Drive Output. When enabled, CKV3 toggles between its high state (connected to V _{ON}) and its low state (connected to V _{OFF}) on each falling edge of the CPV3 input. Further, CKV3 is high impedance whenever CPV3 and STV are both low. |
| 5 | CKVCS3 | CKV3 Charge-Sharing Connection. CKVCS3 connects to CKVBCS3 whenever CPV3 and STV are both low (to make CKV3 and CKVB3 high impedance) to allow CKVB3 to connect to CKV3, sharing charge between the capacitive loads on these two outputs. |
| 6 | CKVBCS3 | CKVB3 Charge-Sharing Connection. CKVBCS3 connects to CKVCS3 whenever CPV3 and STV are both low (to make CKV3 and CKVB3 high impedance) to allow CKV3 to connect to CKVB3, sharing charge between the capacitive loads on these two outputs. |
| 7 | CKVB3 | High-Voltage Scan-Drive Output. CKVB3 is the inverse of CKV3 during active states and is high impedance whenever CKV3 is high impedance. |
| 8 | STVP | High-Voltage Scan-Drive Output. STVP is connected to V _{OFF} when STV is low and is connected to V _{ON} when STV is high and CPV1 is low. When both STV and CPV1 are high, STVP is high impedance. |
| 9 | GND | Ground |
| 10 | STV | Vertical Sync Input. The rising edge of STV begins a frame of data. The STV input is used to generate the high-voltage STVP output. |
| 12 | CPV1 | Vertical Clock Pulse Input. CPV1 controls the timing of the CKV1 and CKVB1 outputs, which change state (by first sharing charge) on its falling edge. |
| 13 | CPV2 | Vertical Clock Pulse Input. CPV2 controls the timing of the CKV2 and CKVB2 outputs, which change state (by first sharing charge) on its falling edge. |
| 14 | CPV3 | Vertical Clock Pulse Input. CPV3 controls the timing of the CKV3 and CKVB3 outputs, which change state (by first sharing charge) on its falling edge. |
| 16 | EN | Enables the MAX17120. Drive EN high to start up the MAX17120 after a delay time, which is set by a capacitor at DLY. |
| 17 | DLY | Startup Delay Setting. Connect a capacitor to adjust the delay based on $t_{DELAY} = C_{DLY} \times 410k\Omega$. |
| 19 | DISH | V _{OFF} Discharge Connection. Pulling DISH below ground activates an internal connection between V _{OFF} and GND, rapidly discharging the V _{OFF} supply. Typically, DISH is capacitively connected to VDD, so that when VDD falls, V _{OFF} is discharged. |
| 20 | VDD | Supply Input. VDD is the logic supply input for the scan driver. Bypass to GND through a minimum 0.1 μ F capacitor. |
| 22 | V _{OFF} | Gate-Off Supply. V _{OFF} is the negative supply voltage for the CKV_, CKVB_, and STVP high-voltage driver outputs. Bypass to GND with a minimum 1 μ F ceramic capacitor. |
| 24 | V _{ON} | Gate-On Supply. V _{ON} is the positive supply voltage for the CKV_, CKVB_, and STVP high-voltage driver outputs. Bypass to GND with a minimum 1 μ F ceramic capacitor. |

Triple High-Voltage Scan Driver for TFT LCD

Pin Description (continued)

| PIN | NAME | FUNCTION |
|-----|---------|--|
| 25 | GND | Ground |
| 26 | CKV1 | High-Voltage Scan-Drive Output. When enabled, CKV1 toggles between its high state (connected to VON) and its low state (connected to VOFF) on each falling edge of the CPV1 input. Further, CKV1 is high impedance whenever CPV1 and STV are both low. |
| 27 | CKVCS1 | CKV1 Charge Sharing Connection. CKVCS1 connects to CKVBCS1 whenever CPV1 and STV are both low (to make CKV1 and CKVB1 high impedance) to allow CKVB1 to connect to CKV1, sharing charge between the capacitive loads on these two outputs. |
| 28 | CKVBCS1 | CKVB1 Charge-Sharing Connection. CKVBCS1 connects to CKVCS1 whenever CPV1 and STV are both low (to make CKV1 and CKVB1 high impedance) to allow CKV1 to connect to CKVB1, sharing charge between the capacitive loads on these two outputs. |
| 29 | CKVB1 | High-Voltage Scan-Drive Output. CKVB1 is the inverse of CKV1 during active states and is high impedance whenever CKV1 is high impedance. |
| 31 | CKV2 | High-Voltage Scan-Drive Output. When enabled, CKV2 toggles between its high state (connected to VON) and its low state (connected to VOFF) on each falling edge of the CPV2 input. Further, CKV2 is high impedance whenever CPV2 and STV are both low. |
| 32 | CKVCS2 | CKV2 Charge-Sharing Connection. CKVCS2 connects to CKVBCS2 whenever CPV2 and STV are both low (to make CKV2 and CKVB2 high impedance) to allow CKVB2 to connect to CKV2, sharing charge between the capacitive loads on these two outputs. |
| — | EP | Exposed Pad. EP is not connected in the IC. The EP should be connected to GND plane on the PCB to improve thermal performance. |

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Triple High-Voltage Scan Driver for TFT LCD

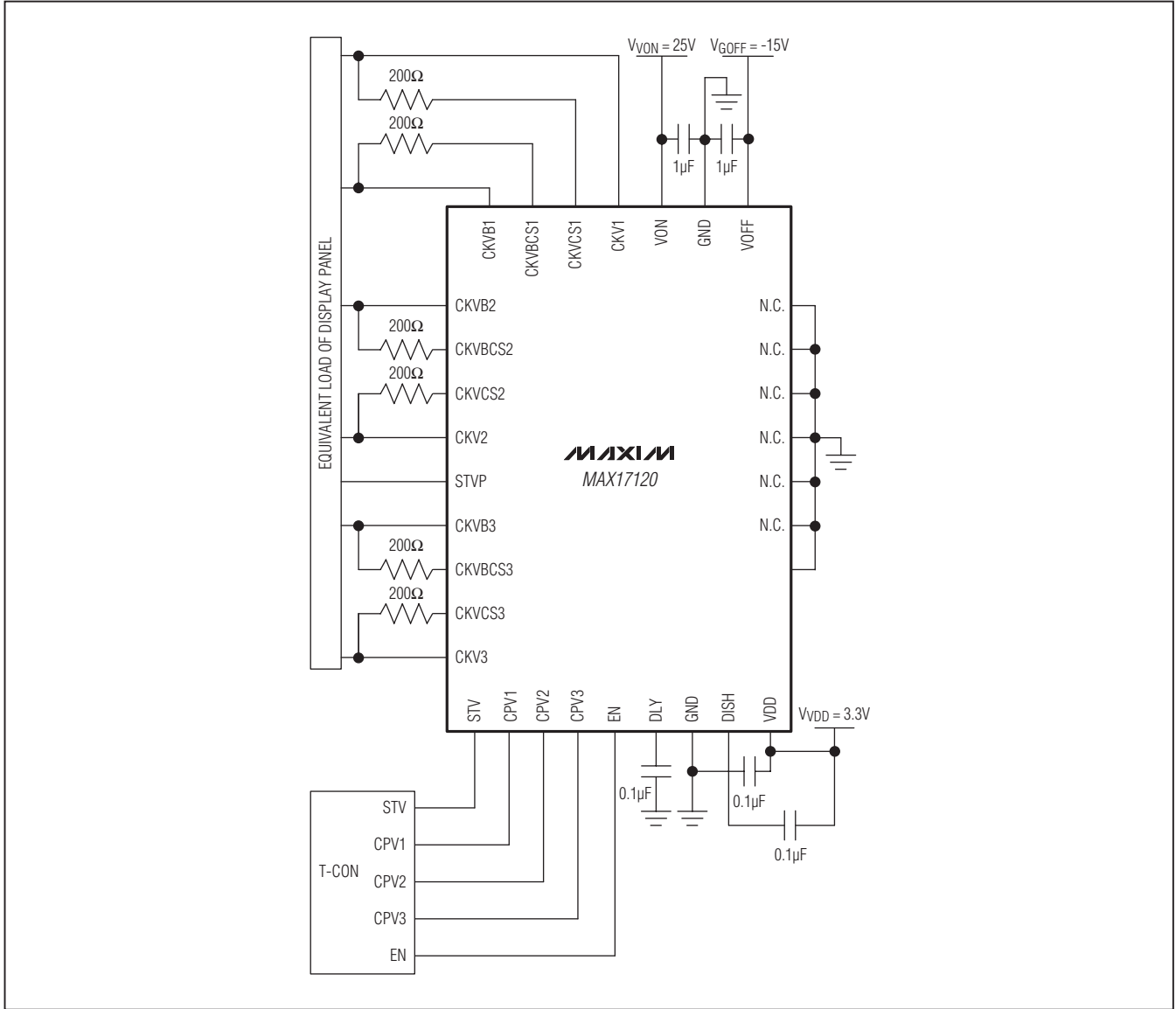


Figure 1. Typical Operating Circuit

Triple High-Voltage Scan Driver for TFT LCD

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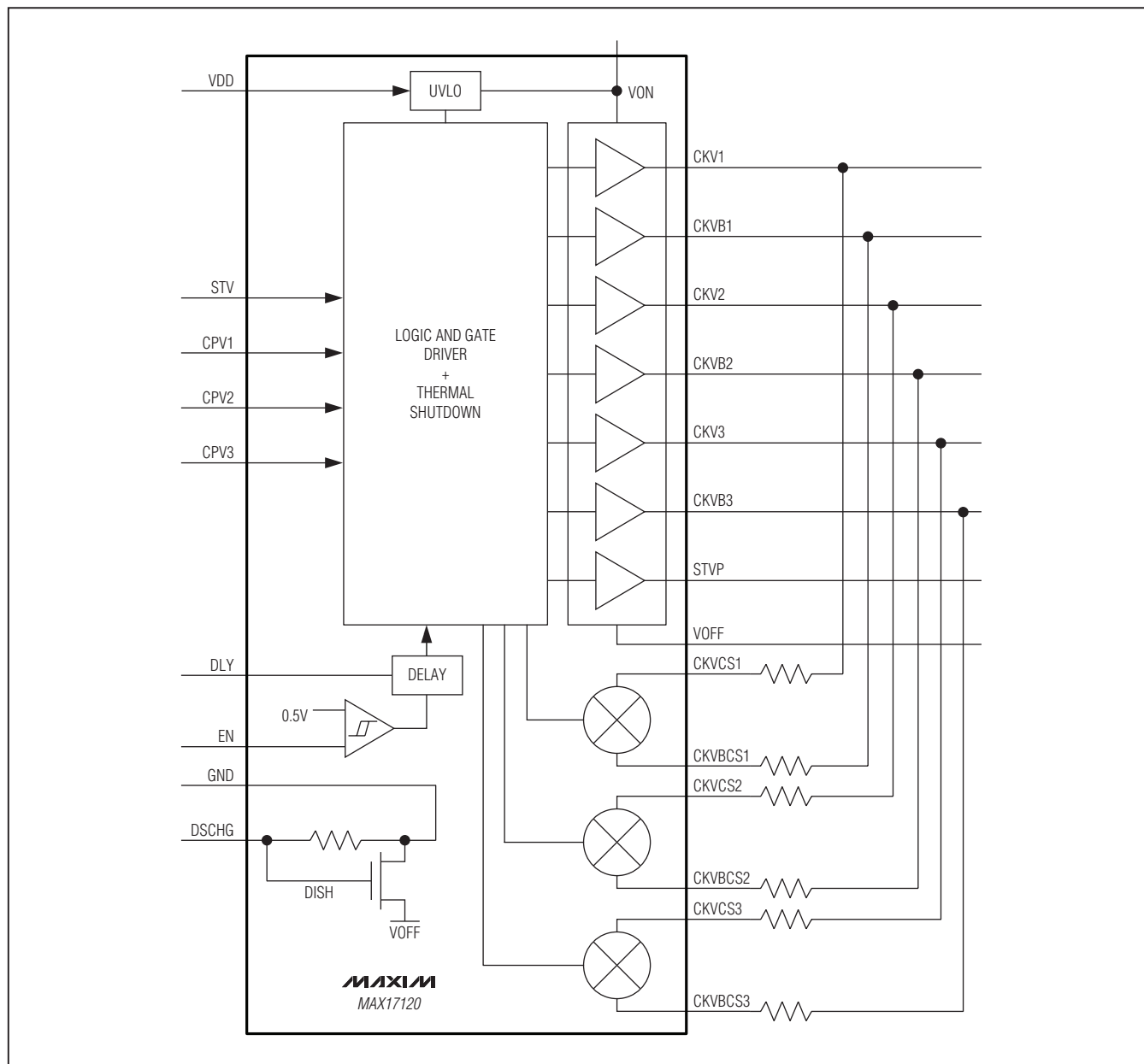


Figure 2. Functional Diagram

Detailed Description

The MAX17120 contains three high-voltage level-shifting scan drivers for active-matrix TFT LCDs. Figure 2 is the functional diagram.

Undervoltage Lockout on VDD

The undervoltage lockout (VDD-UVLO) circuit on VDD compares the input voltage at VDD with the VDD-UVLO (2V typ) to ensure that the input voltage is high enough for reliable operation. There is 100mV of hysteresis to prevent supply transients from causing a restart. When the VDD voltage is below VDD-UVLO, the scan-driver outputs are high impedance.

Triple High-Voltage Scan Driver for TFT LCD

Undervoltage Lockout on VON

The undervoltage lockout (VON-UVLO) circuit on VON compares the input voltage at VON with the VON-UVLO (12V typ) to ensure that the input voltage is high enough for reliable operation. There is 1V of hysteresis to prevent supply transients from causing a restart. When the VON voltage is below VON-UVLO, the scan-driver outputs are high impedance.

High-Voltage Level-Shifting Scan Driver

The MAX17120 includes three high-voltage level-shifting scan drivers. The scan-driver outputs (CKV1, CKV2, CKV3, CKVB1, CKVB2, CKVB3, and STVP) swing between the power-supply rails (VON and VOFF) according to their corresponding input logic levels. The states of the CKV1, CKVB1, and STVP outputs are determined by the input logic levels present on STV and CPV1. The states of the CKV2, CKVB2, and CKV3, CKVB3 outputs are determined by the input logic levels present on STV, CPV2, and STV, CPV3, respectively (see Figure 3, Table 1, and Table 2).

Table 1. STVP Logic

| VON | EN | VDLY | INPUT SIGNALS | | OUTPUT (STVP) |
|--------|----|------|---------------|------|---------------|
| | | | STV | CPV1 | |
| > UVLO | H | H* | L | X | L |
| | | | H | L | H |
| | | | H | H | High-Z |
| | | L* | X | X | L |
| | L | X | X | X | L |
| < UVLO | X | X | X | X | High-Z |

H = high, L = low, high-Z = high impedance, X = Don't care, H* = VDLY > 1/2 x VVDD, L* = VDLY < 1/2 x VVDD.

STV is the vertical timing signal. CPV1, CPV2, and CPV3 are the TFT gate logic timing signals. These signals have CMOS input logic levels set by the VDD supply voltage. CKV1, CKV2, and CKV3 are scan clock outputs, which are complementary to scan clock outputs CKVB1, CKVB2, and CKVB3, respectively. These output signals swing from VON to VOFF, which have a maximum upper level of +40V, a minimum lower level of -30V, and a combined maximum range of VON - VOFF = 65V. Their low output impedance enables them to swiftly drive capacitive loads. Input pins CKVCS1, CKVBSC1, CKVCS2, CKVBSC2, CKVCS3, and CKVBSC3 allow the charge in the panel equivalent capacitors to be shared. This reduces the power loss in state transition.

Enable Function

EN is an active-high logic input that enables/disables the MAX17120 output drive. Drive EN high to enable the MAX17120 scan driver. When EN is low, all the drivers' outputs are pulled to VOFF.

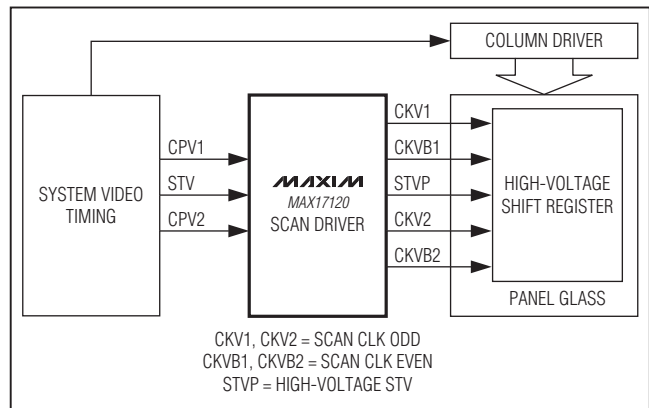


Figure 3. Scan Driver System Diagram

Table 2. CKV_, CKVB_ Logic

| VON | EN | VDLY | INPUT SIGNALS | | OUTPUTS | | |
|--------|-----|------|---------------|------|---------|--------|----------------|
| | | | STV | CPV_ | CKV_ | CKVB_ | CHARGE SHARING |
| > UVLO | H | H* | L | L | High-Z | High-Z | Yes |
| | | | L | ↑ | Toggle | Toggle | No |
| | | | H | L | VOFF | VON | No |
| | | | H | H | VON | VOFF | No |
| | | L* | X | X | VOFF | VOFF | No |
| | Low | X | X | X | VOFF | VOFF | No |
| < UVLO | X | X | X | X | High-Z | | No |

H = high, L = low, high-Z = high impedance, ↑ = rising edge, X = Don't care, H* = VDLY > 1/2 x VVDD, L* = VDLY < 1/2 x VVDD.

Triple High-Voltage Scan Driver for TFT LCD

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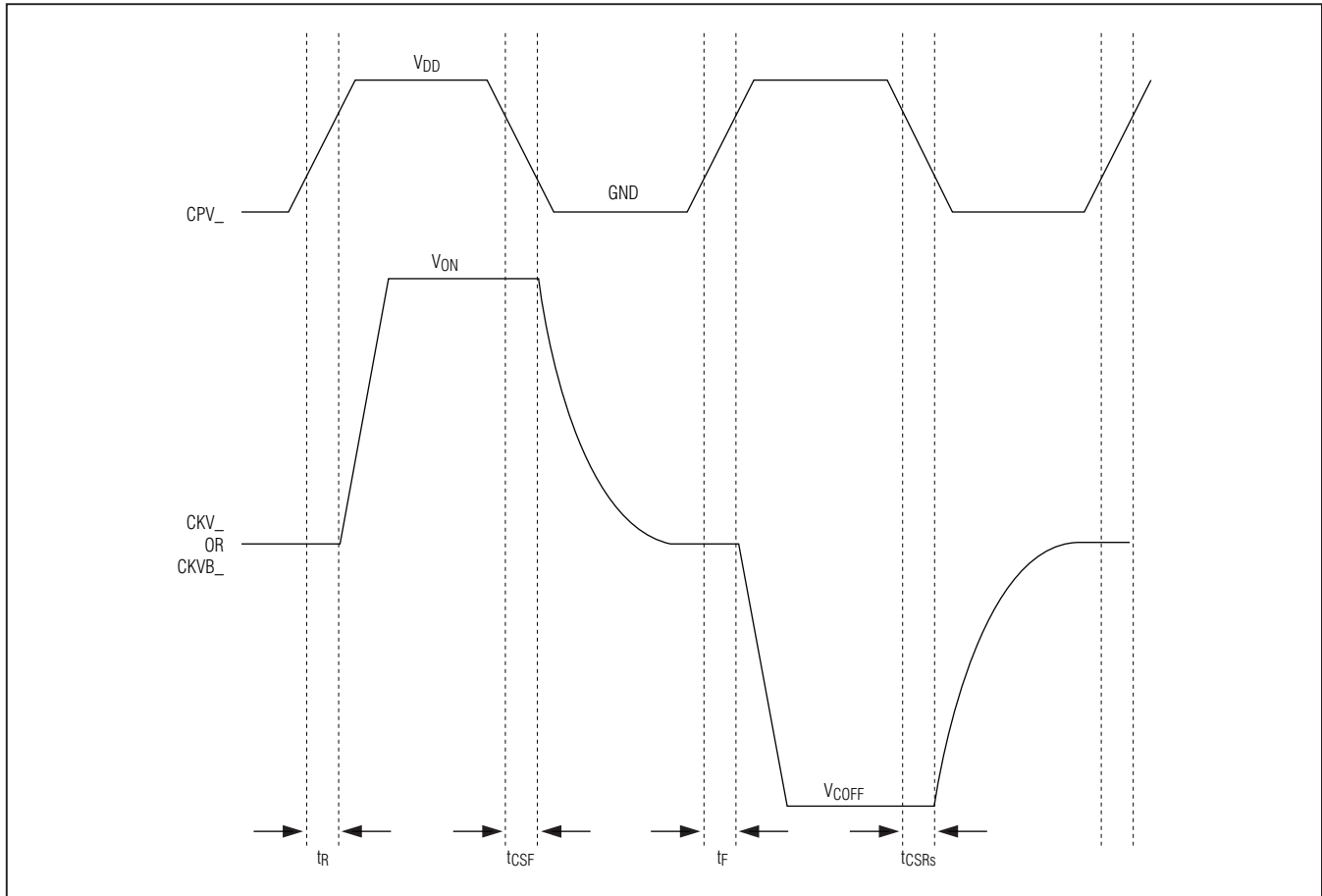


Figure 4. CKV Timing

Delay Function

The DLY input sets the delay time in the startup when the MAX17120 is enabled and the scan-driver outputs are enabled. The delay time is adjustable by choosing a different capacitor at DLY. Calculate the delay capacitance as:

$$C_{DLY} = t_{DELAY}/410k\Omega$$

The delay enable trip point is $V_{VDD}/2$. Before V_{DLY} reaches the threshold, scan-driver outputs stay in the same state as EN is low.

If there is no delay needed in the startup, connect DLY to VDD.

VOFF Rapid-Discharge Function (DISH Input)

The DISH input controls a switch between VOFF and GND. When DISH is pulled below ground by at least 1.5V, VOFF is rapidly discharged to GND. Typically, DISH is capacitively coupled to VDD so that if VDD falls suddenly, VOFF is quickly discharged to GND.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the device. When the junction temperature exceeds $T_J = +160^\circ\text{C}$, a thermal sensor immediately shuts down the scan-driver outputs. The outputs are set to high impedance. Once the device cools down by approximately 15°C , the device reactivates.

The thermal-overload protection protects the IC in the event of overheat conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of $T_J = +150^\circ\text{C}$.

Triple High-Voltage Scan Driver for TFT LCD

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The MAX17120, with its exposed backside paddle soldered to 1in² of PCB copper, can dissipate approximately 27.8mW into +70°C still air. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability.

Scan-Driver Outputs

The power dissipated by the scan-driver outputs (CKV1, CKVB1, STVP, CKV2, and CKVB2), depends on the scan frequency, the capacitive load, and the difference between the VON and VOFF supply voltages. Assuming each output driver is the same capacitance, the power loss is:

$$PD_{SCAN} = 7 \times f_{SCAN} \times C_{PANEL} \times (V_{GON} - V_{GOFF})^2$$

where f_{SCAN} is the scan frequency of the panel, C_{PANEL} is the panel model capacitive load, V_{GON} and V_{GOFF} are the positive gate-on and negative gate-off voltages.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|--------------|--------------|-------------------------|
| 32 TQFN | T-3225 | 21-0140 |

If all the scan drivers operate at a frequency of $f_{SCAN} = 50\text{kHz}$, the load of the six outputs is $C_{PANEL} = 5\text{nF}$, and the supply voltage difference is $V_{ON} - V_{OFF} = 30\text{V}$, then the power dissipated is 1.575W.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Place the VON, VOFF, and VDD pin bypass capacitors as close as possible to the device. The ground connections of the VON, VOFF, and VDD bypass capacitors should be connected directly to the GND pin with a wide trace.
- Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Connect the MAX17120's exposed paddle to GND copper plane and the copper plane area should be maximized to improve thermal dissipation.
- Minimize the length and maximize the width of the traces between the CKV, CKVB, and STV output nodes and the panel load for best transient responses.

Refer to the MAX17120 evaluation kit for an example of proper board layout.

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