

## High Temperature Dual Precision Operational Amplifier HTOP01

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### DESCRIPTION

The HTOP01 is a precision low power op amp, offering very low input offset voltage and drift over an operating temperature range of -55°C to 225°C. Using auto-zeroing techniques input offset voltage is continuously sampled and compensated, providing near perfect offset voltage compensation over temperature and time.

An internal oscillator and logic provides all necessary auto-zero clock signals, and no external capacitors are needed.

The internal auto-zero clock generator produces a pseudo-random clock frequency operating between 2kHz – 4kHz that effectively “spreads out” the clock noise frequency spectrum over a 2kHz span. This greatly reduces detectable clock noise in the amplifier’s output spectrum.

Additionally, an external clock input pin (XCLK) is provided along with a select input pin (SEL) to choose between the internal clock and an optional external clock.



The external clock option allows timing flexibility for synchronously sampled systems, where no clock energy can be tolerated in the sampled amplifier output.

To save power, a power shutdown pin (SHDN) de-powers all analog circuitry when asserted (active high). The current with SHDN asserted is <math><150\mu\text{A}</math> over temperature.

### APPLICATIONS

Downhole Drilling Measurement and Production Tools  
Strain Gauge Transducers  
RTD Temperature Sensing

High Temperature Instrumentation  
High Resolution Data Acquisition  
Low Power Measurement

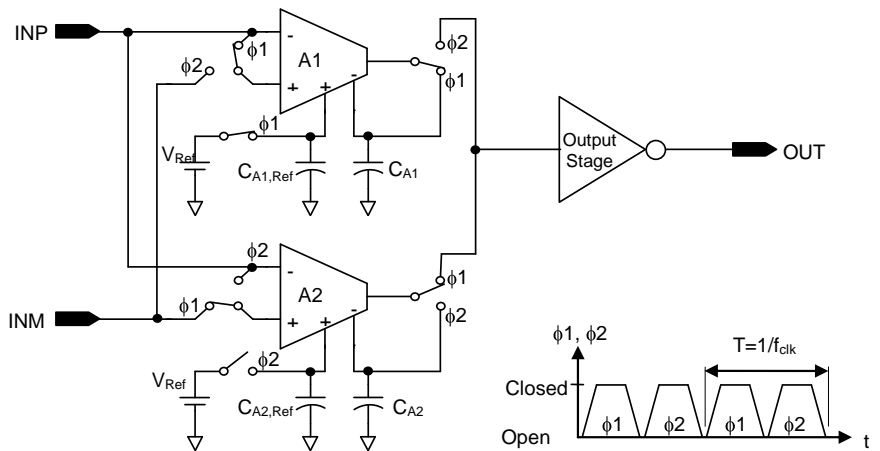
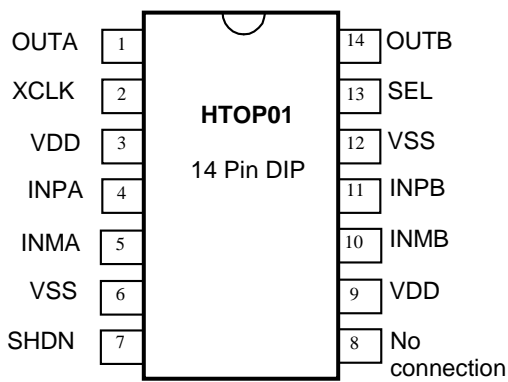
### FEATURES

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- ▶ -55°C to 225°C Ambient Temperature Range
- ▶ Gain-Bandwidth Product: 2.0MHz Typical
- ▶ Continuous Input Offset Voltage Auto-Zeroing With Internal Clock
- ▶ Single 5V Supply Operation
- ▶ Input Offset Voltage  $\pm 100\mu\text{V}$  Max Over Temperature
- ▶ 5.0mA maximum Supply Current
- ▶ Input Offset Drift  $0.2\mu\text{V}/^\circ\text{C}$  Max
- ▶ Power shutdown pin provided
- ▶ High Gain, CMRR: 100dB Min
- ▶ External clocking option for synchronous systems
- ▶ Available in 14 lead DIP package

# HTOP01

## FUNCTIONAL BLOCK DIAGRAM



## SIGNAL DESCRIPTION

Pin Name	Pin Number	Description
SEL	13	Digital input pin. Selects either internal clock (SEL=0) or externally applied clock (SEL=1).
XCLK	2	Digital input pin. External clock input. When SEL=1, XCLK is enabled, and the internal ping-pong amplifier action occurs on each XCLK edge. When SEL=0, XCLK is disabled. When not used, XCLK should be connected to VDD or VSS.
SHDN	7	Digital input pin. Power Shutdown control input. When SHDN=1, all analog circuitry is de-powered/disabled, and only leakage current will flow into VDD. When SHDN=0, normal circuit operation occurs.
INPA, INPB	4, 11	Non-inverting amplifier inputs for amplifier "A" and "B" respectively.
INMA, INMB	5, 10	Inverting amplifier inputs for amplifier "A" and "B" respectively.
OUTA, OUTB	1, 14	Amplifier "A" and "B" outputs.
VDD	3, 9	Positive supply connection.
VSS	6, 12	Negative supply connection.
No connect	8	Pin not used.

## ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating		Units
		Min	Max	
VDD	Supply Voltage (2)	-0.5	6.5	Volts
VPIN	Voltage on Any Pin (2)	-0.5	VDD+0.5	Volts
TSTORE	Storage Temperature	-65	300	°C
IOUT	Average Output Current		50	mA
ESD	Electrostatic Discharge Protection Voltage (3)	1000		V
PJC	Package Thermal Resistance (Junction-to-Case)	14 Pin DIP	15.0	°C/W

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.

(2) Voltage referenced to VSS.

(3) Class 2 Electrostatic Discharge (ESD) input protection voltage per MIL-STD-883, Method 3015

## RECOMMENDED OPERATING CONDITIONS (1)

Symbol	Parameter	Description			Units
		Min	Typ	Max	
VDD	Supply Voltage	4.5	5.0	5.5	Volts
TC	External Package Temperature	-55	25	225	°C
Temp Op	Operating Temperature	-55		225	°C
VPIN	Voltage on Any Pin	-0.3		VDD+0.3	Volts

(1) Voltages referenced to Vss.

## ELECTRICAL CHARACTERISTICS

$V_{DD}=5V$ ,  $V_{SS}=0V$  unless otherwise noted. Values apply over the full  $-55^{\circ}C$  to  $225^{\circ}C$  ambient temperature range except where denoted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OS}$	Input Offset Voltage	SEL=0 (Internal Clock) See Note 6			100	$\mu V$
$\Delta V_{OS}$	Average Input Offset Voltage Drift				0.2	$\mu V/^{\circ}C$
$I_B$	Input Bias Current	$T_A = 25^{\circ}C$ $T_A = -55^{\circ}C$ to $+225^{\circ}C$ See Note 1		$\pm 10$	$\pm 50$ $\pm 150$	$\mu A$ nA
$I_{OS}$	Input Offset Current	$T_A = 25^{\circ}C$ $T_A = -55^{\circ}C$ to $+225^{\circ}C$ See Note 1		$\pm 10$ $\pm 1$		$\mu A$ nA
$e_n$	Input Noise Voltage	RS=100 $\Omega$ , 0.1Hz – 10Hz (internal clock) $25^{\circ}C$ (internal clock) $225^{\circ}C$  (External clock at 30KHz) $25^{\circ}C$		5.7 4.6  1.4		$\mu V$ pk-pk  $\mu V$ pk-pk
$I_R$	Input Range		$V_{SS}$		$V_{DD} - 2.0$	Volts
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0V$ to $V_{DD} - 2.0V$ (Measured at DC)	100			dB
PSRR	Power Supply Rejection Ratio	$V_{SS} = 0$ , $4.75V \leq V_{DD} \leq 5.25V$ (Measured at DC)	90			dB
$A_{VOL}$	Large Signal Voltage Gain	$R_L = 10k\Omega$ (Measured at DC)	100			dB
GBWP	Gain-Bandwidth Product	$R_L = 10k\Omega$ , $C_L = 20pF$		2.0		MHz
SR	Slew Rate	$R_L = 10k\Omega$		1.5		V/ $\mu s$
	Overload Recovery Time	$R_L = 10k\Omega$ $C_L = 20pF$  Positive Negative		140 35		$\mu s$
$I_O$	Output Current	Output swings ( $V_{DD}-0.3V$ ) – ( $V_{SS}+0.3V$ ) See Note 2	$\pm 20$			mA
$I_{OSC}$	Output Short-Circuit Current	Output shorted to $V_{DD}$ , $V_{SS}$ See Note 4		$\pm 50$		mA
$f_{CLK}$	Clock Frequency	Internally generated clock. See Note 5		2 - 4		kHz
$V_{DD} - V_{SS}$	Operating Supply Range		4.75		5.25	Volts
$I_{SUP}$	Supply Current, Total Package	See Note 3			5.0	mA
$V_{IH}$	Digital Input High Voltage	Applies to XCLK, SEL, SHDN pins	$V_{DD} - 0.3$		$V_{DD} + 0.1$	Volts

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IL}$	Digital Input Low Voltage	Applies to XCLK, SEL, SHDN pins	$V_{SS} - 0.1$		$V_{SS} + 0.3$	Volts
$I_{SHDN}$	Supply Current w/SHDN asserted	SHDN=1			150	$\mu A$

## Notes

(1) As temperature increases, current into the op amp inputs becomes dominated by leakage current from the input protect diodes. At 250°C junction temperature, diode leakage current can reach  $\pm 100nA$  when the input level is near VDD or VSS. Net leakage current drops significantly as the input level approaches mid-rail, and is at a minimum when the input level is precisely midway between VDD and VSS.

Additionally, the diode structures on each input are well matched to each other, and will exhibit nearly identical leakage current behavior. Consequently, offset current IOS between the two inputs is typically about  $\pm 1\%$  of the IB level. Thus, if the input level is maintained near mid-rail, IOS is very low ( $< 1nA$ ), even at 250°C junction temperature.

(2) Output drive current capability is related to output swing magnitude. The HTOP01 will sink and source 20mA minimum over temperature with the output swinging to within 300mV of either rail. At lesser loads, the output can swing closer to the supply rails; at loads of  $\leq 1mA$ , the output will reach to within  $\sim 10mV$  of either rail. For applications where the output remains  $\geq 500mV$  away from the rails, up to  $\pm 40mA$  output current is available. Current limiting activates when output current exceeds approximately  $\pm 50mA$ .

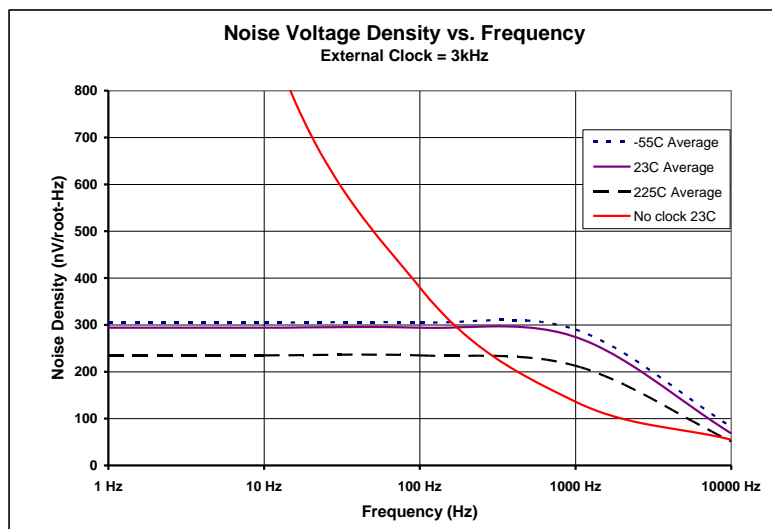
(3) Supply current consumed by each op amp is PTAT (Proportional To Absolute Temperature) in nature, and as the name suggests increases proportional to temperature. The 5.0mA maximum current given in the table reflects the maximum current consumed at 250°C junction temperature by both amplifiers. At 25°C junction temperature, supply current is typically 2mA. PTAT biasing maintains a near-constant amplifier bandwidth over temperature, a desirable characteristic.

(4) The HTOP01 is designed to handle  $\pm 50mA$  output current per amplifier continuously over temperature, with no reduction in rated product life. In the event of an overload condition, current limiting activates and limits output current to  $\sim 50mA$  nominally. However, due to fabrication process variations, the current limiting threshold can vary up to  $\pm 30\%$ . Consequently, it is possible to have a current limiting threshold as high as  $\sim 65mA$ . In this situation, if the overload (65mA) is allowed to continue indefinitely at 225°C ambient, there can be a reduction in rated product life. For maximum product life, it is recommended that any overload output current situation ( $> 50mA$ ) be attended to promptly.

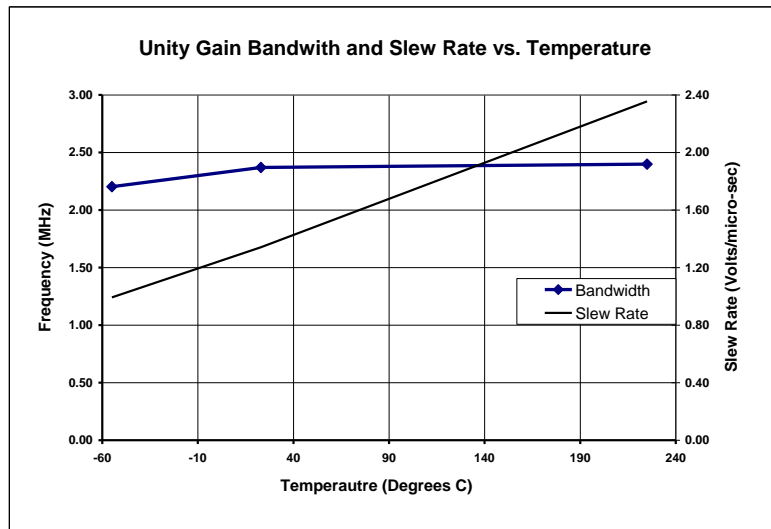
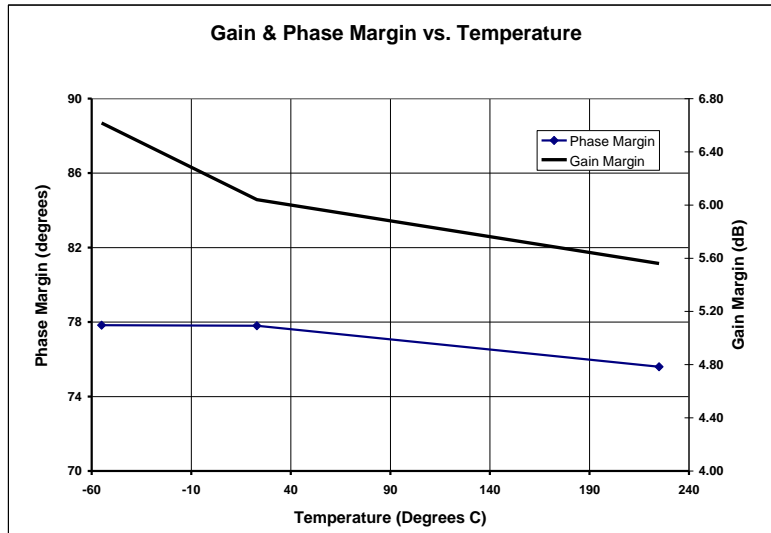
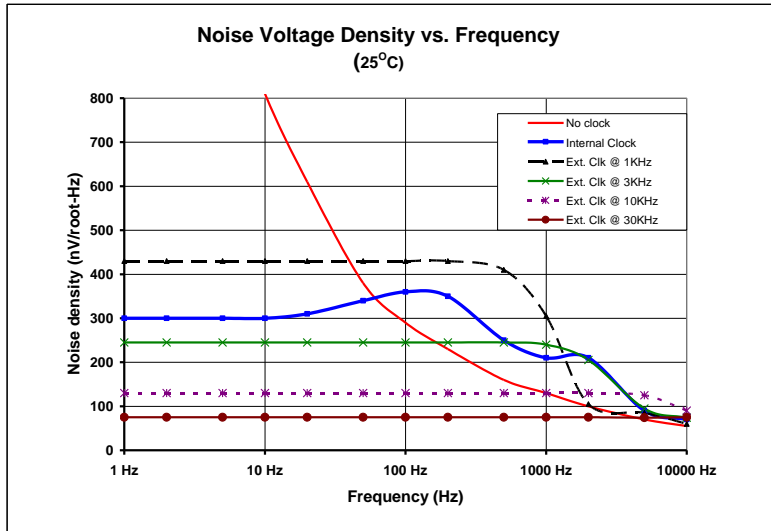
(5) The pseudo-random amplifier auto-zero clock is derived from an on-chip oscillator running at a nominal frequency of 4.0MHz.

(6) With SEL=0 the HTOP01 uses an internally generated clock for offset compensation. Setting SEL=1 and using an external clock provides superior offset performance over the internal clock. The recommended frequency range for an external clock is from 4KHz to 100KHz. Optimum performance is achieved with an external clock frequency of approximately 30KHz.

## TYPICAL PERFORMANCE PLOTS



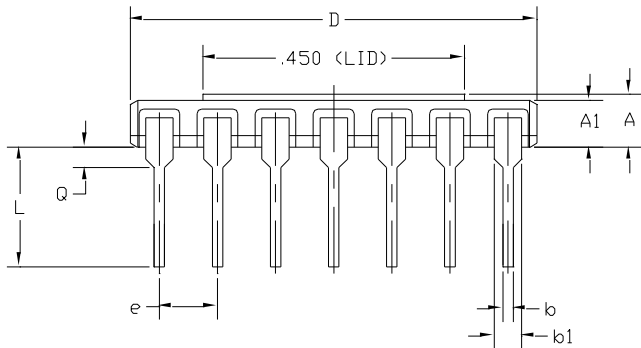
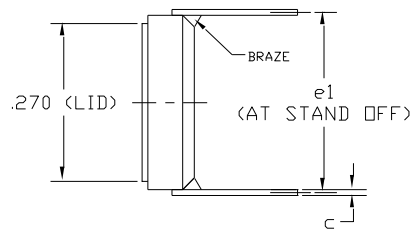
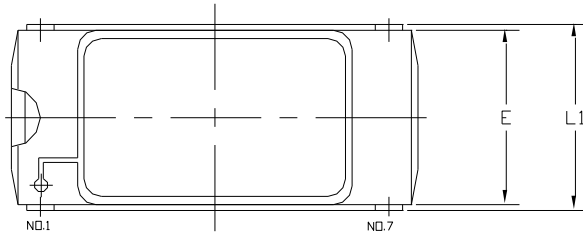
TYPICAL PERFORMANCE PLOTS



# HTOP01

## PACKAGE INFORMATION

### 14 Lead Ceramic DIP Package



SYMBOL	COMMON DIMENSIONS MILLIMETERS			COMMON DIMENSIONS INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.09	2.33	2.59	.083	.092	.102
A1	1.83	2.03	2.23	.072	.080	.088
b	0.41	0.46	0.51	.016	.018	.020
b1	1.14	1.19	1.24	.045	.047	.049
c	0.20	0.25	0.30	.008	.010	.012
D	17.58	17.78	17.98	.692	.700	.708
E	7.25	7.50	7.75	.285	.295	.305
e	2.41	2.54	2.67	.095	.100	.105
e1	7.37	7.62	7.87	.290	.300	.310
L	---	4.93	---	---	.194	---
L1	7.62	7.87	8.12	.300	.310	.320
Q	0.64	0.89	1.14	.025	.035	.045

## APPLICATION NOTES

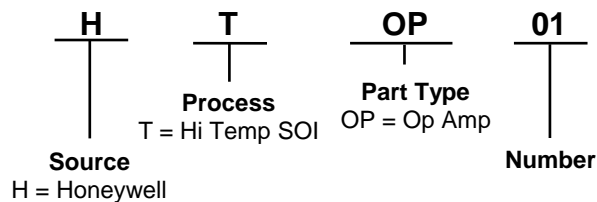
### 1. SUPPLY BY-PASS CAPACITANCE

In order to minimize the effects of supply-coupled clock noise on amplifier output it is recommended that a supply by-pass capacitor with low equivalent series resistance be connected between VDD and VSS.

### 2. INPUT IMPEDANCE MATCHING

At high temperature input currents into the HTOP01 will increase due primarily to leakage of the input ESD protection diodes. It is therefore helpful to minimize and/or balance input impedance to avoid voltage offsets from input current flowing in external connections.

## ORDERING INFORMATION <sup>(1)</sup>



### Notes

(1.) Bare die deliverable is an option with the HTOP01. Contact factory for more information and availability.

## Find out more

For more information on Honeywell's High Temperature Electronics visit us online at [www.honeywell.com/hightemp](http://www.honeywell.com/hightemp), or contact us at 800-323-8295 or 763-954-2474. Customer Service Email: [ps.customer.support@honeywell.com](mailto:ps.customer.support@honeywell.com).

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