AK4618

192kHz 24-bit 6ch/12ch Audio CODEC with Microphone Interface

GENERAL DESCRIPTION

The AK4618 is a single chip audio CODEC that includes 6-channel ADC and 12-channel DAC. The 6-channel ADC supports differential/single-ended analog inputs. The high performance 12-channel DAC integrates full-range digital volume control and achieves 106dB dynamic range. A car audio system can be easily designed with an audio DSP and the AK4618. The AK4618 is housed in a space saving 48-pin LQFP package.

FEATURES

- ☐ **6ch ADC**
  - **Sampling Frequency: 8KHz~48KHz**
  - **ADC S/N: 98dB, S/ (N+D): 87dB**
  - **I/F format: MSB justified, I^2S or TDM**
- ☐ **12ch DAC**
  - **Sampling Frequency: 8KHz~192KHz**
  - **DAC S/N: 106dB, S/ (N+D): 92dB**
  - **I/F format: MSB justified, LSB justified (16bit, 24bit), I^2S or TDM**
  - **Channel Independent Digital Attenuator (Linear 256 steps)**
- ☐ **Microphone Interface**
  - **Single-ended/Differential Input Select**
  - **Programmable Gain (+33dB ~ +15dB and 0dB, 3dB step)**
  - **Low Noise Microphone Bias**
- ☐ **Master / Slave mode**
- ☐ **Master clock**
  - **Slave mode: 256fs, 384fs or 512fs (Normal Speed Mode: fs=8kHz ~ 48kHz)**
    256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
    128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)
  - **Master mode: 256fs, 384fs or 512fs (Normal Speed Mode: fs=8kHz ~ 48kHz)**
    256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
    128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)
- ☐ **µP I/F: I^2C**
- ☐ **Power supply**
  - **Analog Power Supply: 3.0V ~ 3.6V (typ.3.3V)**
  - **Digital I/O Power Supply: 3.0V ~ 3.6V (typ.3.3V)**
- ☐ **Operating temperature range: -40°C ~ 105°C**
- ☐ **Package: 48pin LQFP**

■ Block Diagram

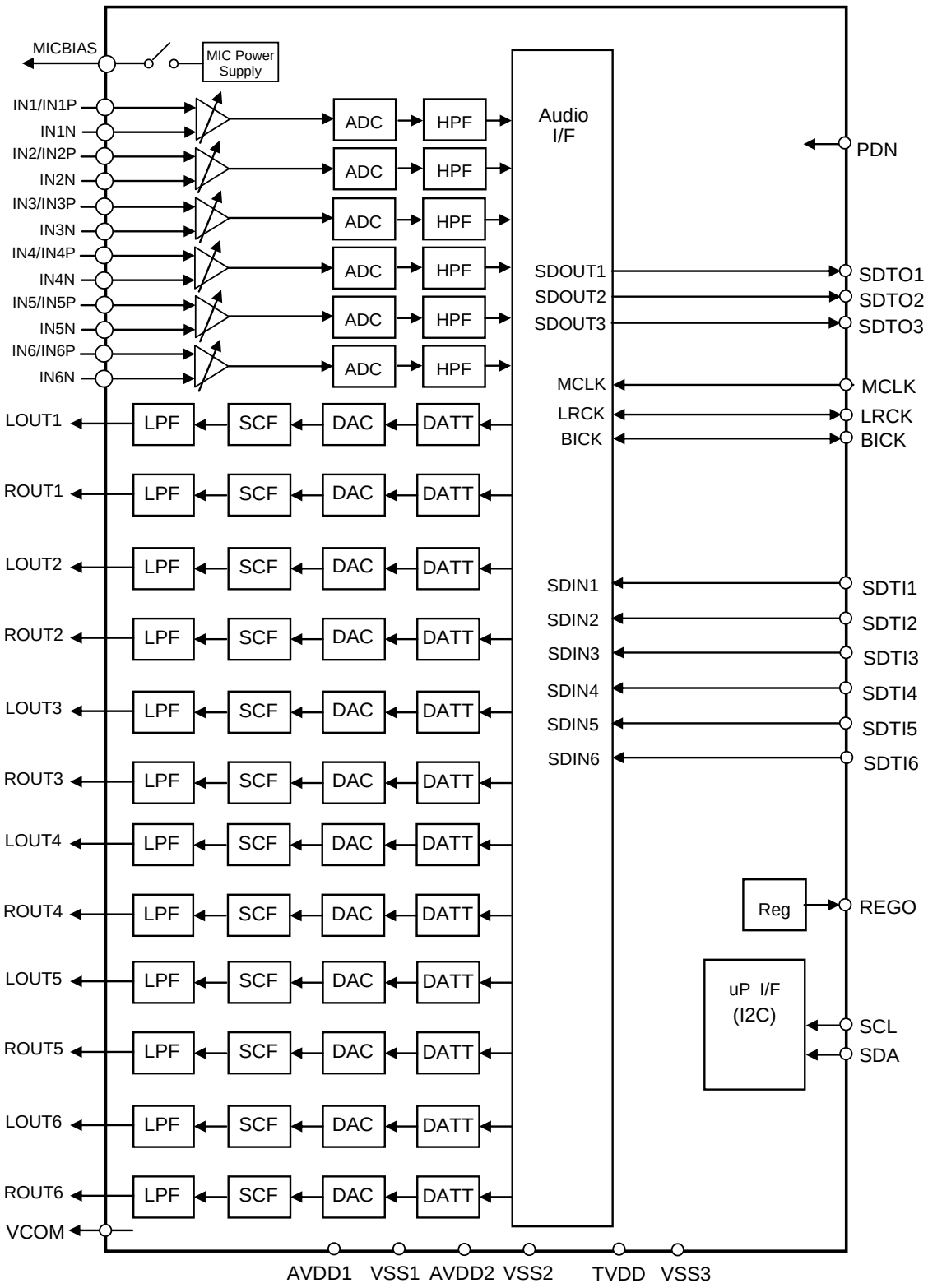
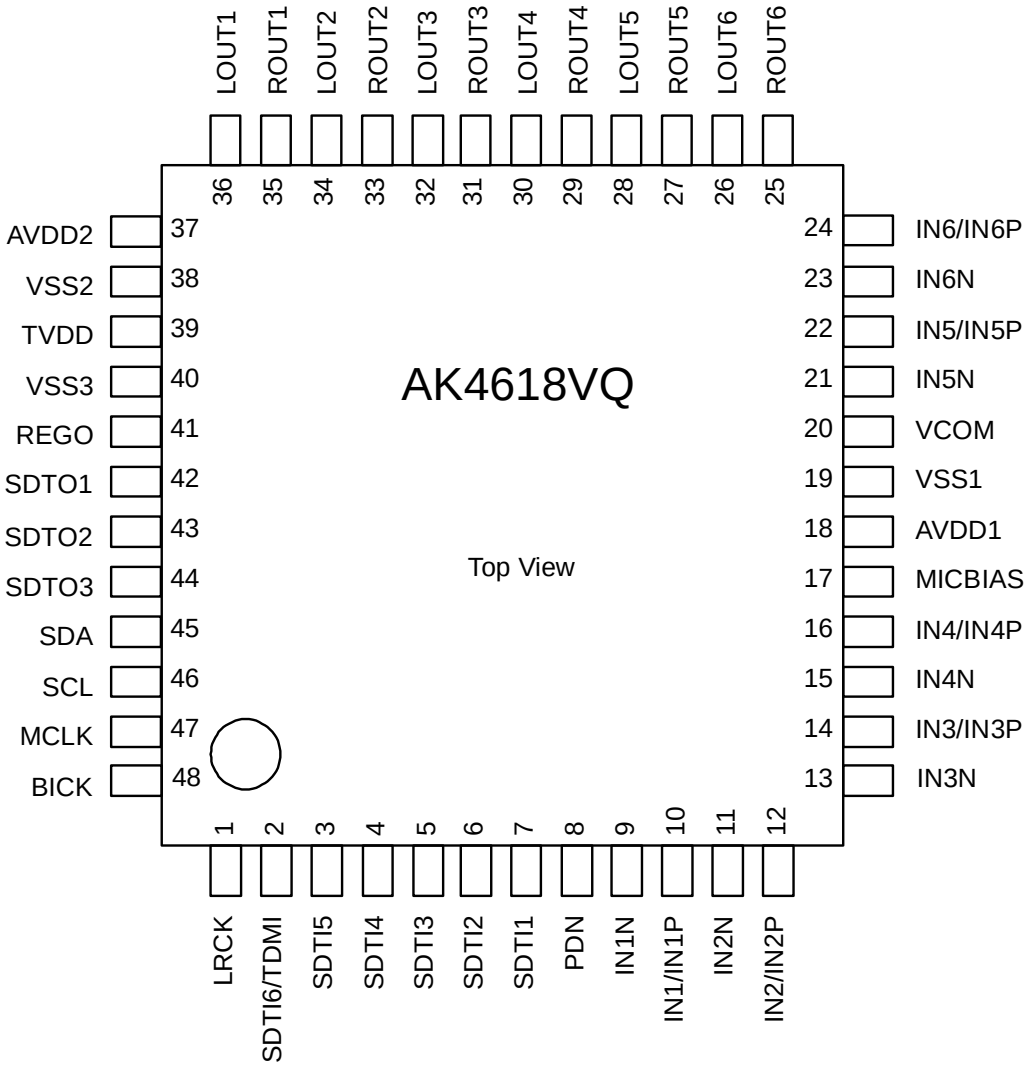


Figure 1. Block Diagram

■ Ordering Guide

AK4618VQ	–40 ~ +105°C	48pin LQFP (0.5mm pitch)
AKD4618	Evaluation Board for AK4618	

■ Pin Layout



■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	IN1/IN1P, IN1N, IN2/IN2P, IN2N, IN3/IN3P, IN3N, IN4/IN4P, IN4N, IN5/IN5P, IN5N, IN6/IN6P, IN6N	Open
	MICBIAS	Open
	LOUT1-6, ROUT1-6	Open
Digital	SDTI1-6	Connect to VSS3
	SDTO1-3	Open

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LRCK	I/O	Input Channel Clock Pin
2	SDTI6	I	(TDM1-0 bits = "00") Audio Serial Data Input 6 Pin
	TDMI	I	(TDM1-0 bits = "01" or "10") TDM Data Input Pin
3	SDTI5	I	Audio Serial Data Input 5 Pin
4	SDTI4	I	Audio Serial Data Input 4 Pin
5	SDTI3	I	Audio Serial Data Input 3 Pin
6	SDTI2	I	Audio Serial Data Input 2 Pin
7	SDTI1	I	Audio Serial Data Input 1 Pin
8	PDN	I	Power-Down & Reset Pin When "L", the AK4618 is powered-down and the control registers are reset to default state.
9	IN1N	I	(MDIE1 bit = "1") Differential Analog Negative input 1 pin
10	IN1	I	(MDIE1 bit = "0") Single-ended Analog Input 1 pin
	IN1P	I	(MDIE1 bit = "1") Differential Analog Positive input 1 pin
11	IN2N	I	(MDIE2 bit = "1") Differential Analog Negative input 2 pin
12	IN2	I	(MDIE2 bit = "0") Single-ended Analog Input 2 pin
	IN2P	I	(MDIE2 bit = "1") Differential Analog Positive input 2 pin
13	IN3N	I	(MDIE3 bit = "1") Differential Analog Negative input 1 pin
14	IN3	I	(MDIE3 bit = "0") Single-ended Analog Input 1 pin
	IN3P	I	(MDIE3 bit = "1") Differential Analog Positive input 1 pin
15	IN4N	I	(MDIE4 bit = "1") Differential Analog Negative input 2 pin
16	IN4	I	(MDIE4 bit = "0") Single-ended Analog Input 2 pin
	IN4P	I	(MDIE4 bit = "1") Differential Analog Positive input 2 pin
17	MICBIAS	O	Microphone bias pin.
18	AVDD1	-	Analog Power Supply Pin, 3.0V~3.6V
19	VSS1	-	Ground Pin, 0V
20	VCOM	O	Common Voltage Output Pin, AVDD1x1/2 Large external capacitor around 1µF is used to reduce power-supply noise.
21	IN5N	I	(MDIE5 bit = "1") Differential Analog Negative input 1 pin
22	IN5	I	(MDIE5 bit = "0") Single-ended Analog Input 1 pin
	IN5P	I	(MDIE5 bit = "1") Differential Analog Positive input 1 pin
23	IN6N	I	(MDIE6 bit = "1") Differential Analog Negative input 2 pin
24	IN6	I	(MDIE6 bit = "0") Single-ended Analog Input 2 pin
	IN6P	I	(MDIE6 bit = "1") Differential Analog Positive input 2 pin
25	ROUT6	O	Rch Analog Output 6 Pin
26	LOUT6	O	Lch Analog Output 6 Pin

27	ROUT5	O	Rch Analog Output 5 Pin
28	LOUT5	O	Lch Analog Output 5 Pin
29	ROUT4	O	Rch Analog Output 4 Pin
30	LOUT4	O	Lch Analog Output 4 Pin
31	ROUT3	O	Rch Analog Output 3 Pin
32	LOUT3	O	Lch Analog Output 3 Pin
33	ROUT2	O	Rch Analog Output 2 Pin
34	LOUT2	O	Lch Analog Output 2 Pin
35	ROUT1	O	Rch Analog Output 1 Pin
36	LOUT1	O	Lch Analog Output 1 Pin
37	AVDD2	-	Analog Power Supply Pin, 3.0V~3.6V
38	VSS2	-	Ground Pin, 0V
39	TVDD	-	Digital Power Supply Pin, 3.0V~3.6V
40	VSS3	-	Ground Pin, 0V
41	REGO	O	Regulator Output Pin This pin should be connected to ground with 1.0uF.
42	SDTO1	O	Audio Serial Data Output Pin1
43	SDTO2	O	Audio Serial Data Output Pin2
44	SDTO3	O	Audio Serial Data Output Pin3
45	SDA	I/O	Control Data Input Pin in I^2C Bus Serial control mode
46	SCL	I	Control Data Clock Pin in I^2C Bus serial control mode
47	MCLK	I	External Master Clock Input Pin
48	BICK	I/O	Audio Serial Data Clock Pin

Note 1. All digital input pins must not be allowed to float.

ABSOLUTE MAXIMUM RATINGS

(VSS1 ~ 3 = 0V; Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog1	AVDD1	-0.3	6.0	V
	Analog2	AVDD2	-0.3	6.0	V
	Digital1	TVDD	-0.3	6.0	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD1+0.3	V
Digital Input Voltage (MCLK, LRCK, BICK, SDTI1-6/TDMI, SCL, SDA, PDN pins)		VIND	-0.3	TVDD+0.3	V
Ambient Temperature (power applied)(Note 3)		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground. VSS1 ~ 3 must be connected to the same analog ground plane.
Note 3. In case that PCB wiring density is 100%.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1 ~ 3 = 0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 4)	Analog	AVDD1, AVDD2	3.0	3.3	3.6	V
	Digital	TVDD	3.0	3.3	3.6	V
	Difference	AVDD1, AVDD2 – TVDD	-0.1	0	+0.1	V

Note 4. The power up sequence between AVDD1, AVDD2 and TVDD is not critical. Each power supplies should be powered up during the PDN pin = "L". The PDN pin should be "H" after all power supplies are powered up. All power supplies should be powered on, only a part of these power supplies cannot be powered off. (Power off means power supplies equal to ground or power supplies are floating.) Do not turn off only the AK4618 under the condition that a surrounding device is powered on and the I2C bus is in use. AVDD1 and AVDD2 must be connected with the same power supply.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25ºC; AVDD1, AVDD2=TVDD=3.3V, VSS1 ~ 3 =0V, BICK=64fs; Signal frequency 1kHz; Measurement frequency = 20Hz~20kHz @fs=48kHz, 20Hz~40kHz at fs=96kHz, 20Hz~40kHz at fs=192kHz; Unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
MIC AMP						
Input Resistance			40			kΩ
Gain	MGAIN[2:0]bits=0h			0		dB
	MGAIN[2:0]bits=1h			15		dB
	MGAIN[2:0]bits=2h			18		dB
	MGAIN[2:0]bits=3h			21		dB
	MGAIN[2:0]bits=4h			24		dB
	MGAIN[2:0]bits=5h			27		dB
	MGAIN[2:0]bits=6h			30		dB
	MGAIN[2:0]bits=7h			33		dB
MIC BIAS						
Bias Output Voltage	Load current = 0mA			2.40		V
	Load current = 6mA			2.40		V
Load Resistance			0.4			kΩ
Load Capacitance					30	pF
ADC Analog Input Characteristics(Differential inputs)						
Resolution					24	Bits
S/(N+D) (-1dBFS)	MGAIN[2:0]bits=0h(0dB)		77	87		dB
	MGAIN[2:0]bits=3h(+21dB)			80		dB
DR (-60dBFS with A-weighted)	MGAIN[2:0]bits=0h(0dB)		88	98		dB
	MGAIN[2:0]bits=3h(+21dB)			85		dB
S/N (A-weighted)	MGAIN[2:0]bits=0h(0dB)		88	98		dB
	MGAIN[2:0]bits=3h(+21dB)			85		dB
Interchannel Isolation				110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20		ppm/°C
Input Voltage	Single-ended (AIN=0.81x AVDD1)			2.67		Vpp
	Differential (AIN=±0.81x AVDD1)			±2.67		Vpp
Power Supply Rejection Ratio (Note 5)				60		dB
DAC Analog Output Characteristics						
Resolution					24	Bits
S/(N+D) (0dBFS)	fs=48kHz	BW=20kHz	82	92		dB
	fs=96kHz	BW=40kHz		90		dB
	fs=192kHz	BW=40kHz		90		dB
DR (-60dBFS with A-weighted)			100	106		dB
S/N (A-weighted)			100	106		dB
Interchannel Isolation				100		dB
Interchannel Gain Mismatch (Note 6)				0	0.7	dB
Gain Drift				20		ppm/°C
Output Voltage	AOUT=0.86x AVDD2		2.54	2.83	3.12	Vpp
Load Resistance (AC Load)			5			kΩ
Load Capacitance					30	pF
Power Supply Rejection (Note 5)				60		dB

Note 5. PSRR is applied to AVDD1, AVDD2 and TVDD with 1kHz, 50mVpp.
Note 6. Channel gain mismatch between all output channels (LOUT1-6, ROUT1-6).

Parameter		Min.	Typ.	Max.	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
AVDD1+AVDD2	fs=48kHz		55	77	mA
AVDD1+AVDD2	fs=96kHz, 192kHz		40		mA
TVDD	fs=48kHz		8	12	mA
TVDD	fs=96kHz		7		mA
TVDD	fs=192kHz		10		mA
Power-down mode (PDN pin = "L") (Note 7)					
AVDD1+AVDD2+TVDD			10	200	μA

Note 7. In the power-down mode, all digital input pins including clock pins are held VSS3.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF): Sharp roll-off mode (SD_AD bit = "0")						
Passband (Note 8)	±0.16dB	PB	0	-	18.8	kHz
	–0.28dB		-	20.0	-	kHz
	–3.0dB		-	22.8	-	kHz
Stopband (Note 8)		SB	28.4	-	-	kHz
Stopband Attenuation		SA	71	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	15.5	-	1/fs
ADC Digital Filter (Decimation LPF): Short delay Sharp roll-off mode (SD_AD bit = "1")						
Passband (Note 8)	±0.16dB	PB	0	-	18.8	kHz
	–0.28dB		-	20.0	-	kHz
	–3.0dB		-	22.8	-	kHz
Stopband (Note 8)		SB	28.4		-	-
Stopband Attenuation		SA	72		-	-
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	2.4	1/fs
Group Delay (Note 10)		GD	-	5.5	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3.0dB	FR	-	3.7	-	Hz
	–0.5dB		-	10.9	-	Hz
	–0.1dB		-	24.0	-	Hz

FILTER CHARACTERISTICS (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	19.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR	-	-0.1	-	dB
DAC Digital Filter (LPF): Slow roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	 22.5	9.8 -	kHz kHz
Stopband		SB	40.1			kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		6.8		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR		-4.0		dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	6.2	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR		-0.1		dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode (DEM=OFF; SD_DA bit="1" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	- 22.5	9.8 -	kHz kHz
Stopband		SB	40.1	-	-	kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR	-	-4.0	-	dB

FILTER CHARACTERISTICS (fs=96kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB –6.0dB	PB	0 -	- 48.0	43.6 -	kHz kHz
Stopband		SB	52.4	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	19.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR	-	-0.3	-	dB
DAC Digital Filter (LPF): Slow roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB –6.0dB	PB	0 -	 45.0	19.6 -	kHz kHz
Stopband		SB	80.2			kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		6.8		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR		-4.2		dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB –6.0dB	PB	0 -	- 48.0	43.6 -	kHz kHz
Stopband		SB	52.4	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	6.2	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR		-0.3		dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode (DEM=OFF; SD_DA bit="1" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB –6.0dB	PB	0 -	- 45.0	19.6 -	kHz kHz
Stopband		SB	80.2	-	-	kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR	-	-4.2	-	dB

FILTER CHARACTERISTICS (fs=192kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB –6.0dB	PB	0 -	- 96.0	87.2 -	kHz kHz
Stopband		SB	104.8	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	19.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR	-	-1.0	-	dB
DAC Digital Filter (LPF): Slow roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB –6.0dB	PB	0 -	 90.0	39.2 -	kHz kHz
Stopband		SB	160.4			kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		6.8		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR		-5.0		dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB –6.0dB	PB	0 -	- 96.0	87.2 -	kHz kHz
Stopband		SB	104.8	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	6.2	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR		-1.0		dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode (DEM=OFF; SD_DA bit="1" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB –6.0dB	PB	0 -	- 90.0	39.2 -	kHz kHz
Stopband		SB	160.4	-	-	kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR	-	-5.0	-	dB

Note 8. The passband and stopband frequencies scale with fs (sampling frequency). For example, ADC: Passband (±0.1dB) = 0.375 x fs, DAC: Passband (±0.06dB) = 0.454 x fs (@ fs=48kHz).

Note 9. The passband and stopband frequencies scale with fs (sampling frequency). For example, DAC: Passband (±0.06dB) = 0.204 x fs (@ fs=48kHz).

Note 10. The calculated delay time is resulting from digital filtering. For the ADC, this time is from the input of an analog signal to the setting of 24bit data for both channels to the ADC output register. For the DAC, this time is from setting the 24 bit data both channels at the input register to the output of an analog signal.

Note 11. The reference frequency is 1kHz.

DC CHARACTERISTICS

(Ta=-40°C~+105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage (MCLK, LRCK, BICK, SDTI1-6/TDMI, SCL, SDA, PDN pins)	VIH	70% TVDD	-	-	V
Low-Level Input Voltage (MCLK, LRCK, BICK, SDTI1-6/TDMI, SCL, SDA, PDN pins)	VIL	-	-	30% TVDD	V
High-Level Output Voltage (LRCK, BICK, SDTO1-3 pins: Iout=-100µA)	VOH	TVDD-0.5	-	-	V
Low-Level Output Voltage (LRCK, BICK, SDTO1-3 pins: Iout= 100µA)	VOL		-	0.5	V
(SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta=-40~+105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V; C_L=20pF; unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
External Clock					
256fsn:	fCLK	2.048		12.288	MHz
Pulse Width Low	tCLKL	32			ns
Pulse Width High	tCLKH	32			ns
384fsn:	fCLK	3.072		18.432	MHz
Pulse Width Low	tCLKL	22			ns
Pulse Width High	tCLKH	22			ns
512fsn:	fCLK	4.096		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
256fsd, 128fsq:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
LRCK Timing (Slave mode)					
Stereo mode					
(TDM1-0 bits = "00")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	45		55	%
TDM512 mode (Note 12)					
(TDM1-0 bits = "01")					
LRCK frequency	fsn	8		48	kHz
"H" time	tLRH	1/512fs			ns
"L" time	tLRL	1/512fs			ns
TDM256 mode (Note 13)					
(TDM1-0 bits = "10")					
LRCK frequency	fsn	8		48	kHz
	fsd	64		96	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM128 mode (Note 14)					
(TDM1-0 bits = "11")					
LRCK frequency	fsq	128		192	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns
LRCK Timing (Master Mode)					
Stereo mode					
(TDM1-0 bits = "00")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	-	50	-	%
TDM512 mode (Note 12)					
(TDM1-0 bits = "01")					
LRCK frequency	fsn	8		48	kHz
"H" time (Note 15)	tLRH		1/16fs		ns
TDM256 mode (Note 13)					
(TDM1-0 bits = "10")					
LRCK frequency	fsn	8		48	kHz
	fsd	64		96	kHz
"H" time (Note 15)	tLRH		1/8fs		ns

TDM128 mode (Note 14) **(TDM1-0 bits = "11")**						
LRCK frequency		fsq	128		192	kHz
"H" time	(Note 15)	tLRH		1/4fs		ns

Note 12. Please use for Normal Speed mode. Master clock should be input the 512fs in Master mode.
Note 13. Please use for Normal Speed mode, Double Speed mode. Master clock should be input the 256fs or 512fs in Master mode.
Note 14. Please use for Quad Speed mode. Master clock should be input the 128fs in Master mode.
Note 15. If the format is I^2S, it is "L" time.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Slave mode)						
Stereo mode (TDM1-0 bits = "00") **for Normal Speed mode**						
BICK Period		tBCK	324			ns
BICK Pulse Width Low		tBCKL	130			ns
Pulse Width High		tBCKH	130			ns
LRCK Edge to BICK "↑"	(Note 16)	tLRB	20			ns
BICK "↑" to LRCK Edge	(Note 16)	tBLR	20			ns
LRCK to SDTO(MSB) (Except I^2S mode)		tLRS			80	ns
BICK "↓" to SDTO		tBSD			80	ns
SDTI Hold Time		tSDH	50			ns
SDTI Setup Time		tSDS	50			ns
Stereo mode (TDM1-0 bits = "00") **for Double and Quad Speed mode**						
BICK Period		tBCK	81			ns
BICK Pulse Width Low		tBCKL	33			ns
Pulse Width High		tBCKH	33			ns
LRCK Edge to BICK "↑"	(Note 16)	tLRB	23			ns
BICK "↑" to LRCK Edge	(Note 16)	tBLR	23			ns
SDTI Hold Time		tSDH	10			ns
SDTI Setup Time		tSDS	10			ns
TDM512 mode (TDM1-0 bits = "01")						
(Note 12)						ns
BICK Period		tBCK	40			ns
BICK Pulse Width Low		tBCKL	16			ns
Pulse Width High		tBCKH	16			ns
LRCK Edge to BICK "↑"	(Note 16)	tLRB	10			ns
BICK "↑" to LRCK Edge	(Note 16)	tBLR	10			ns
SDTO Setup time BICK "↑"		tBSS	6			ns
SDTO Hold time BICK "↑"		tBSH	5			ns
SDTI/TDMI Hold Time		tSDH	5			ns
SDTI/TDMI Setup Time		tSDS	6			ns
TDM256 mode (TDM1-0 bits = "10")						
(Note 13)						ns
BICK Period		tBCK	40			ns
BICK Pulse Width Low		tBCKL	16			ns
Pulse Width High		tBCKH	16			ns
LRCK Edge to BICK "↑"	(Note 16)	tLRB	10			ns
BICK "↑" to LRCK Edge	(Note 16)	tBLR	10			ns
SDTO Setup time BICK "↑"		tBSS	6			ns
SDTO Hold time BICK "↑"		tBSH	5			ns
SDTI/TDMI Hold Time		tSDH	5			ns
SDTI/TDMI Setup Time		tSDS	6			ns

TDM128 mode (TDM1-0 bits = "11") (Note 14)					
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 16)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 16)	tBLR	10			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Master mode)					
Stereo mode (TDM1-0 bits = "00") for Normal Speed mode					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–80	-	80	ns
BICK "↓" to SDTO	tBSD	–80	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Stereo mode (TDM1-0 bits = "00") for Double and Quad Speed mode					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty (Note 17)	dBCK	-	50	-	%
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
TDM512 mode (TDM1-0 bits = "01") (Note 12)					
BICK Frequency	fBCK	-	512fs	-	Hz
BICK Duty (Note 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	-10		10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI/TDMI Hold Time	tSDH	5	-	-	ns
SDTI/TDMI Setup Time	tSDS	6	-	-	ns
TDM256 mode (TDM1-0 bits = "10") (Note 13)					
BICK Frequency	fBCK	-	256fs	-	Hz
BICK Duty (Note 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	--	ns
SDTI/TDMI Hold Time	tSDH	5	-	-	ns
SDTI/TDMI Setup Time	tSDS	6	-		ns
TDM128 mode (TDM1-0 bits = "11") (Note 14)					
BICK Frequency	fBCK	-	128fs	-	Hz
BICK Duty (Note 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns

Note 16. BICK rising edge must not occur at the same time as LRCK edge.
Note 17. The case that duty of MCLK is 50%.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 18)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 19)	tPD	150			ns
PDN "↑" to SDTO valid (Note 20)	tPDV		32768/MCLK +1059/fs		1/fs

Note 18. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 19. The AK4618 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 150ns for a certain reset. The AK4618 is not reset by the "L" pulse less than 30ns.

Note 20. These cycles are the numbers of MCLK and LRCK rising from the PDN pin rising.

Note 21. I^2C-bus is a trademark of NXP B.V.

■ Timing Diagram

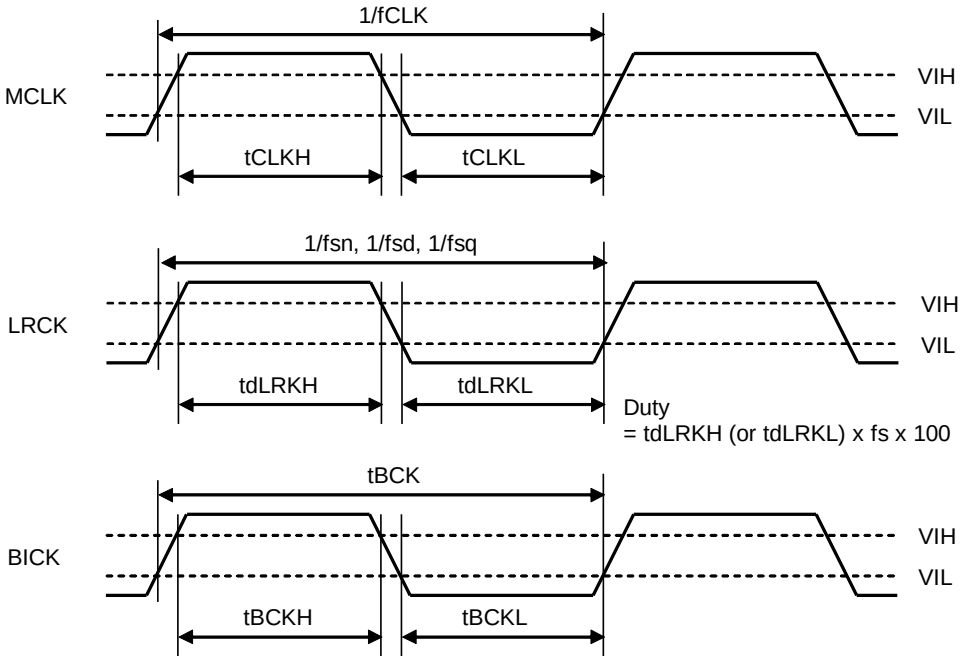


Figure 2. Clock Timing (TDM1-0 bits = "00" & Slave mode)

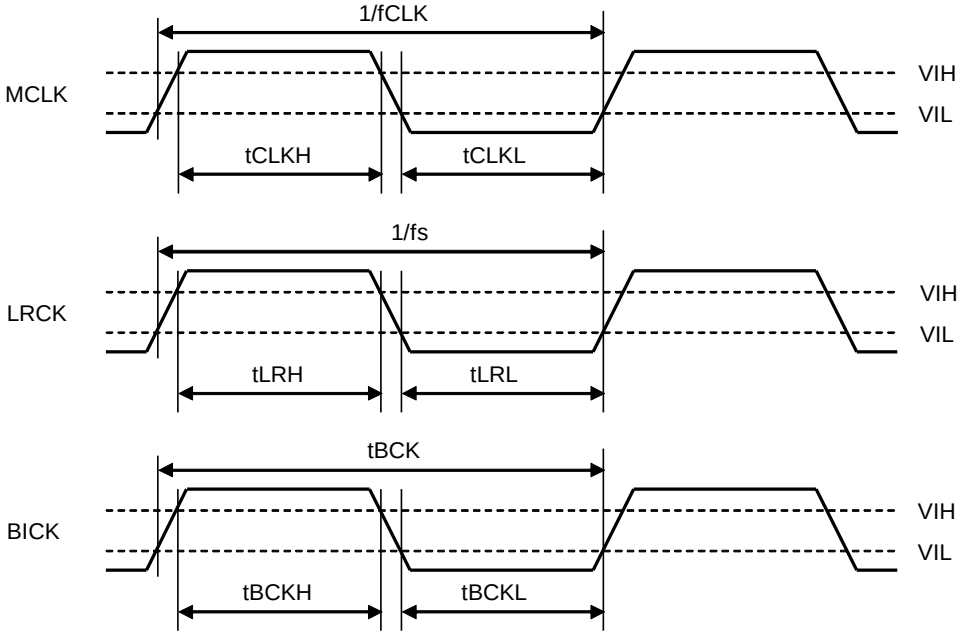


Figure 3. Clock Timing (Except TDM1-0 bits = "00" & Slave mode)

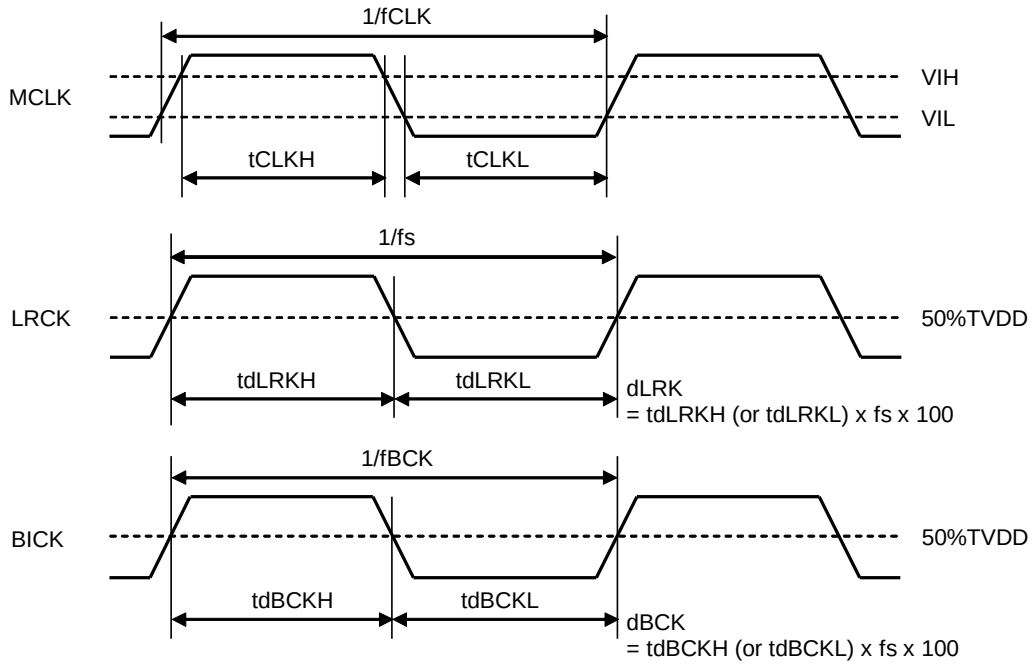


Figure 4. Clock Timing (TDM1-0 bits = "00" & Master mode)

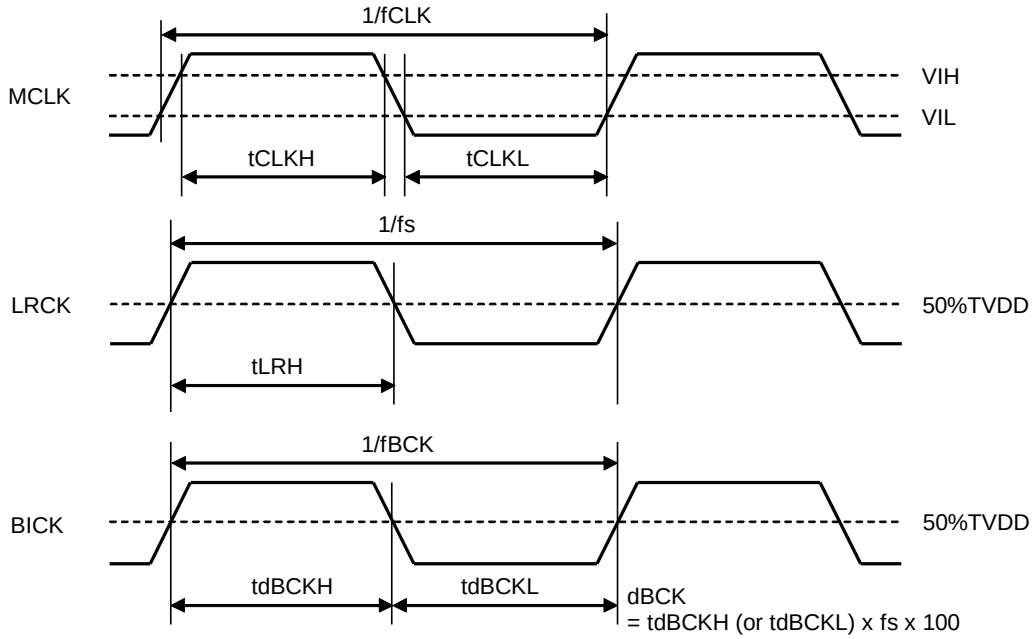


Figure 5. Clock Timing (Except TDM1-0 bits = "00" & Master mode)

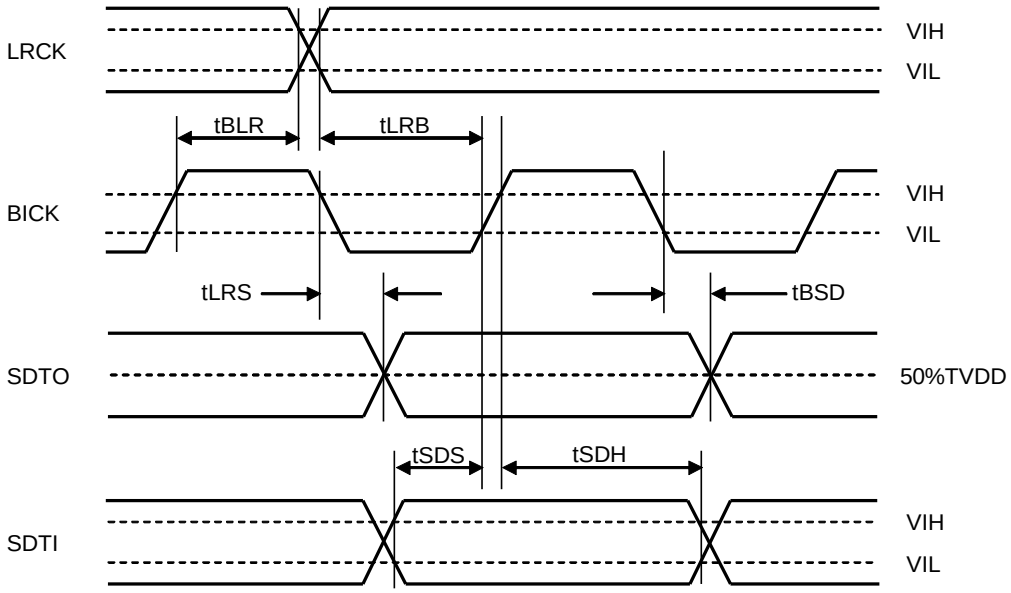


Figure 6. Audio Interface Timing (TDM1-0 bits = "00" & Slave mode)

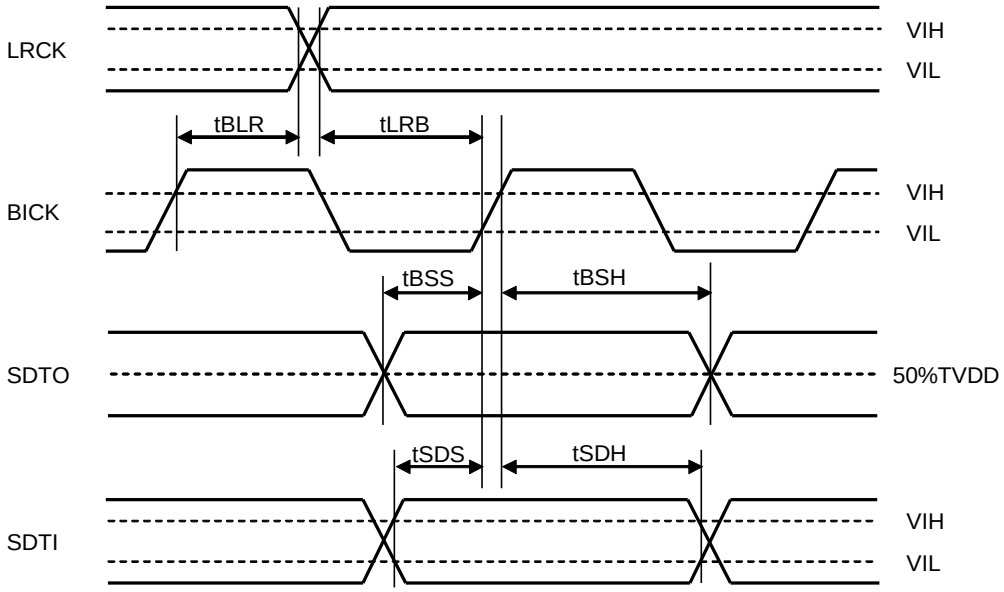


Figure 7. Audio Interface Timing (Except TDM1-0 bits = "00" & Slave mode)

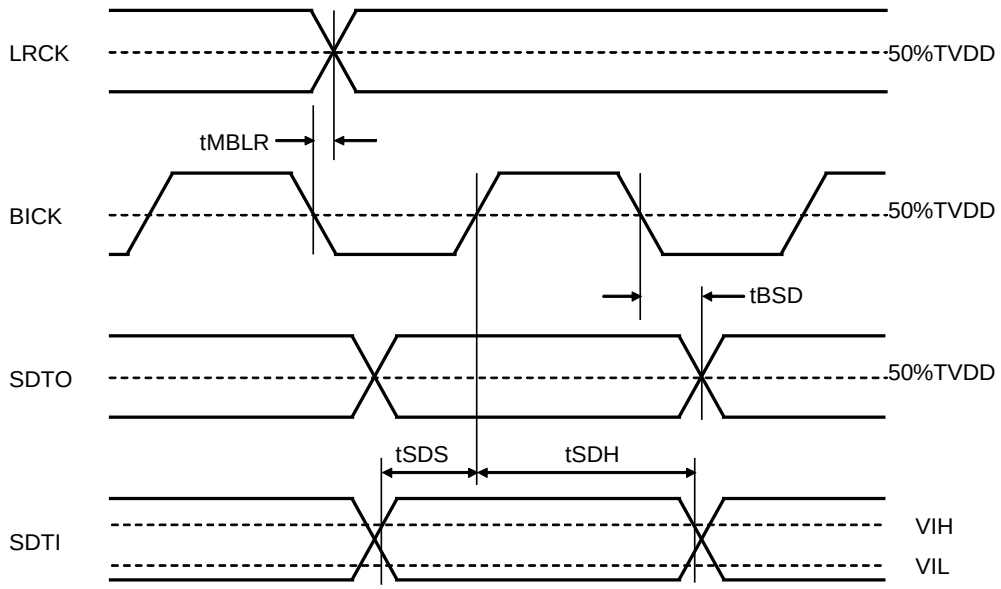


Figure 8. Audio Interface Timing (TDM1-0 bits = "00" & Master mode)

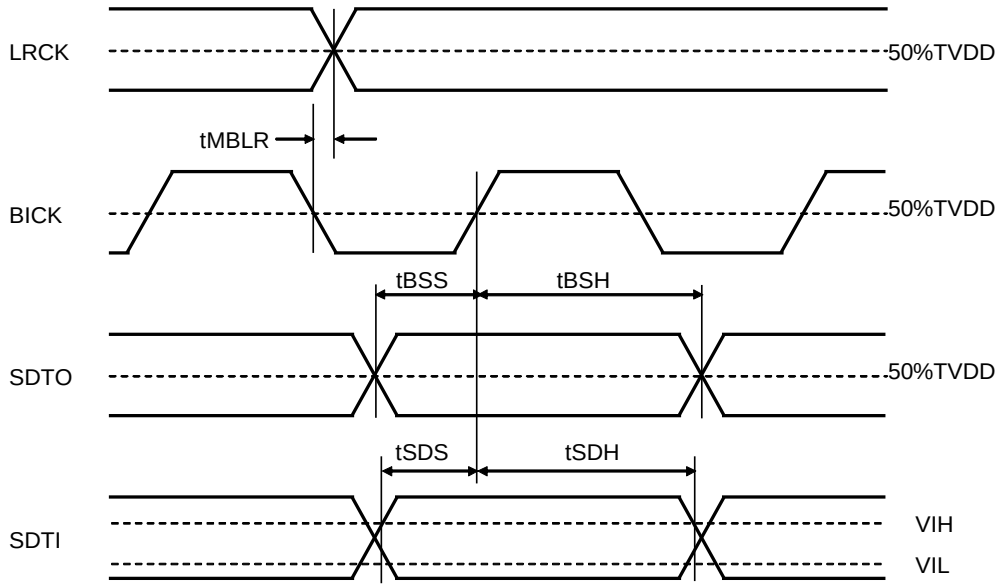


Figure 9. Audio Interface Timing (Except TDM1-0 bits = "00" & Master mode)

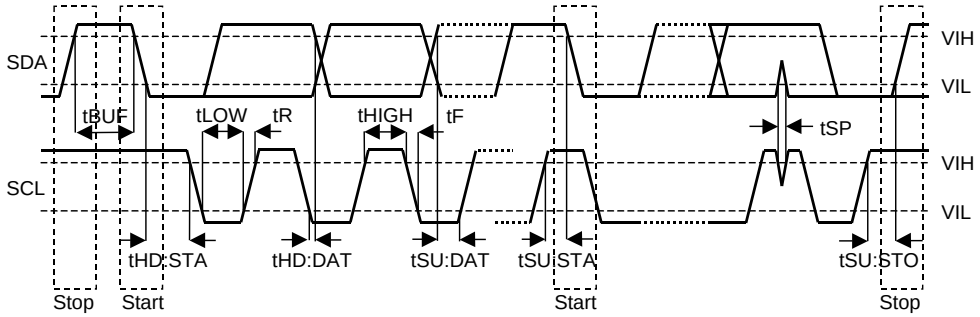


Figure 10. I^{2}C Bus mode Timing

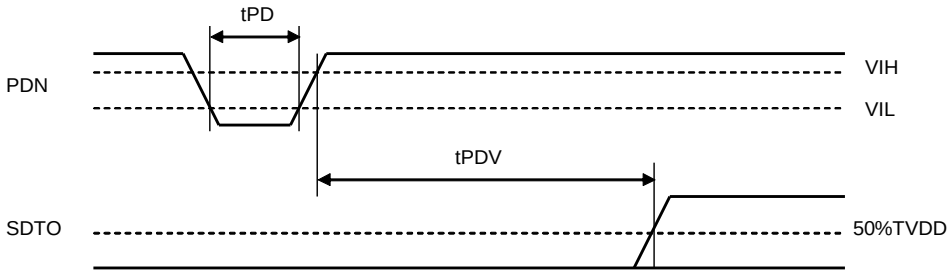


Figure 11. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks which are required to operate the AK4618 in slave mode are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK but the phase is not critical. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit= "0": Default), the sampling speed is set by DFS0, DFS1 (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 3, Table 4, Table 5). In Auto Setting Mode (ACKS bit= "1"), as MCLK frequency is detected automatically (Table 6) and the internal master clock attains the appropriate frequency (Table 7), so it is not necessary to set DFS.

In master mode, only MCLK is required. Master Clock Input Frequency should be set with the CKS1-0 bits, and the sampling speed should be set by the DFS1-0 bits. The frequencies and the duties of the clocks (LRCK, BICK) are not stabile immediately after setting CKS1-0 bits and DFS1-0 bits up.

After exiting reset at power-up in slave mode, the AK4618 is in power-down mode until MCLK and LRCK are input.

If the clock is stopped, click noise occurs when restarting the clock. Mute the digital output externally if the click noise influences system applications.

Note: ADC is automatically powered-down in Doble Speed Mode and Quad Speed Mode.

DFS1	DFS0	Sampling Speed Mode (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	(default)
0	1	Double Speed Mode	64kHz~96kHz	
1	0	Quad Speed Mode	128kHz~192kHz	
1	1	N/A	-	

(N/A: Not available)

Table 1. Sampling Speed (Manual Setting Mode)

CKS1	CKS0	Normal Speed Mode	Double Speed Mode	Quad Speed Mode	
0	0	256fs	256fs	128fs	
0	1	384fs	256fs	128fs	
1	0	512fs	256fs	128fs	(default)
1	1	512fs	256fs	128fs	

Table 2. Master Clock Input Frequency Select (Master Mode)
Note: In Normal Speed Mode, TDM mode (TDM1-0 bits ="01) can be used when CKS1 bit = "1".

LRCK	MCLK (MHz)			BICK (MHz)
fs	256fs	384fs	512fs	64fs
32.0kHz	8.1920	12.2880	16.3840	2.0480
44.1kHz	11.2896	16.9344	22.5792	2.8224
48.0kHz	12.2880	18.4320	24.5760	3.0720

Table 3. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)	BICK (MHz)
fs	256fs	64fs
88.2kHz	22.5792	5.6448
96.0kHz	24.5760	6.1440

Table 4. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)	BICK (MHz)
fs	128fs	64fs
176.4kHz	22.5792	11.2896
192.0kHz	24.5760	12.2880

Table 5. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK	Sampling Speed Mode
512fs	Normal Speed Mode
256fs	Double Speed Mode
128fs	Quad Speed Mode

Table 6. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)			Sampling Speed Mode
fs	128fs	256fs	512fs	
32.0kHz	-	-	16.3840	Normal Speed Mode
44.1kHz	-	-	22.5792	
48.0kHz	-	-	24.5760	
88.2kHz	-	22.5792	-	Double Speed Mode
96.0kHz	-	24.5760	-	
176.4kHz	22.5792	-	-	Quad Speed Mode
192.0kHz	24.5760	-	-	

Table 7. System Clock Example (Auto Setting Mode)

■ De-emphasis Filter

The AK4618 has a digital de-emphasis filter (tc=50/15μs) by an IIR filter. The de-emphasis filter supports only Normal Speed Mode. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis of each DAC can be set individually by registers, DAC1(SDTI1), DAC2(SDTI2), DAC3(SDTI3), DAC4(SDTI4), DAC5(SDTI5), DAC6(SDTI6).

Mode	Sampling Speed Mode	DEM11 (DEM61-21)	DEM10 (DEM60-20)	DEM	
0	Normal Speed Mode	0	0	44.1kHz	
1	Normal Speed Mode	0	1	OFF	(default)
2	Normal Speed Mode	1	0	48kHz	
3	Normal Speed Mode	1	1	32kHz	

Table 8. De-emphasis Control

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 3.7Hz at fs=48kHz and scales with the sampling rate (fs).

■ Master Mode and Slave Mode

Master Mode and Slave Mode are selected by setting the MS bit.
LRCK and BICK pins are outputs in Master Mode (MS bit= “1”)
LRCK and BICK pins are inputs in Slave Mode (MS bit= “0”)

The BICK and LRCK pins are in Hi-z state before an internal power up and MS bit = "1".
When a problem is occurred by this, pulldown BICK and LRCK pins by external resistance(ex. 100kohm).

PDN	MS bit	LRCK pin	BICK pin
L	0	Input	Input
	1	Hi-z	Hi-z
H	0	Input	Input
	1	Output	Output

Table 9. LRCK and BICK pins

■ Audio Serial Interface Format

(1) Stereo Mode

When TDM1-0 bits = "00", ten modes can be selected by the DIF2-0 bits as shown in Table 10. In all modes the serial data is MSB-first, 2's compliment format. The data SDTO is clocked out on the falling edge of BICK and the SDTI1-6 is latched on the rising edge of BICK.

Mode3/4/8/9/13/14/18/19/23/24/28/29/33/34/38/39 in SDTI input formats can be used for 16-20bit data by zeroing the unused LSBs.

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO1-3	SDTI1-6	LRCK		BICK		
										I/O		I/O	
0	0	0	0	0	0	0	24bit, Left justified (*)	16bit, Right justified	H/L	I	≥32fs 64fs≥	I	
1	0	0	0	0	0	1	24bit, Left justified	20bit, Right justified	H/L	I	≥48fs 64fs≥	I	
2	0	0	0	0	1	0	24bit, Left justified	24bit, Right justified	H/L	I	≥48fs 64fs≥	I	
3	0	0	0	0	1	1	24bit, Left justified	24bit, Left justified	H/L	I	≥48fs 64fs≥	I	
4	0	0	0	1	0	0	24bit, I^2S	24bit, I^2S	L/H	I	≥48fs 64fs≥	I	(default)
5	1	0	0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
6	1	0	0	0	0	1	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
7	1	0	0	0	1	0	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
8	1	0	0	0	1	1	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	
9	1	0	0	1	0	0	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	

Table 10. Audio Data Formats (Stereo mode)

(*)When the BICK is less than 48fs, the output data length from SDTO is limited to the clock number of BICK in the half LRCK period.

(2) TDM Mode

The audio serial interface format is set in TDM mode by the TDM1-0 bits = "01". Five modes can be selected by the DIF2-0 bits as shown in Table 11. In all modes the serial data is MSB-first, 2's compliment format. The SDTO is clocked out on the rising edge of BICK and the SDTI1/2/3 are latched on the rising edge of BICK.
TDM512 mode can be set by TDM1-0 bits as show in Table 11. In the TDM512 mode (fs = 48kHz), the serial data of all ADC (six channels) is output to the SDTO1 pin, SDTO2/3 pin = "L". And the serial data of all DAC (twelve channels) is input to the SDTI1 pin. The input data to SDTI2-6 pins are ignored and the SDTI6 pin is used as the TDMI pin in TDM cascade Mode(Figure 32). BICK should be fixed to 512fs. "H" time and "L" time of LRCK should be 1/512fs at least.
TDM256 mode can be set by TDM1-0 bits as show in Table 12. In the TDM256 mode (fs =48, 96kHz), the serial data of all ADC (six channels) is output to the SDTO1 pin, SDTO2/3 pin = "L". And the serial data of DAC (eight channels; L1, R1, L2, R2, L3, R3, L4, R4) is input to the SDTI1 pin. Other four data (L5, R5, L6, R6) are input to the SDTI2 pin. The input data to SDTI3-6 pins are ignored and the SDTI6 pin is used as the TDMI pin in TDM cascade Mode(Figure 32). BICK should be fixed to 256fs. "H" time and "L" time of LRCK should be 1/256fs at least. TDM128 mode can be set by TDM1-0 bits as show in Table 13.
TDM128 mode can be set by TDM1-0 bits as show in Table 13. In TDM128 mode (fs=192kHz), SDTO1/2/3 pin = "L". And the serial data of DAC (four channels; L1, R1, L2, R2) is input to the SDTI1 pin and the serial data of DAC (four channels; L3, R3, L4, R4) is input to the SDTI2 pin, the serial data of DAC (four channels; L5, R5, L6, R6) is input to the SDTI3 pin. The input data to SDTI4-6 pins are ignored. BICK should be fixed to 128fs. "H" time and "L" time of LRCK should be 1/128fs at least.

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO1	SDTI1	LRCK		BICK	
										I/O		I/O
10	0	0	1	0	0	0	24bit, Left justified	16bit, Right justified	↑	I	512fs	I
11	0	0	1	0	0	1	24bit, Left justified	20bit, Right justified	↑	I	512fs	I
12	0	0	1	0	1	0	24bit, Left justified	24bit, Right justified	↑	I	512fs	I
13	0	0	1	0	1	1	24bit, Left justified	24bit, Left justified	↑	I	512fs	I
14	0	0	1	1	0	0	24bit, I^2S	24bit, I^2S	↓	I	512fs	I
15	1	0	1	0	0	0	24bit, Left justified	16bit, Right justified	↑	O	512fs	O
16	1	0	1	0	0	1	24bit, Left justified	20bit, Right justified	↑	O	512fs	O
17	1	0	1	0	1	0	24bit, Left justified	24bit, Right justified	↑	O	512fs	O
18	1	0	1	0	1	1	24bit, Left justified	24bit, Left justified	↑	O	512fs	O
19	1	0	1	1	0	0	24bit, I^2S	24bit, I^2S	↓	O	512fs	O

Table 11. Audio Data Formats (TDM512 mode)

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO1	SDTI1-2	LRCK		BICK	
										I/O		I/O
20	0	1	0	0	0	0	24bit, Left justified	16bit, Right justified	↑	I	256fs	I
21	0	1	0	0	0	1	24bit, Left justified	20bit, Right justified	↑	I	256fs	I
22	0	1	0	0	1	0	24bit, Left justified	24bit, Right justified	↑	I	256fs	I
23	0	1	0	0	1	1	24bit, Left justified	24bit, Left justified	↑	I	256fs	I
24	0	1	0	1	0	0	24bit, I^2S	24bit, I^2S	↓	I	256fs	I
25	1	1	0	0	0	0	24bit, Left justified	16bit, Right justified	↑	O	256fs	O
26	1	1	0	0	0	1	24bit, Left justified	20bit, Right justified	↑	O	256fs	O
27	1	1	0	0	1	0	24bit, Left justified	24bit, Right justified	↑	O	256fs	O
28	1	1	0	0	1	1	24bit, Left justified	24bit, Left justified	↑	O	256fs	O
29	1	1	0	1	0	0	24bit, I^2S	24bit, I^2S	↓	O	256fs	O

Table 12. Audio Data Formats (TDM256 mode)

Mode	M/S	TDM1	TDM0	DIF2	DIF1	DIF0	SDTO1-3	SDTI1-3	LRCK		BICK	
										I/O		I/O
30	0	1	1	0	0	0	L	16bit, Right justified	↑	I	128fs	I
31	0	1	1	0	0	1	L	20bit, Right justified	↑	I	128fs	I
32	0	1	1	0	1	0	L	24bit, Right justified	↑	I	128fs	I
33	0	1	1	0	1	1	L	24bit, Left justified	↑	I	128fs	I
34	0	1	1	1	0	0	L	24bit, I^2S	↓	I	128fs	I
35	1	1	1	0	0	0	L	16bit, Right justified	↑	O	128fs	O
36	1	1	1	0	0	1	L	20bit, Right justified	↑	O	128fs	O
37	1	1	1	0	1	0	L	24bit, Right justified	↑	O	128fs	O
38	1	1	1	0	1	1	L	24bit, Left justified	↑	O	128fs	O
39	1	1	1	1	0	0	L	24bit, I^2S	↓	O	128fs	O

Table 13. Audio Data Formats (TDM128 mode)

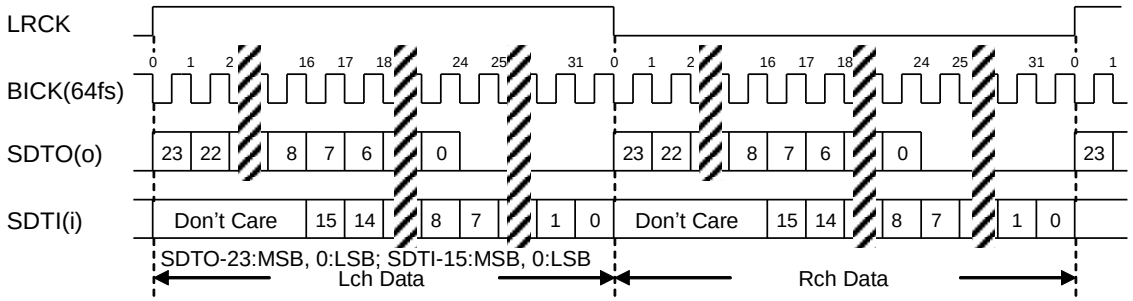


Figure 12. Mode 0/5 Timing (Stereo Mode)

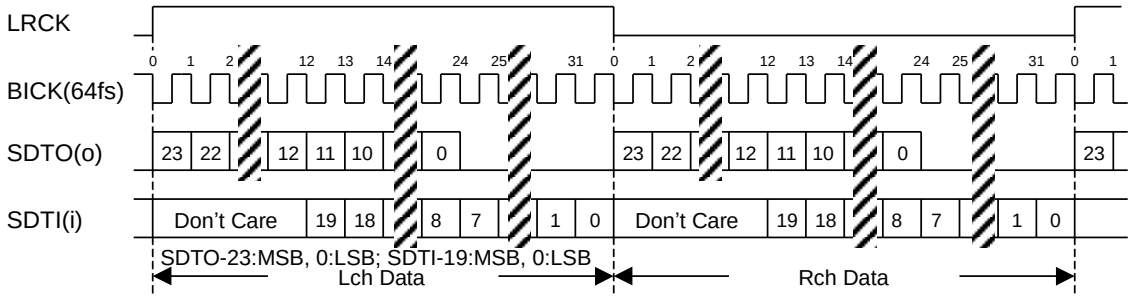


Figure 13. Mode 1/6 Timing (Stereo Mode)

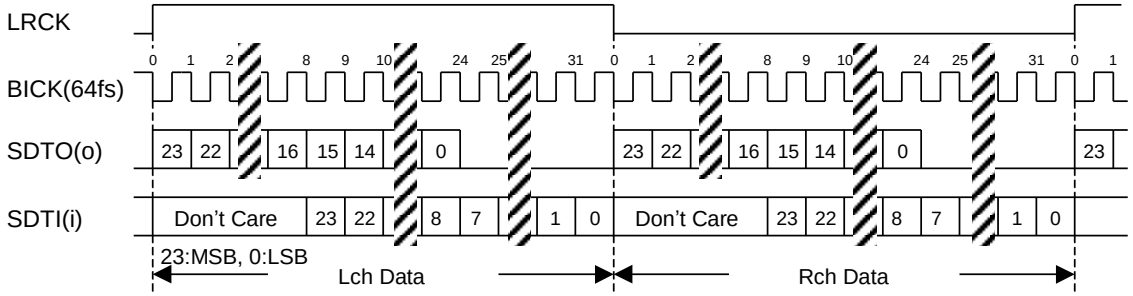


Figure 14. Mode 2/7 Timing (Stereo Mode)

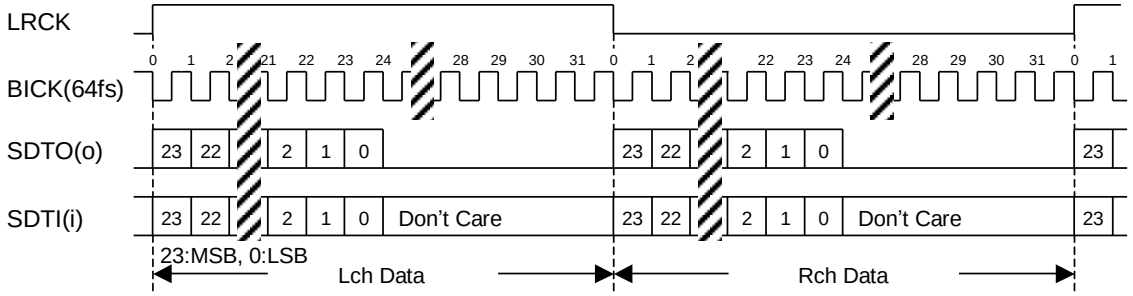


Figure 15. Mode 3/8 Timing (Stereo Mode)

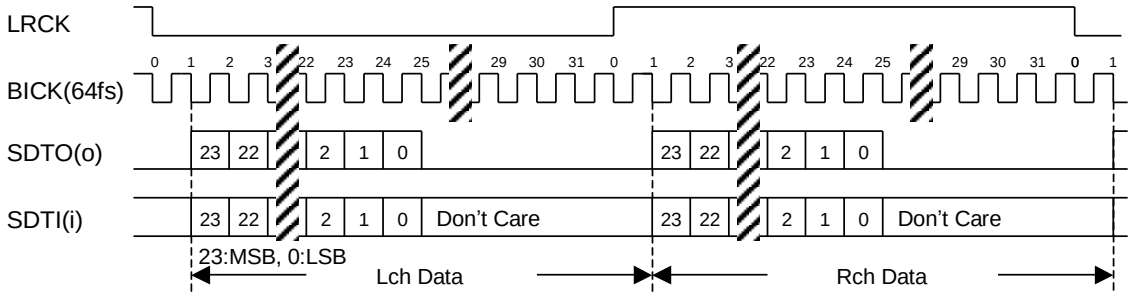
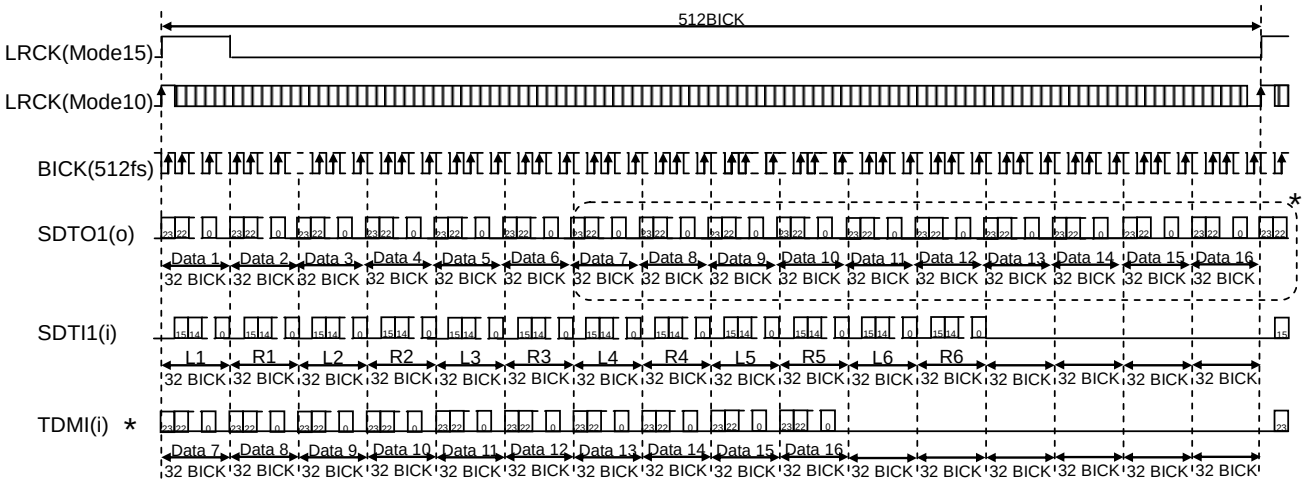
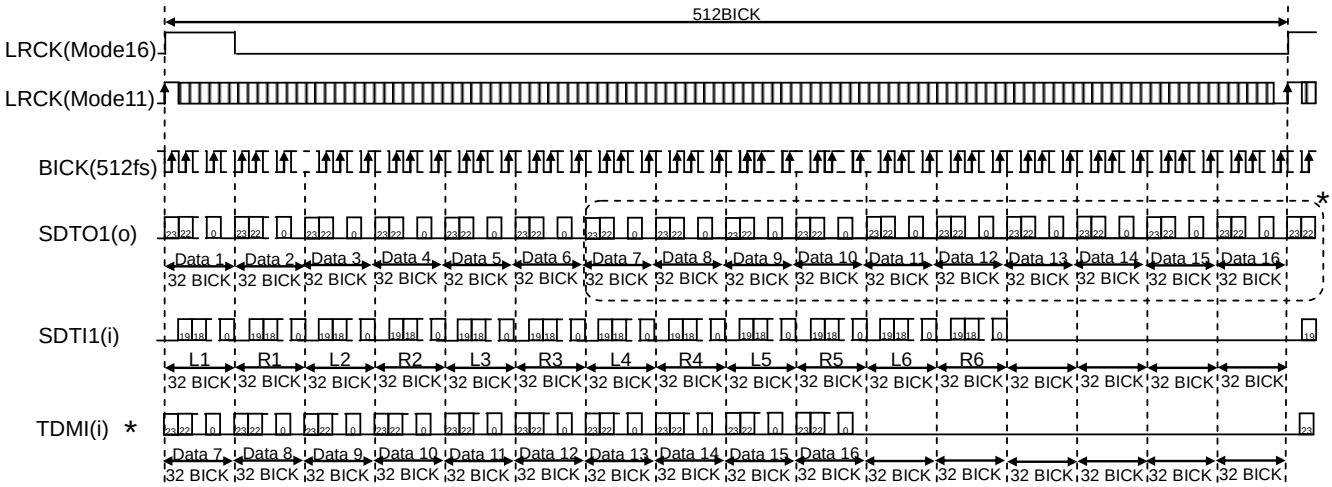


Figure 16. Mode 4/9 Timing (Stereo Mode)



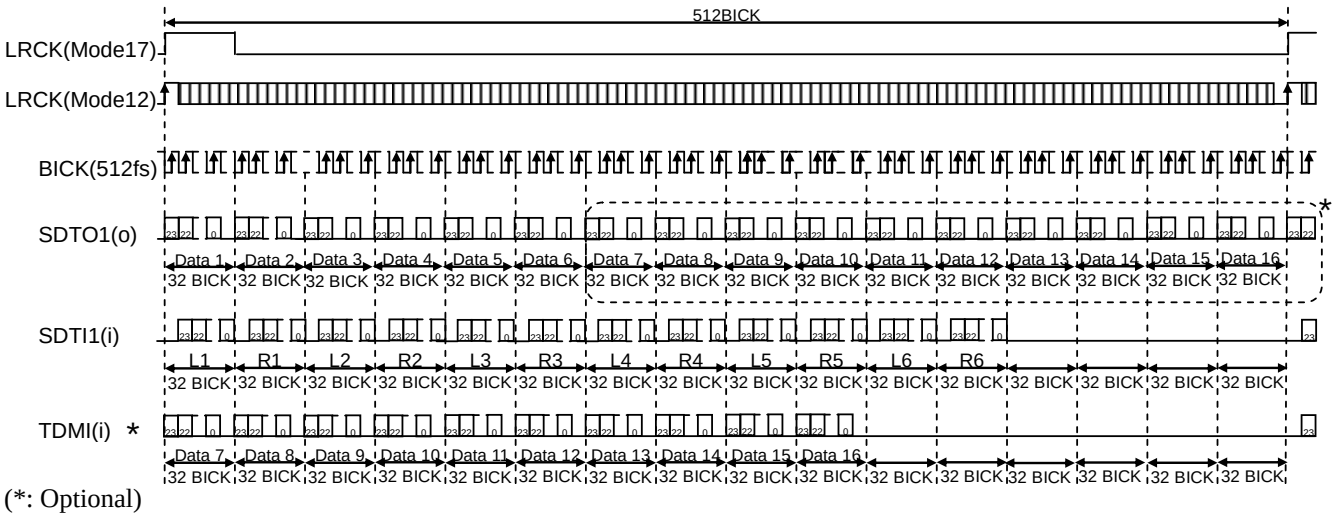
(*: Optional)

Figure 17. Mode 10/15 Timing (TDM512 Mode)



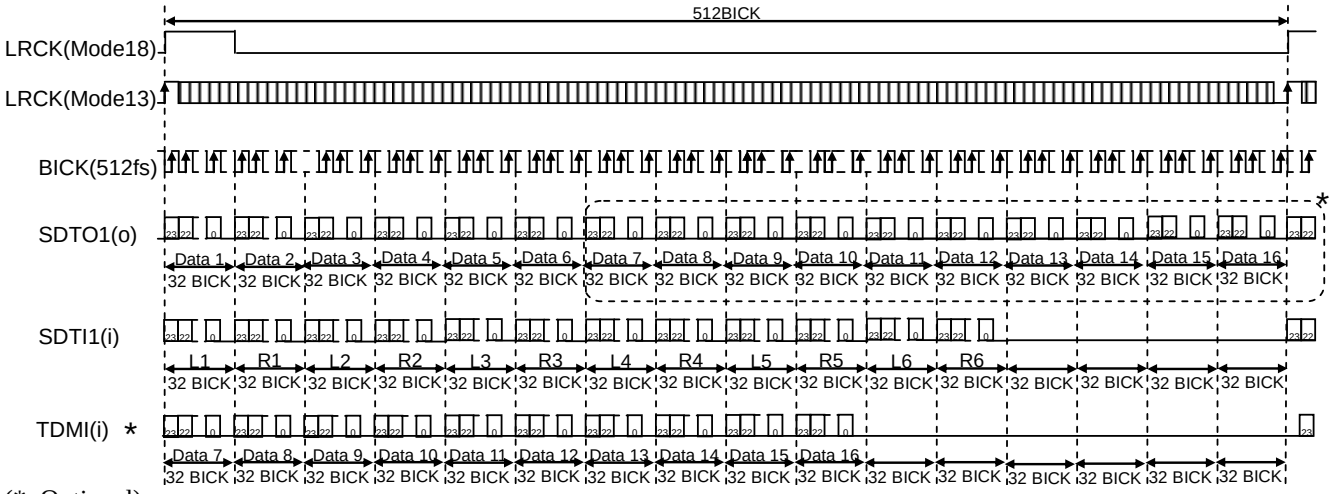
(*: Optional)

Figure 18. Mode 11/16 Timing (TDM512 Mode)



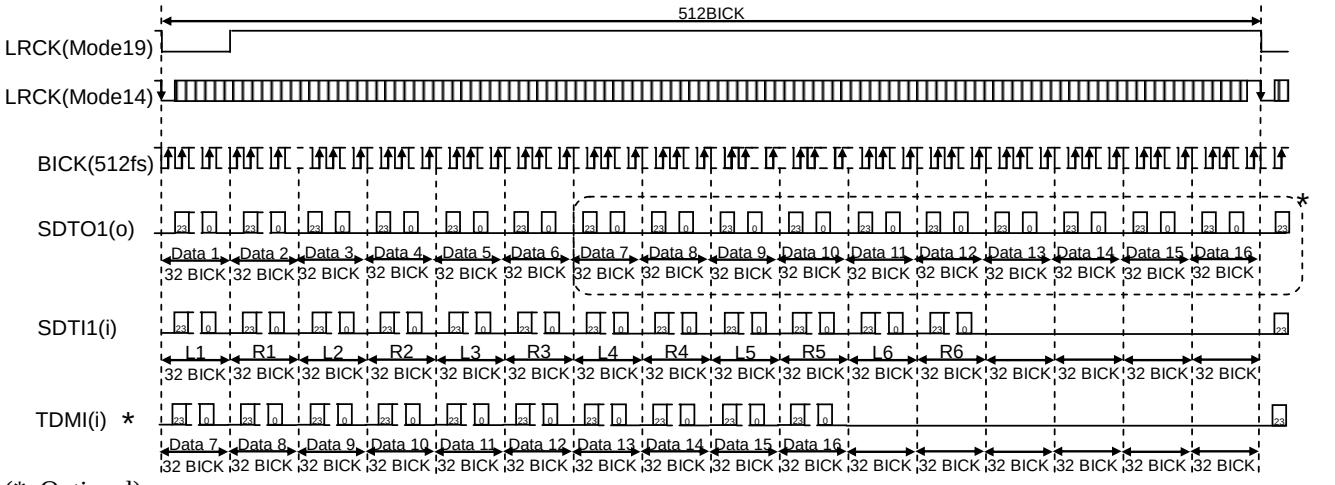
(*: Optional)

Figure 19. Mode 12/17 Timing (TDM512 Mode)



(*: Optional)

Figure 20. Mode 13/18 Timing (TDM512 Mode)



(*: Optional)

Figure 21. Mode 14/19 Timing (TDM512 Mode)

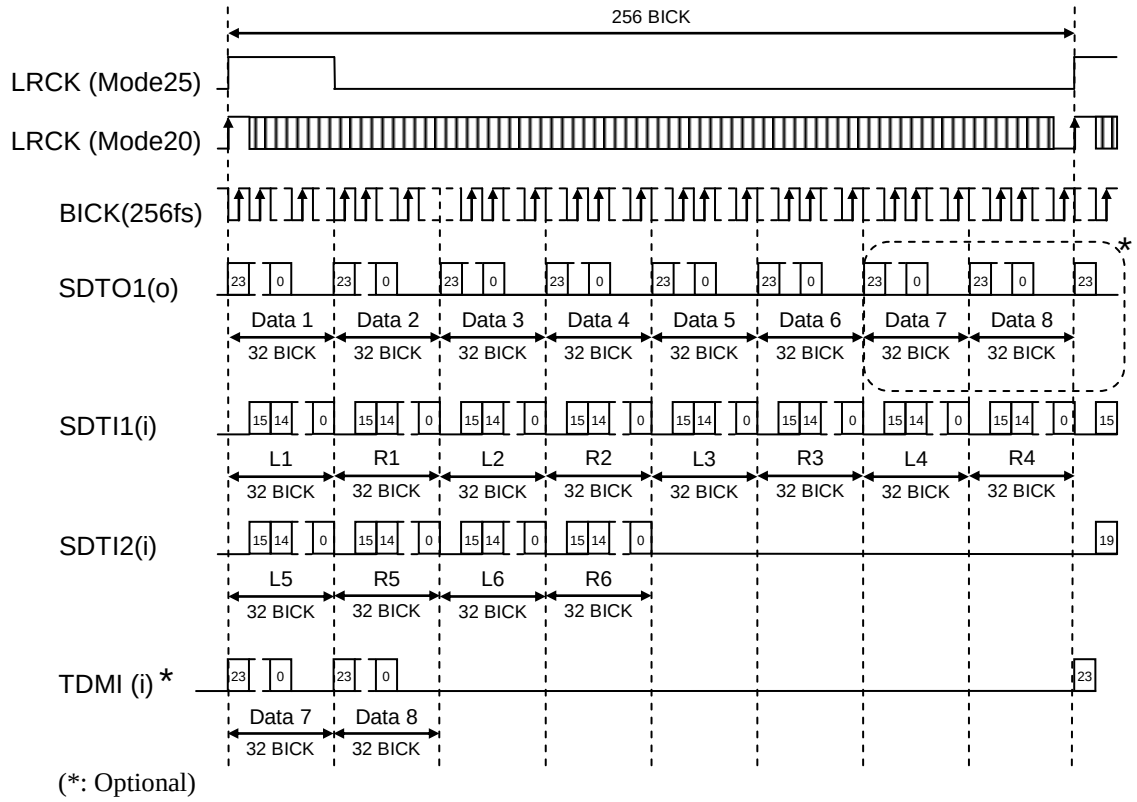


Figure 22. Mode 20/25 Timing (TDM256 Mode)

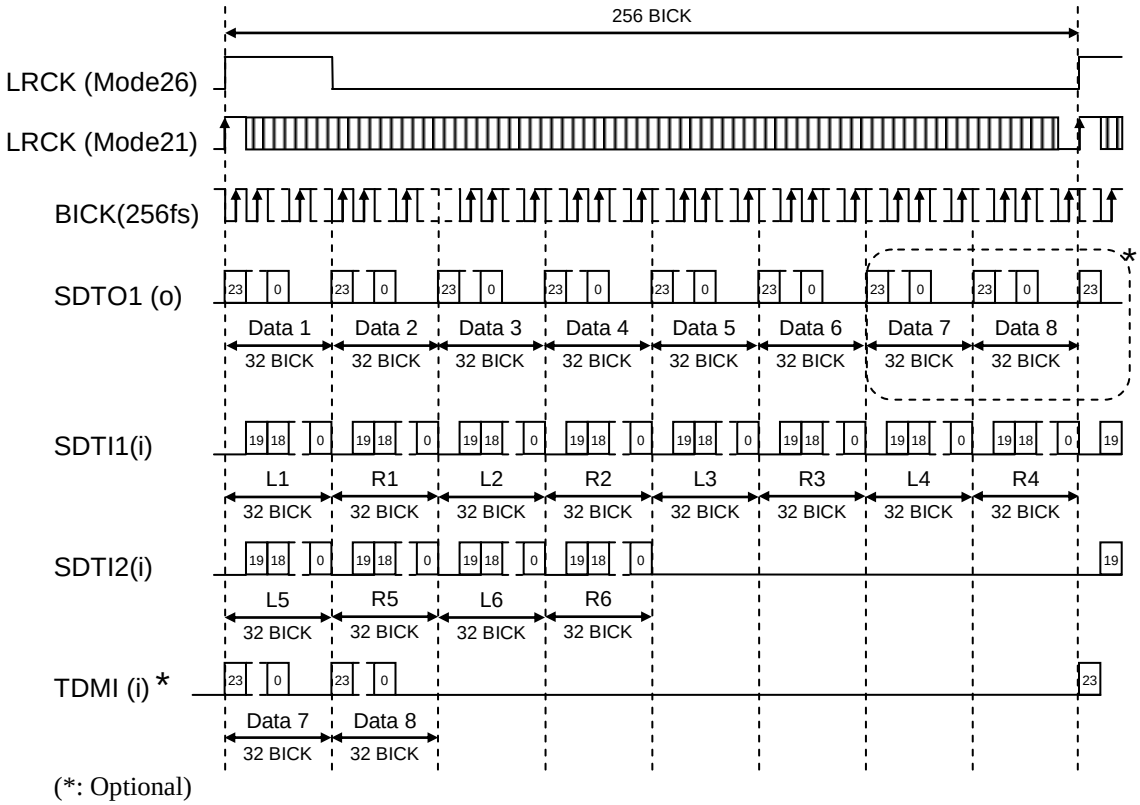
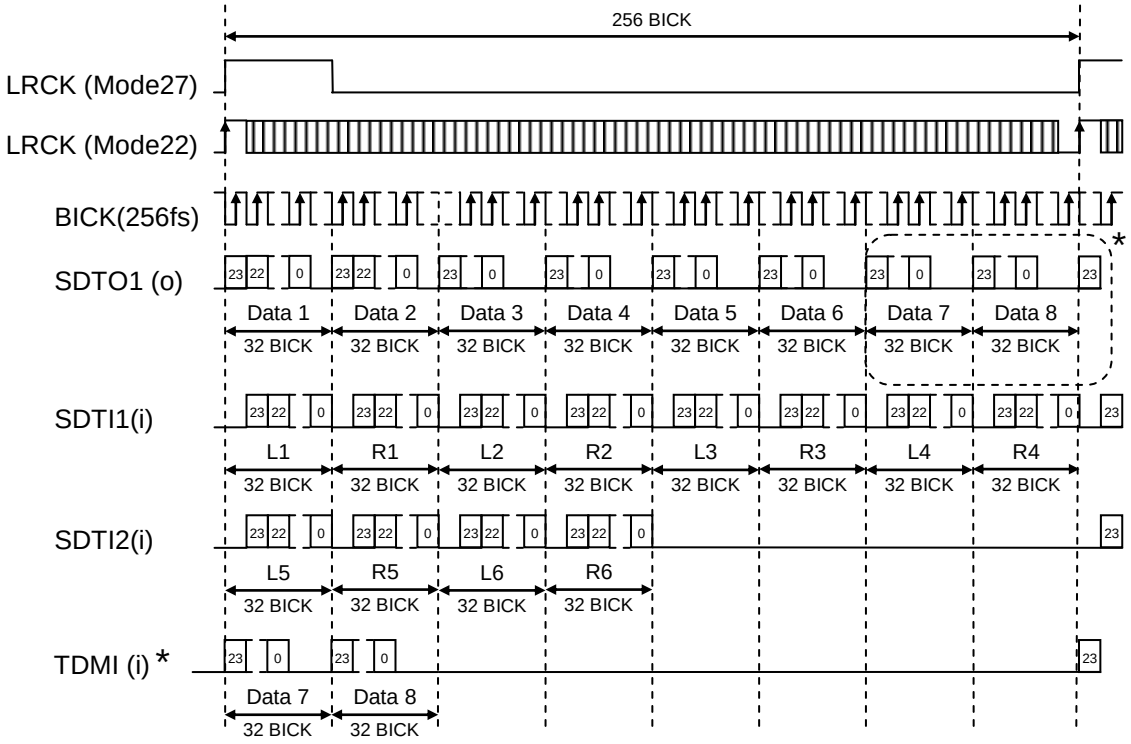
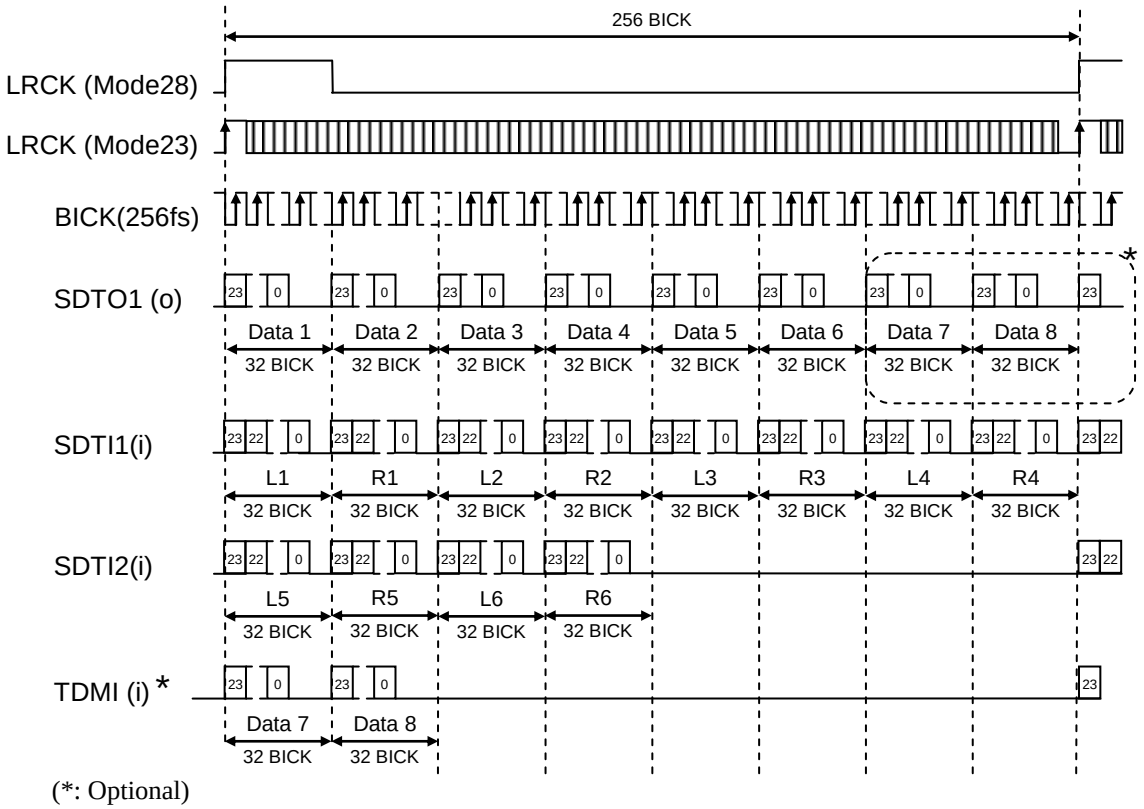


Figure 23. Mode 21/26 Timing (TDM256 Mode)



(*: Optional)

Figure 24. Mode 22/27 Timing (TDM256 Mode)



(*: Optional)

Figure 25. Mode 23/28 Timing (TDM256 Mode)

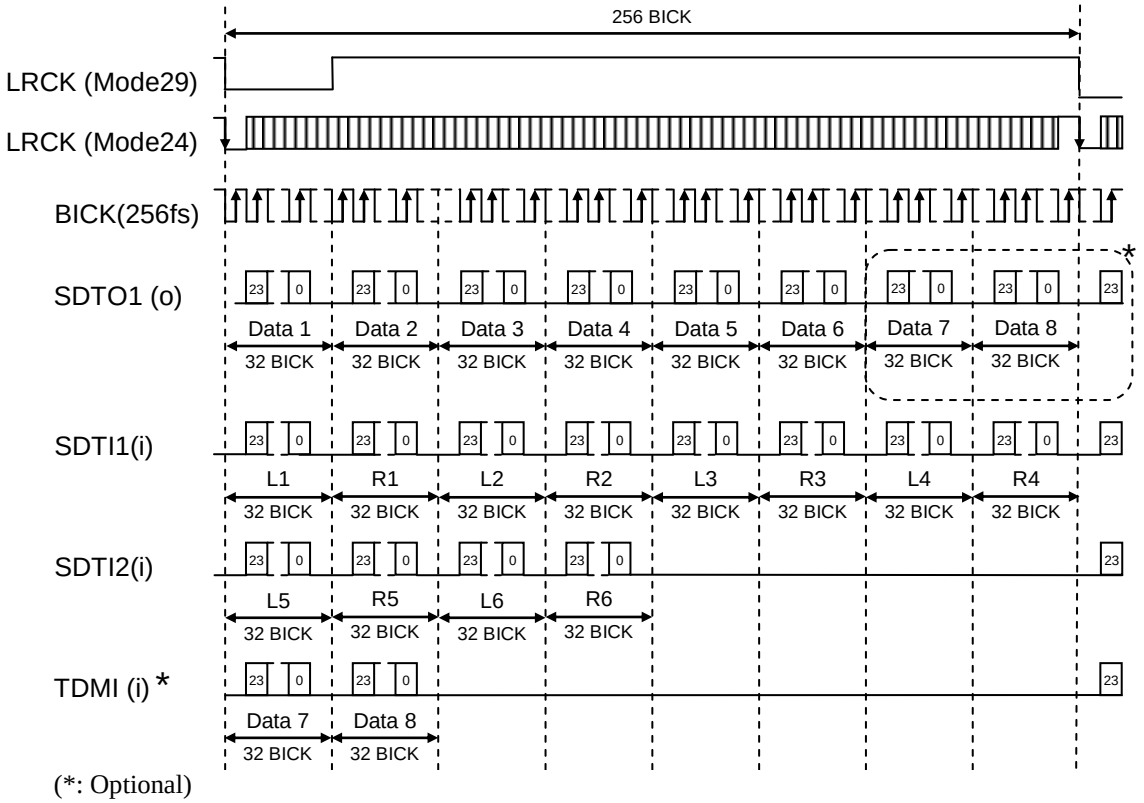


Figure 26. Mode 24/29 Timing (TDM256 Mode)

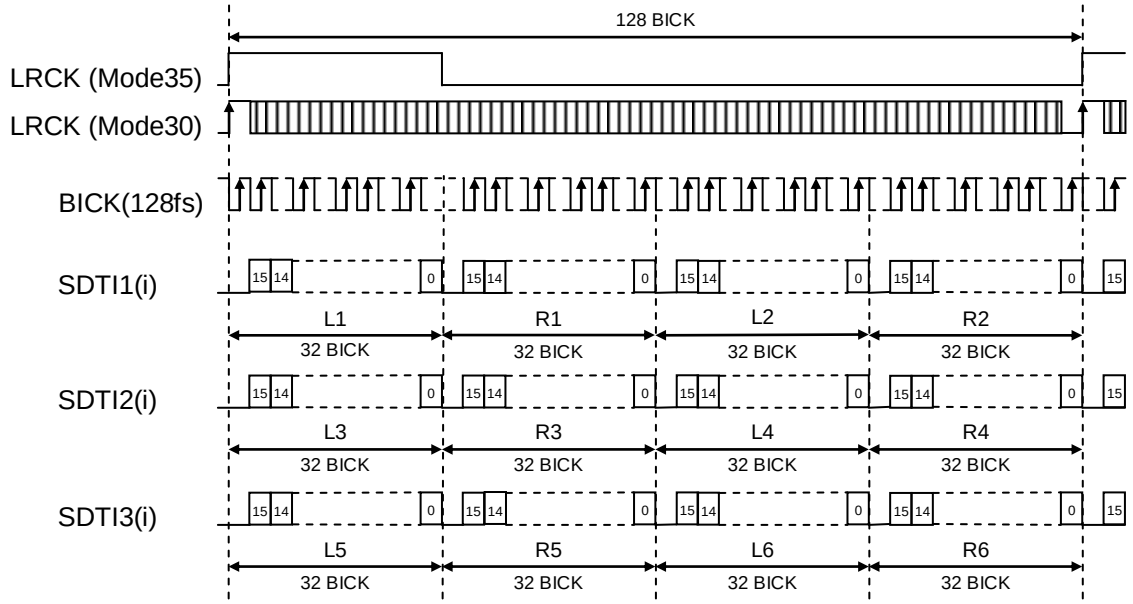


Figure 27. Mode 30/35 Timing (TDM128 Mode)

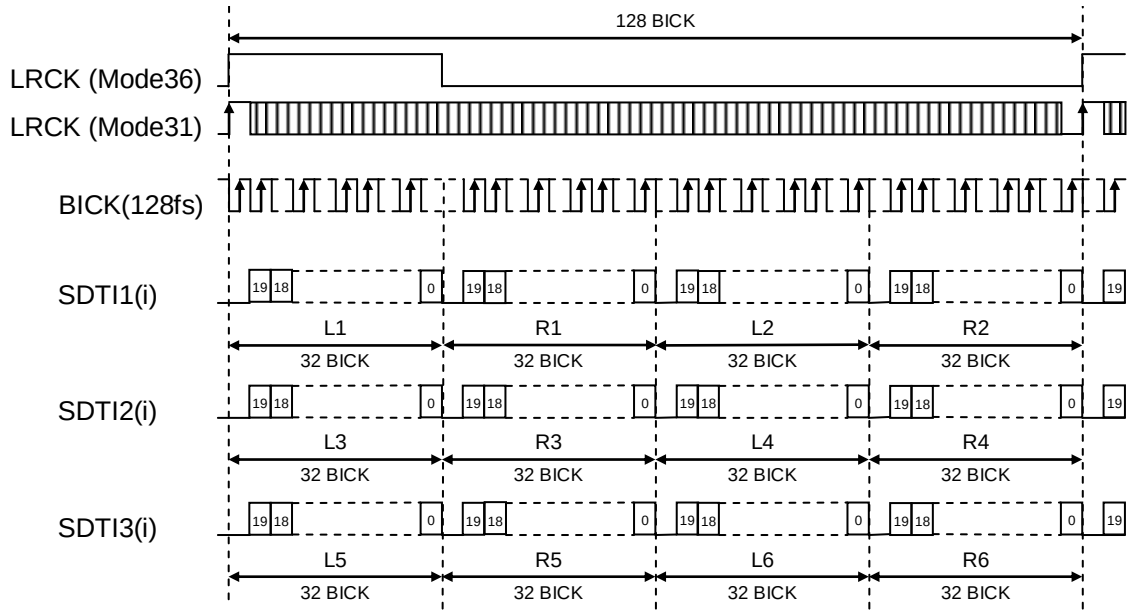


Figure 28. Mode 31/36 Timing (TDM128 Mode)

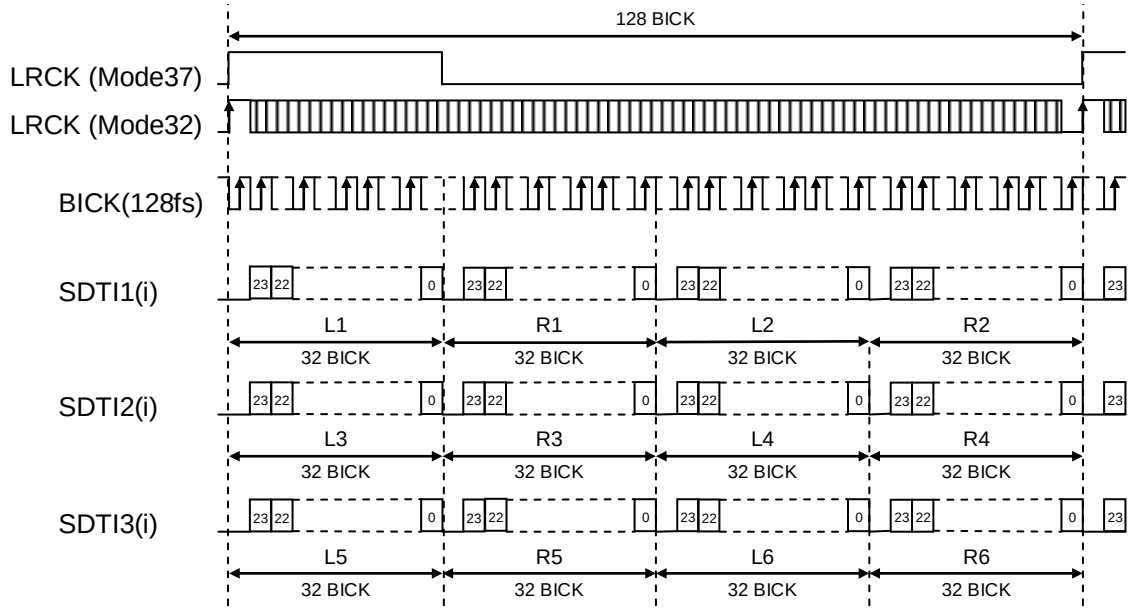


Figure 29. Mode 32/37 Timing (TDM128 Mode)

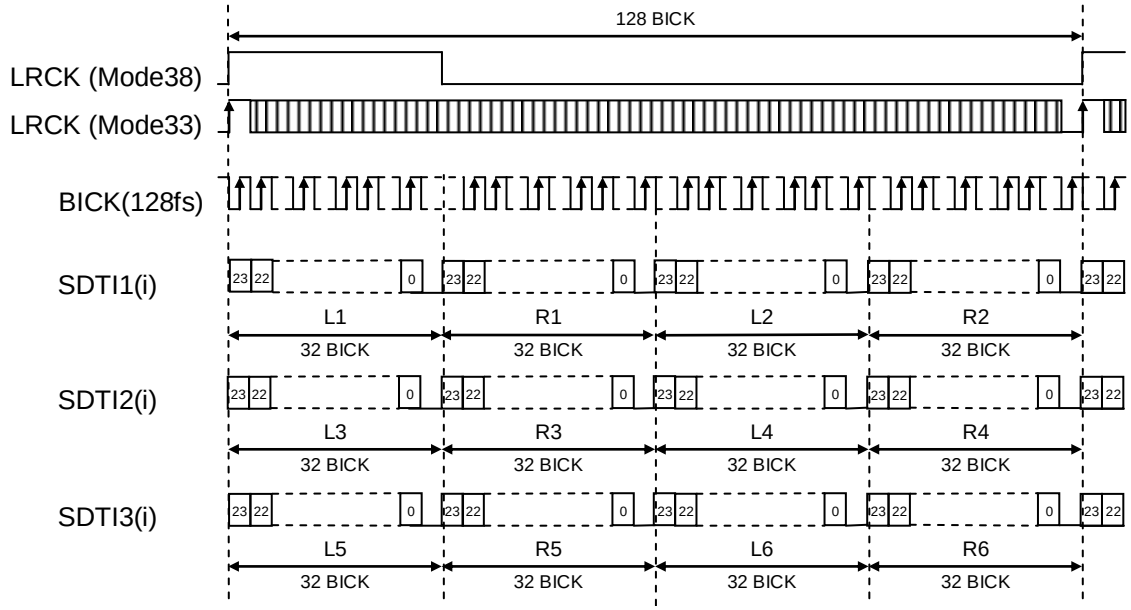


Figure 30. Mode 33/38 Timing (TDM128 Mode)

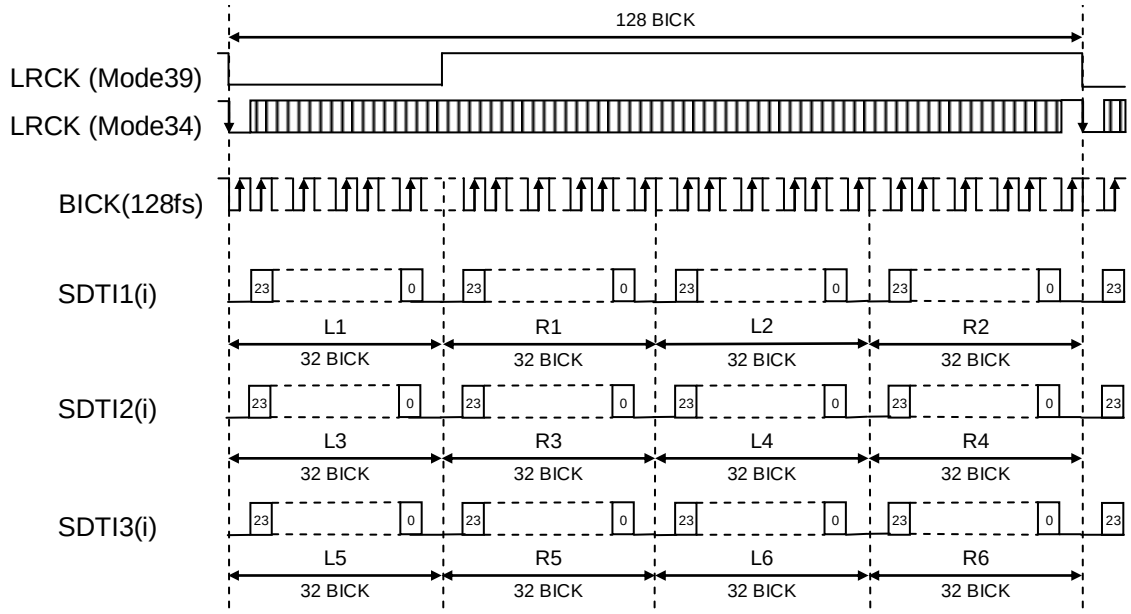


Figure 31. Mode 34/39 Timing (TDM128 Mode)

■ TDM Cascade Mode

The AK4618 can be connected with other ADCs or CODECs in cascades in TDM mode. In Figure 32, the SDTO pin of ADC or CODEC is connected with the TDMI pin of the AK4618. TDMI data is added after the 6channel ADC data of SDTO1.It is possible to output 8channel TDM data from the SDTO1 pin of the AK4618 as shown in Figure 22 ~ Figure 26 in TDM256 mode, and it is possible to output 16channel TDM data as shown Figure 17 ~ Figure 21 in TDM512 mode.

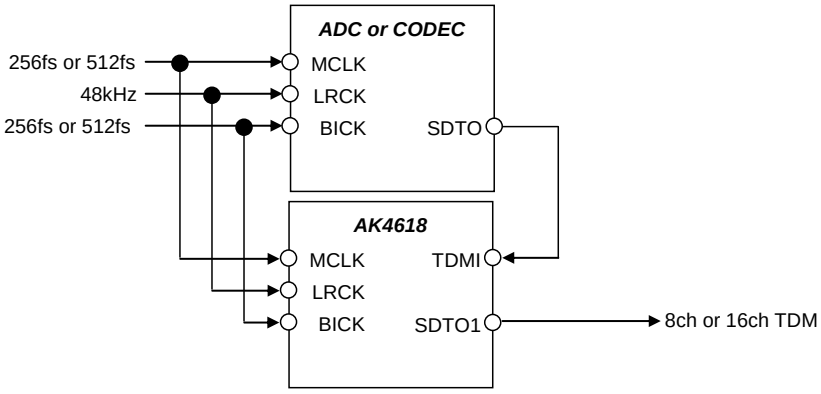


Figure 32. Cascade TDM Connection Diagram

■ Digital Attenuator

AK4618 has a channel-independent digital attenuator (256 levels, 0.5dB steps). Attenuation level of each DAC1-6 can be set by DAATL1/R1 7-0 bits, DAATL2/R2 7-0 bit, DAATL3/R3 7-0 bit, DAATL4/R4 7-0 bit, DAATL5/R5 7-0 bit, DAATL6/R6 7-0 bit, respectively (Table 14).

DAATL1/R1 7-0bits DAATL2/R2 7-0 bits DAATL3/R3 7-0 bits DAATL4/R4 7-0 bits DAATL5/R5 7-0 bits DAATL6/R6 7-0 bits	Attenuation Level	
00H	+0dB	(default)
01H	-0.5dB	
02H	-1.0dB	
:	:	
7DH	-62.5dB	
7EH	-63.0dB	
7FH	-63.5dB	
:	:	
FEH	-127.0dB	
FFH	MUTE (-∞)	

Table 14. Attenuation level of DAC Digital Attenuator

Transition time between set values of DAATL1/R1 7-0, DAATL2/R2 7-0, DAATL3/R3 7-0, DAATL4/R4 7-0, DAATL5/R5 7-0, DAATL6/R6 7-0 bits can be selected by the DAATS1-0 bits (Table 15). Transition between set values is the soft transition in Mode1/2/3 eliminating switching noise in the transition.

Mode	DAATS1	DAATS0	ATT speed	
0	0	0	4080/fs	(default)
1	0	1	2040/fs	
2	1	0	510/fs	
3	1	1	255/fs	

Table 15. Transition Time between Set Values of DAATL1/R1 7-0, DAATL2/R2 7-0, DAATL3/R3 7-0, DAATL4/R4 7-0, DAATL5/R5 7-0, DAATL6/R6 7-0 bits

The transition between set values is a soft transition of 4080 levels in mode 0. It takes 4080/fs (85ms@fs=48kHz) from 00H to FFH. If the PDN pin goes to “L”, DAATL1/R1 7-0, DAATL2/R2 7-0, DAATL3/R3 7-0, DAATL4/R4 7-0, DAATL5/R5 7-0, DAATL6/R6 7-0 bits are initialized to 00H. These bits are also set to 00H respectively when RSTN bit = “0”, and fade to their current value when RSTN bit returns to “1”.

■ MIC Gain Amplifier

The AK4618 has a gain amplifier which supports both single-ended and differential inputs. When MDIE 6-1bit is set to "1", differential inputs are supported by the IN6-1P IN6-1N, pins and the maximum input voltage is dependent on AVDD1. If the AVDD= 3.3V, the maximum input voltage for single-ended input is 2.67Vpp and ±2.67Vpp for differential inputs. The typical input impedance is 60kΩ (typ). MGAIN1 2-0, MGAIN2 2-0, MGAIN3 2-0, MGAIN4 2-0, MGAIN5 2-0, MGAIN6 2-0 bits control the input gain of the microphone amplifier (Table 16). A pop nose may occur if the input gain is changed during an operation.

Mode	MGAIN12 MGAIN22 MGAIN32 MGAIN42 MGAIN52 MGAIN62	MGAIN11 MGAIN21 MGAIN31 MGAIN41 MGAIN51 MGAIN61	MGAIN10 MGAIN20 MGAIN30 MGAIN40 MGAIN50 MGAIN60	Input Gain	
0	0	0	0	0dB	(default)
1	0	0	1	15dB	
2	0	1	0	18dB	
3	0	1	1	21dB	
4	1	0	0	24dB	
5	1	0	1	27dB	
6	1	1	0	30dB	
7	1	1	1	33dB	

Table 16. MIC Input Gain (typ.)

■ MIC Bias

The AK4618 integrates power supply for microphone. When PMMB bit = "1", the MICBIAS pin supplies power for the microphone. This output voltage is typically 2.40V and the load resistance is minimum 0.3 kΩ. (Figure 33, Figure 34)

Maximum interchannel isolation of microphone inputs is 70dB. The isolation depends on MICBIAS common impedance. The microphone impedance and the microphone bias resistance is 2k ohm and MIC-Amp input voltage is ±500mVpp (500mVpp). At this time, internal MICBIAS common impedance is 600m ohms or less, and external MICBIAS common impedance should be 200m ohms or less.

PMMB bit	MICBIAS pin	
0	Hi-Z	
1	Output	(default)

Table 17. MICBIAS pin

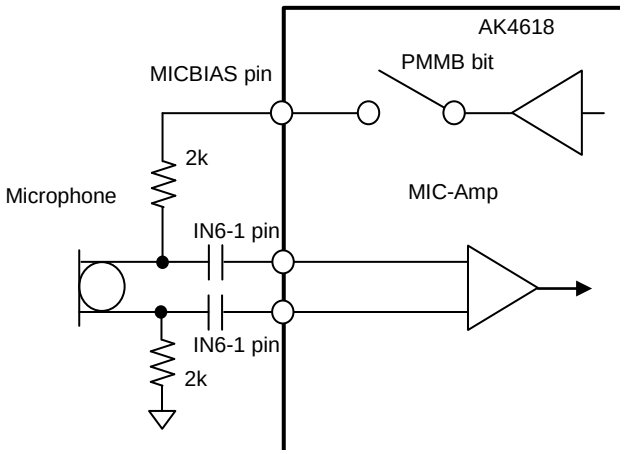


Figure 33. MIC Input Block Circuit (differential input)

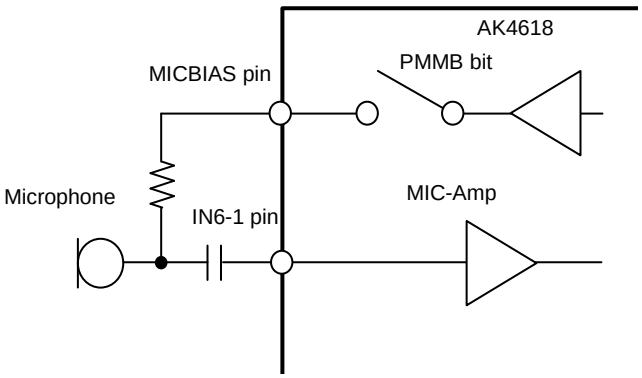
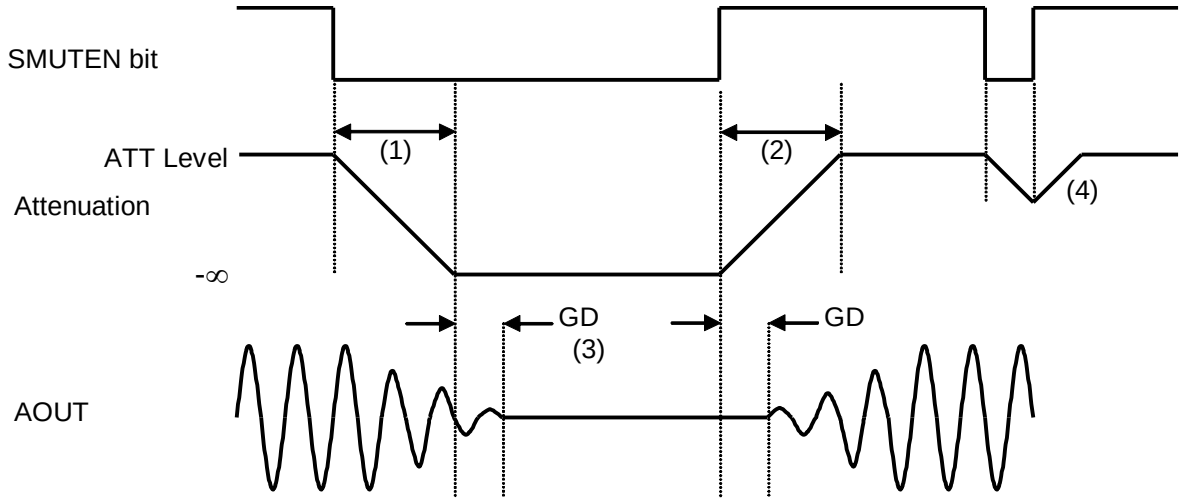


Figure 34. MIC Input Block Circuit (single-ended input)

■ Soft Mute Operation

Soft mute operation is performed in the digital domain. When the SMUTEN bit is set "0", the output signal is attenuated to -∞ in the cycle set by ATS bits (Table 15) from the current ATT level. When the SMUTEN bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level in the cycle set by ATS bits. If the soft mute is cancelled before attenuating to -∞ after starting the operation, attenuation is discontinued and it is returned to ATT level by the same cycle. Soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) The time for input data attenuation to -∞ (Table 15). For example, this time is 4080LRCK cycles (4080/fs) at ATT_DATA=00H. ATT transition of the soft-mute is from 00H to FFH

(2) The time for input data recovery to ATT level (Table 15). For example, this time is 4080LRCK cycles (4080/fs) at ATT-DATA=FFH. ATT transition of soft-mute is from FFH to 00H.

(3) The analog output corresponding to the digital input has group delay, GD.

(4) If the soft mute is cancelled before attenuating to -∞, the attenuation is discontinued and returned to ATT level by the same cycle.

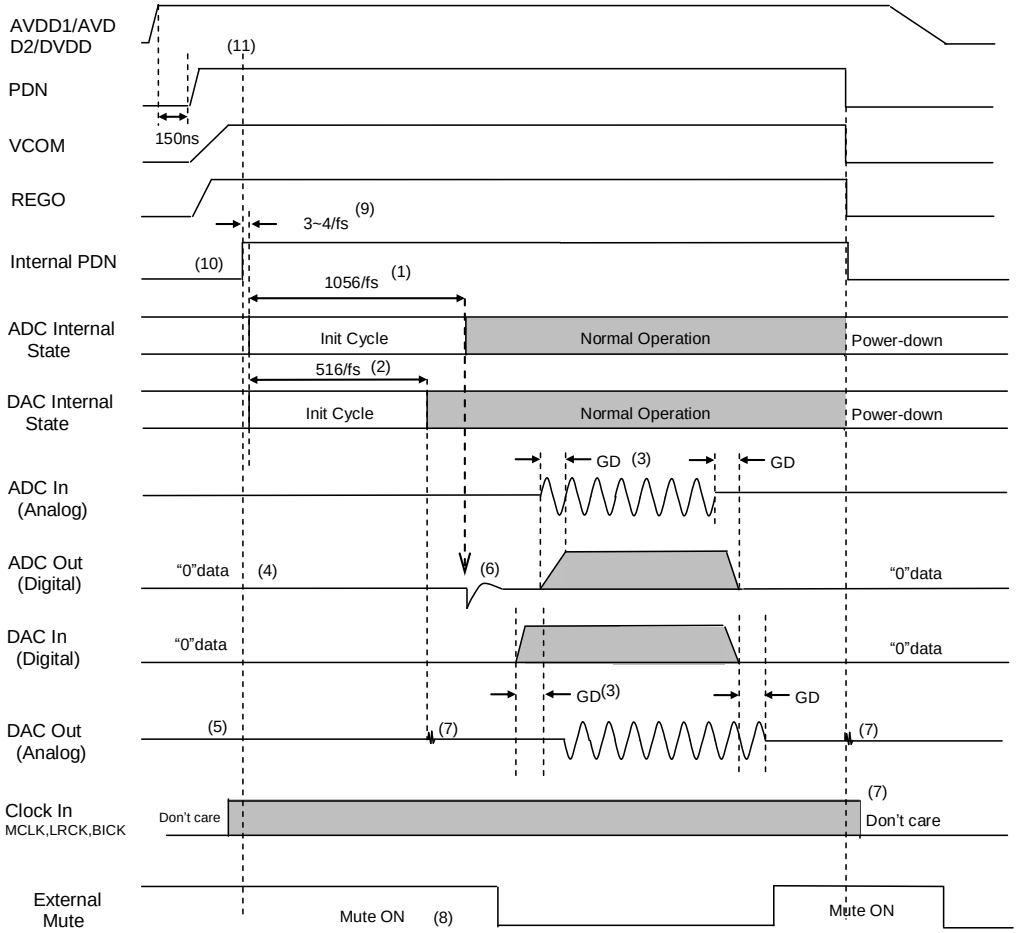
Figure 35. Soft Mute

■ System Reset

The AK4618 should be reset once by bringing the PDN pin = "L" upon power-up. The AK4618 is powered up and the internal timing starts clocking by MCLK or LRCK "↑" after exiting the power down state of reference voltage (such as VCOM) by the PDN pin. The AK4618 is in power-down mode until MCLK and LRCK, BICK are input.

■ Power-Down

All ADCs and DACs of the AK4618 are placed in power-down mode by bringing the PDN pin "L" which resets both digital filters at the same time. The PDN pin "L" also resets the control registers to their default values. In power-down mode, the SDTO goes to "L", and the analog outputs go to Hi-Z. This reset should always be executed after power-up. For the ADC, an analog initialization cycle (1056/fs) starts 3~4/fs after exiting power-down mode. The output data, SDTO is available after 1059~1060 cycles of the LRCK clock. For the DAC, an analog initialization cycle (516/fs) starts 3~4/fs after exiting power-down mode. The analog outputs go to Hi-Z during the initialization. Figure 36 shows the power-down and power-up sequences.



Notes:

(1) The analog part of ADC is initialized after exiting internal power-down state.
When start-up the AK4618, ADC input voltage should be operating common voltage.
It is necessary to wait for the charge up time of HPF which consists of analog inputs.
When the external capacitor is 1uF and the input impedance is 60kΩ(typ), τ = 0.06 sec.

(2) The analog part of DAC is initialized after exiting internal power-down state.

(3) Digital output corresponds to analog input and analog output corresponds to digital input have group delay (GD).

(4) ADC output is "0" data at power-down state.

(5) The analog outputs go to Hi-Z in power-down mode.

(6) Click noise occurs at the end of initialization of the analog part. Mute the digital output externally if the click noise influences system applications.

(7) Click noise occurs at the falling edge of PDN and at 519~520/fs after exiting internal power-down state.

(8) Mute the analog output externally if the click noise (7) influences system applications.

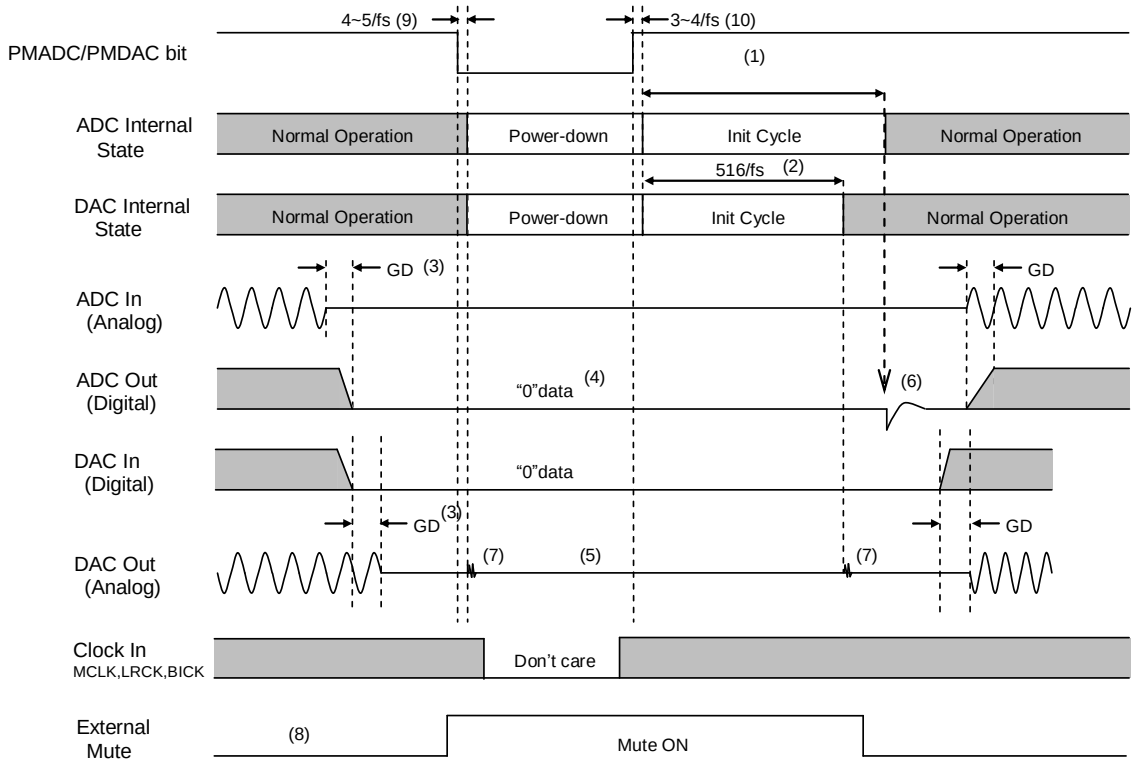
(9) There is a delay, 3~4/fs from internal power up to the start of initial cycle.

(10) The PDN pin must be "L" when power up the AK4618 and set to "H" after all poweres are supplied.

(11) The internal power-down state is released when MCLK counter rise.Do not write to the registers for 32768/MCLK(2.67ms@MCLK=12.288MHz, until internal power down is released after the PDN pin = "H".

Figure 36. Pin power-down/Pin power-up sequence example

All ADCs and all DACs can be powered-down individually through the PMADC bits and PMDAC bits. DAC1-6 can be power-down individually by PMDA6-1 bits. In this case, the internal register values are not initialized. When PMADC bit = "0", SDTO goes to "L". When PMDAC bit = "0", the analog outputs go to Hi-Z. As some click noise occurs, the analog output should be muted externally if the click noise influences system applications. Figure 37 shows the power-down and power-up sequences.



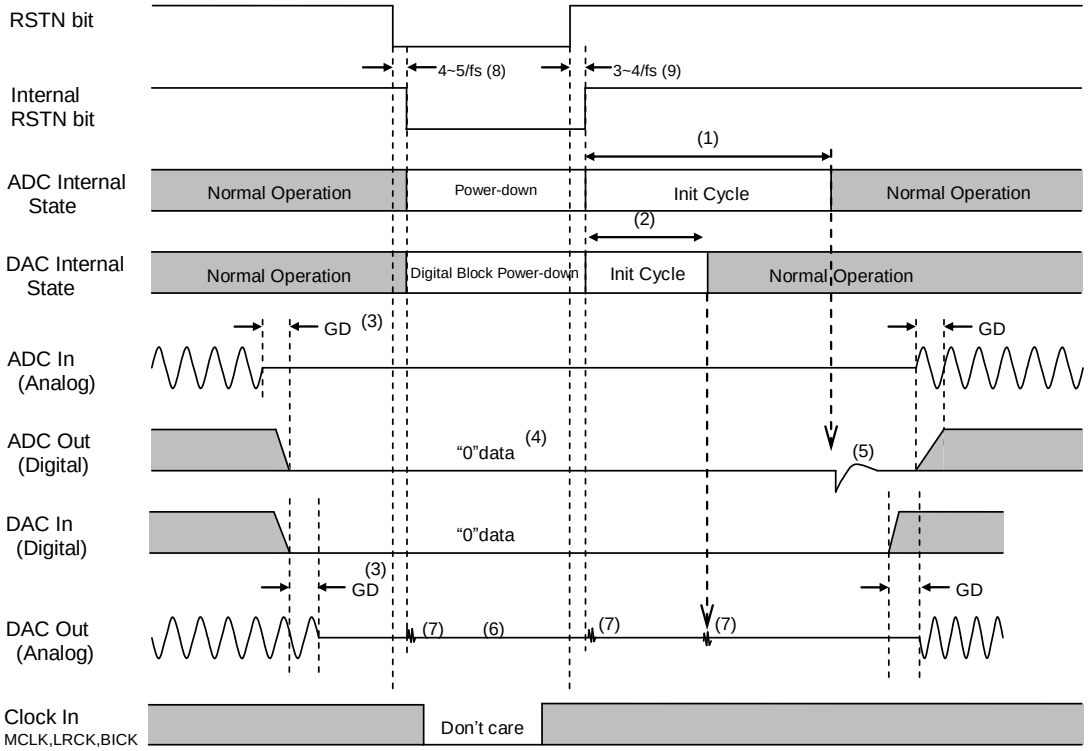
Notes:

(1) The analog section of ADC is initialized after exiting power-down state.
(2) The analog section of DAC is initialized after exiting power-down state.
(3) Digital output corresponding to the analog inputs and analog outputs corresponding to the digital inputs have group delay (GD).
(4) ADC output is "0" data at power-down state.
(5) DAC output is Hi-Z in power-down state.
(6) Click noise occurs at the end of initialization of the analog part. Mute the digital output externally if the click noise influences system application.
(7) Click noise occurs at 4~5/fs after PMDAC bit becomes "0", and occurs at 519~520/fs after PMDAC bit becomes "1".
(8) Mute the analog output externally if the click noise (7) influences system application.
(9) There is a delay, 4~5/fs from PMDAC bit becomes "0" to the applicable ADC power-down.
There is a delay, 4~5/fs from PMDAC bit becomes "0" to the applicable DAC power-down.
(10) There is a delay, 3~4/fs from PMADC and PMDAC bits become "1" to the start of initial cycle.

Figure 37. Bit power-down/Bit power-up sequence example

■ Reset Function

When RSTN bit= "0", the analog and digital part of ADC and DACs are powered-down, but the internal register are not initialized. The analog outputs go to Hi-Z, the SDTO pin goes to "L". As some click noise occurs, the analog output should be muted externally if the click noise influences system application. Figure 38 shows the power-up sequence.



Notes:

(1) The analog section of the ADC is initialized after exiting reset state.
The initializing cycle is 1056fs. When start-up the AK4618, ADC input voltage should be operating common voltage.

(2) The analog section of DAC is initialized after exiting exiting reset state.

(3) Digital output corresponding to the analog inputs, and analog outputs corresponding to the digital inputs have group delay (GD).

(4) ADC output is "0" data at power-down state.

(5) Click noise occurs when the initializing cycle is finished. Mute the digital output externally if the click noise influences system application.

(6) The analog outputs go to Hi-Z when RSTN bit becomes "0".

(7) Click noise occurs at 4~5/fs after RSTN bit becomes "0", and it occurs at 3~4/fs after RSTN bit becomes "1".

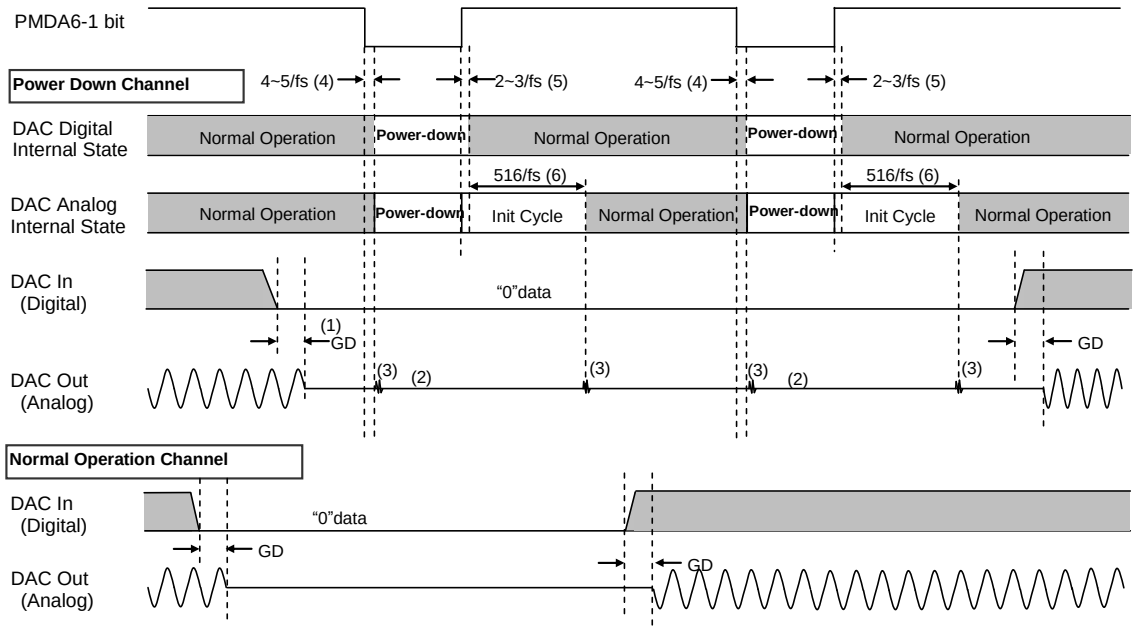
(8) There is a delay, 4~5/fs from RSTN bit "0" to the internal RSTN bit "0".

(9) There is a delay, 3~4/fs from RSTN bit "1" to the start of initial cycle.

Figure 38. Reset Sequence Example

■ DAC Partial Power-Down Function

All of the DACs can be powered-down individually by PMDA6-1 bits. The analog section and the digital section of the DAC are placed in power-down mode when the PMDA6-1 bits = "0". The analog output of the powered-down channels, which are set by PMDA6-1 bits, go to Hi-Z. Some click noise occurs in both set-up and release of power-down. Mute the analog output externally or set PMDA6-1 bits when PMDAC bit = "0" or RSTN bit = "0", if click noise aversely affects system performance. Figure 39 shows the sequence of the power-down and the power-up by PMDA6-1 bits.



Notes:

(1) Analog outputs corresponding to the digital inputs have group delay (GD).
(2) Analog output of the DAC is powered down by PMDA6-1 = "0" and goes to Hi-Z.
(3) Click noise occurs in 4~5/fs after PMDA6-1 bits are set to "0", and it occurs in 518~519/fs after PMDA6-1 bits are set to "1".
(4) The DACs will be powered-down 4~5fs after PMDA6-1 bits = "0"
(5) The initialization stars 2~3fs after PMDA6-1 bits are set to "1".
(6) The analog parts of DACs are initialized after exiting power down mode.

Figure 39. DAC Partial Power-down Example

■ Serial Control Interface

I²C-bus Control Mode
The AK4618 supports the fast-mode I²C-bus (max: 400kHz).

1. WRITE Operations
Figure 40 shows the data transfer sequence of the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 46). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010000" (Figure 41). If the slave address matches that of the AK4618, the AK4618 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 47). R/W bit = "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4618. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 42). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 43). The AK4618 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 46).

The AK4618 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4618 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 16H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 48) except for the START and STOP conditions.

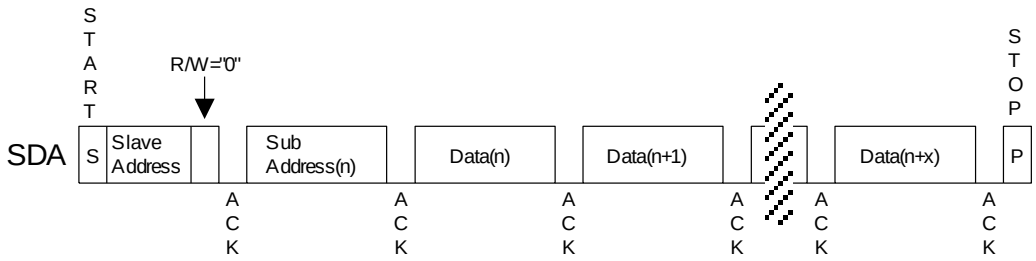


Figure 40. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	0	0	R/W

Figure 41. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 42. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 43. Byte Structure after the second byte

2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4618. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 16H prior to generating stop condition, the address counter will "roll over" to 00H and the data of 16H will be read out.

The AK4618 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK4618 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4618 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4618 ceases transmission.

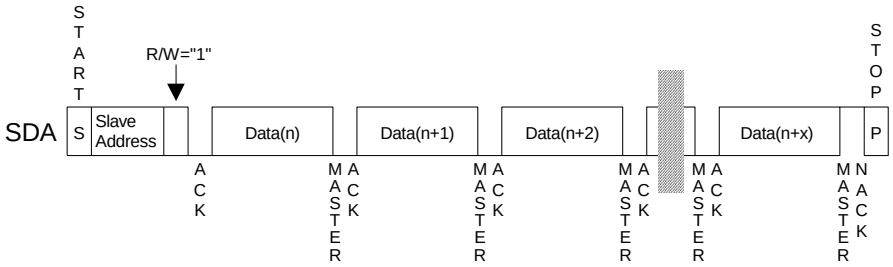


Figure 44. CURRENT ADDRESS READ

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit ="1", the master must execute a "dummy" write operation first. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit ="1". The AK4618 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4618 ceases transmission.

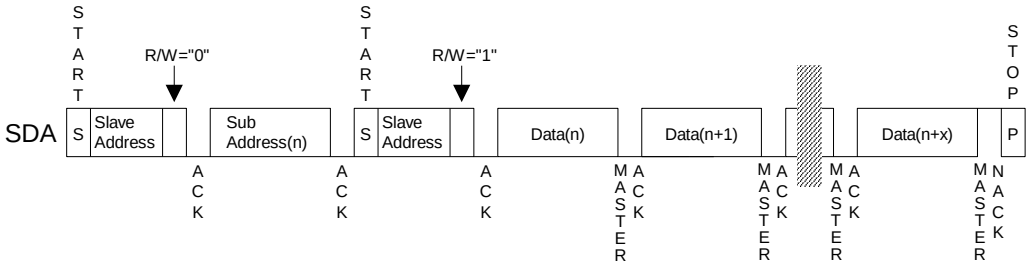


Figure 45. RANDOM ADDRESS READ

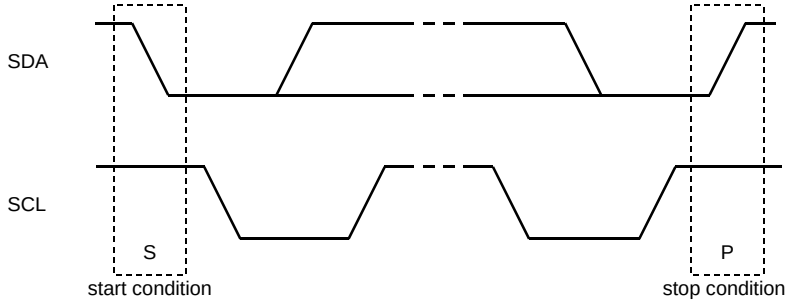


Figure 46. START and STOP Conditions

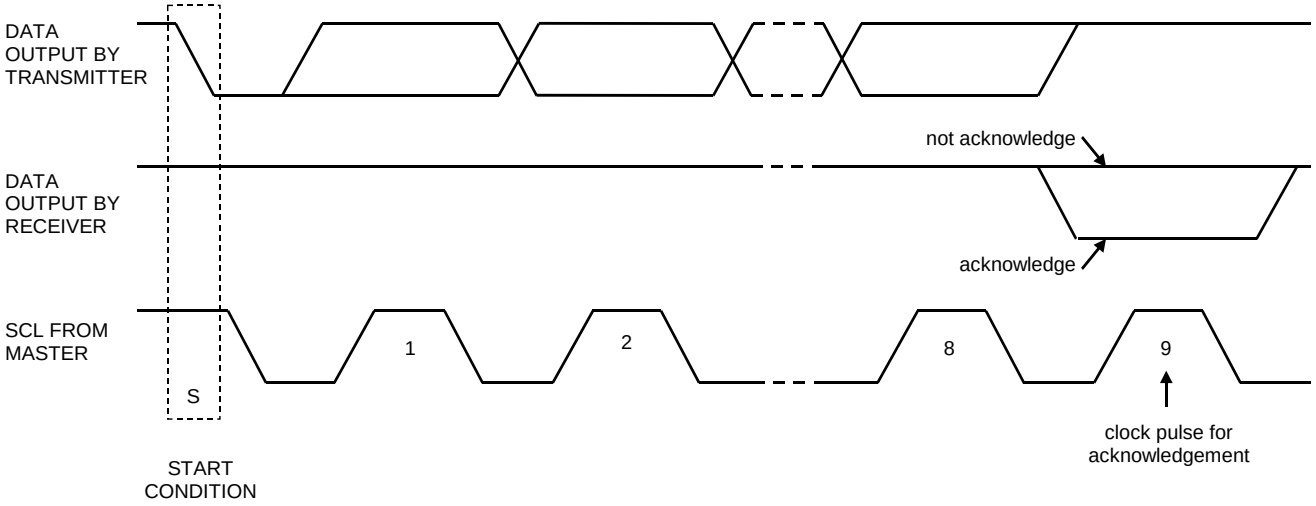


Figure 47. Acknowledge on the I^2C-Bus

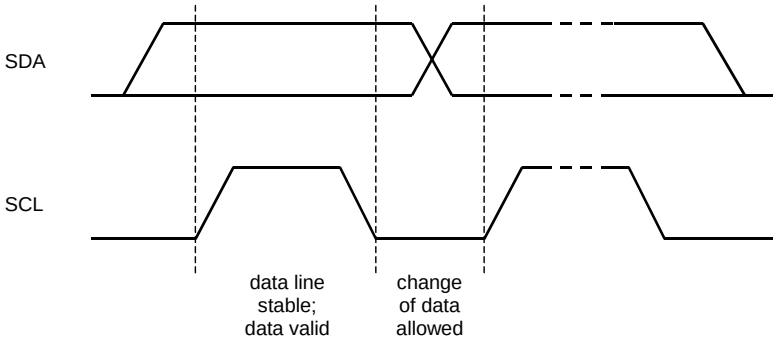


Figure 48. Bit Transfer on the I^2C-Bus

■ Register Map

Add	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	MS	PMMB	PMADC	PMDAC	PMADC56	PMADC34	PMADC12	RSTN
01H	Power Management 2	0	0	PMDA6	PMDA5	PMDA4	PMDA3	PMDA2	PMDA1
02H	System Clock	CKS1	CKS0	DFS1	DFS0	0	0	0	ACKS
03H	Filter setting1	DEM41	DEM40	DEM31	DEM30	DEM21	DEM20	DEM11	DEM10
04H	Filter setting2	SLOW	SD_DA	0	SD_AD	DEM61	DEM60	DEM51	DEM50
05H	Audio Interface Format	0	0	TDM1	TDM0	0	DIF2	DIF1	DIF0
06H	Soft Mute	0	0	DAATS1	DAATS0	0	0	0	SMUTEN
07H	DAC1L Volume	DAATL17	DAATL16	DAATL15	DAATL14	DAATL13	DAATL12	DAATL11	DAATL10
08H	DAC1R Volume	DAATR17	DAATR16	DAATR15	DAATR14	DAATR13	DAATR12	DAATR11	DAATR10
09H	DAC2L Volume	DAATL27	DAATL26	DAATL25	DAATL24	DAATL23	DAATL22	DAATL21	DAATL20
0AH	DAC2R Volume	DAATR27	DAATR26	DAATR25	DAATR24	DAATR23	DAATR22	DAATR21	DAATR20
0BH	DAC3L Volume	DAATL37	DAATL36	DAATL35	DAATL34	DAATL33	DAATL32	DAATL31	DAATL30
0CH	DAC3R Volume	DAATR37	DAATR36	DAATR35	DAATR34	DAATR33	DAATR32	DAATR31	DAATR30
0DH	DAC4L Volume	DAATL47	DAATL46	DAATL45	DAATL44	DAATL43	DAATL42	DAATL41	DAATL40
0EH	DAC4R Volume	DAATR47	DAATR56	DAATR45	DAATR44	DAATR43	DAATR42	DAATR41	DAATR40
0FH	DAC5L Volume	DAATL57	DAATL56	DAATL55	DAATL54	DAATL53	DAATL52	DAATL51	DAATL50
10H	DAC5R Volume	DAATR67	DAATR66	DAATR55	DAATR54	DAATR53	DAATR52	DAATR51	DAATR50
11H	DAC6L Volume	DAATL67	DAATL66	DAATL65	DAATL64	DAATL63	DAATL62	DAATL61	DAATL60
12H	DAC6R Volume	DAATR67	DAATR66	DAATR65	DAATR64	DAATR63	DAATR62	DAATR61	DAATR60
13H	Input Control	0	0	DIE6	DIE5	DIE4	DIE3	DIE2	DIE1
14H	Microphone Gain	0	0	MGAIN22	MGAIN21	MGAIN20	MGAIN12	MGAIN11	MGAIN10
15H	Microphone Gain	0	0	MGAIN42	MGAIN41	MGAIN40	MGAIN32	MGAIN31	MGAIN30
16H	Microphone Gain	0	0	MGAIN62	MGAIN61	MGAIN60	MGAIN52	MGAIN51	MGAIN50

Note: For addresses from 14H to 1FH, data must not be written. The bits defined as 0 must contain a “0” value.
When the PDN pin goes to “L”, the registers are initialized to their default values.
When RSTN bit goes to “0”, the internal timing is reset, but registers are not initialized to their default values.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	MS	PMMB	PMADC	PMDAC	PMAD56	PMAD34	PMAD12	RSTN
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	1	1	1	1	1	1

RSTN: Internal timing reset
0: Reset.
1: Normal operation (default)

PMAD12/34/56: Power management of ADC1-6 (0: Power-down, 1: Normal operation)
PMAD12: Power management control of ADC1 and ADC2
PMAD34: Power management control of ADC3 and ADC4
PMAD56: Power management control of ADC5 and ADC6

PMDAC: Power management of DAC1-6
0: All DAC's Power-down. PMDA1-6 bits are invalid.
1: Normal operation. (default) PMDA1-6 bits are valid.

PMADC: Power management of mono-stereo
0: All ADC's Power-down.
1: Normal operation. (default)

PMMB: Power management of microphone bias
0: Power-down
1: Normal operation (default)

MS : Master Mode Select
0: Slave Mode (default)
1: Master Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 3	0	0	PMDA6	PMDA5	PMDA4	PMDA3	PMDA2	PMDA1
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	1	1	1	1

PMDA6-1: Power management of DAC1-6 (0: Power-down, 1: Normal operation)
PMDA1: Power management control of DAC1
PMDA2: Power management control of DAC2
PMDA3: Power management control of DAC3
PMDA4: Power management control of DAC4
PMDA5: Power management control of DAC5
PMDA6: Power management control of DAC6

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	System Clock	CKS1	CKS0	DFS1	DFS0	0	0	0	ACKS
R/W		R/W	R/W	R/W	R/W	RD	RD	RD	R/W
Default		1	0	0	0	0	0	0	0

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the setting of DFS are ignored. When this bit is "0", DFS0, 1 set the sampling speed mode.

DFS1-0: Sampling speed mode (Table 1)
The setting of DFS is ignored at ACKS bit =“1”.

CKS1-0: Master Clock Input Frequency Select (Table 2)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Filter setting1	DEM41	DEM40	DEM31	DEM30	DEM21	DEM20	DEM11	DEM10
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	1	0	1

DEM11-10: De-emphasis response control for DAC1 data on SDTI1 (Table 8)
Initial: “01”, OFF

DEM21-20: De-emphasis response control for DAC2 data on SDTI2 (Table 8)
Initial: “01”, OFF

DEM31-30: De-emphasis response control for DAC3 data on SDTI3 (Table 8)
Initial: “01”, OFF

DEM41-40: De-emphasis response control for DAC4 data on SDTI4 (Table 8)
Initial: “01”, OFF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Filter setting2	SLOW	SD_DA	0	SD_AD	DEM61	DEM60	DEM51	DEM50
R/W		R/W	R/W	RD	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	1	0	1	0	1

DEM51-50: De-emphasis response control for DAC5 data on SDTI5 (Table 8)
Initial: “01”, OFF

DEM61-60: De-emphasis response control for DAC6 data on SDTI6 (Table 8)
Initial: “01”, OFF

SD_AD: Digital filter Setting for ADC
0: Sharp roll off filter
1: Short delay Sharp roll off filter (default)

SD_DA: Digital filter Setting for DAC
0: Sharp roll off filter or Slow roll off filter
1: Short delay Sharp roll off filter or Short delay Slow roll off filter (default)

SLOW: Slow Roll-off Filter Enable for DAC
0: Sharp Roll-off Filter (default)
1: Slow Roll-off Filter

SD_DA bit	SLOW bit	Mode	
0	0	Sharp roll-off filter	
0	1	Slow roll-off filter	
1	0	Short delay Sharp roll-off filter	(default)
1	1	Short delay Slow roll-off filter	

Table 18 Digital Filter setting for DAC

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	Audio Interface Format	0	0	TDM1	TDM0	0	DIF2	DIF1	DIF0
R/W		RD	RD	R/W	R/W	RD	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	0

DIF2-0: Audio Data Interface Modes (Table 10, Table 11, Table 12, Table 13)
Initial: "100", mode 4

TDM1-0: TDM Format Select (Table 10, Table 11, Table 12, Table 13)

Mode	TDM1	TDM0	SDTI	Sampling Speed
0	0	0	1-6	Stereo mode (Normal, Double, Quad Speed Mode)
1	0	1	1	TDM512 mode (Normal Speed Mode)
2	1	0	1-2	TDM256 mode (Normal, Double Speed Mode)
3	1	1	1-3	TDM128 mode (Quad Speed Mode)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Soft Mute	0	0	DAATS1	DAATS0	0	0	0	SMUTEN
R/W		RD	RD	R/W	R/W	RD	RD	RD	R/W
Default		0	0	0	0	0	0	0	1

SMUTEN: Soft Mute Enable
0: Mute
1: Unmute (default)

DAATS1-0: DAC Digital attenuator transition time setting (Table 15)
Initial: "00", mode 0

Add	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	DAC1L Volume	DAATL17	DAATL16	DAATL15	DAATL14	DAATL13	DAATL12	DAATL11	DAATL10
08H	DAC1R Volume	DAATR17	DAATR16	DAATR15	DAATR14	DAATR13	DAATR12	DAATR11	DAATR10
09H	DAC2L Volume	DAATL27	DAATL26	DAATL25	DAATL24	DAATL23	DAATL22	DAATL21	DAATL20
0AH	DAC2R Volume	DAATR27	DAATR26	DAATR25	DAATR24	DAATR23	DAATR22	DAATR21	DAATR20
0BH	DAC3L Volume	DAATL37	DAATL36	DAATL35	DAATL34	DAATL33	DAATL32	DAATL31	DAATL30
0CH	DAC3R Volume	DAATR37	DAATR36	DAATR35	DAATR34	DAATR33	DAATR32	DAATR31	DAATR30
0DH	DAC4L Volume	DAATL47	DAATL46	DAATL45	DAATL44	DAATL43	DAATL42	DAATL41	DAATL40
0EH	DAC4R Volume	DAATR47	DAATR56	DAATR45	DAATR44	DAATR43	DAATR42	DAATR41	DAATR40
0FH	DAC5L Volume	DAATL57	DAATL56	DAATL55	DAATL54	DAATL53	DAATL52	DAATL51	DAATL50
10H	DAC5R Volume	DAATR67	DAATR66	DAATR55	DAATR54	DAATR53	DAATR52	DAATR51	DAATR50
11H	DAC6L Volume	DAATL67	DAATL66	DAATL65	DAATL64	DAATL63	DAATL62	DAATL61	DAATL60
12H	DAC6R Volume	DAATR67	DAATR66	DAATR65	DAATR64	DAATR63	DAATR62	DAATR61	DAATR60
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DAATL1/R1 7-0, DAATL2/R2 7-0, DAATL3/R3 7-0, DAATL4/R4 7-0, DAATL5/R5 7-0, DAATL6/R6 7-0: Attenuation Level (Table 14)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Input Control	0	0	DIE6	DIE5	DIE4	DIE3	DIE2	DIE1
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

DIE6-1: Single-ended/Differential Input Select
0: Single-ended input to the IN1-6 pins. Leave the IN1-6N pins open. (default)
1: Differential input (IN1-6P and IN1-6N pins)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	Microphone Gain	0	0	MGAIN22	MGAIN21	MGAIN20	MGAIN12	MGAIN11	MGAIN10
15H	Microphone Gain	0	0	MGAIN42	MGAIN41	MGAIN40	MGAIN32	MGAIN31	MGAIN30
16H	Microphone Gain	0	0	MGAIN62	MGAIN61	MGAIN60	MGAIN52	MGAIN51	MGAIN50
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

MGAIN6-1 2-0: Microphone-Amp Gain Control (Table 16)
MGAIN6-1 2-0: “000” (0dB) (default)

SYSTEM DESIGN

Figure 49 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

- Differential Input Mode (DIE6-1 bits = "111111")

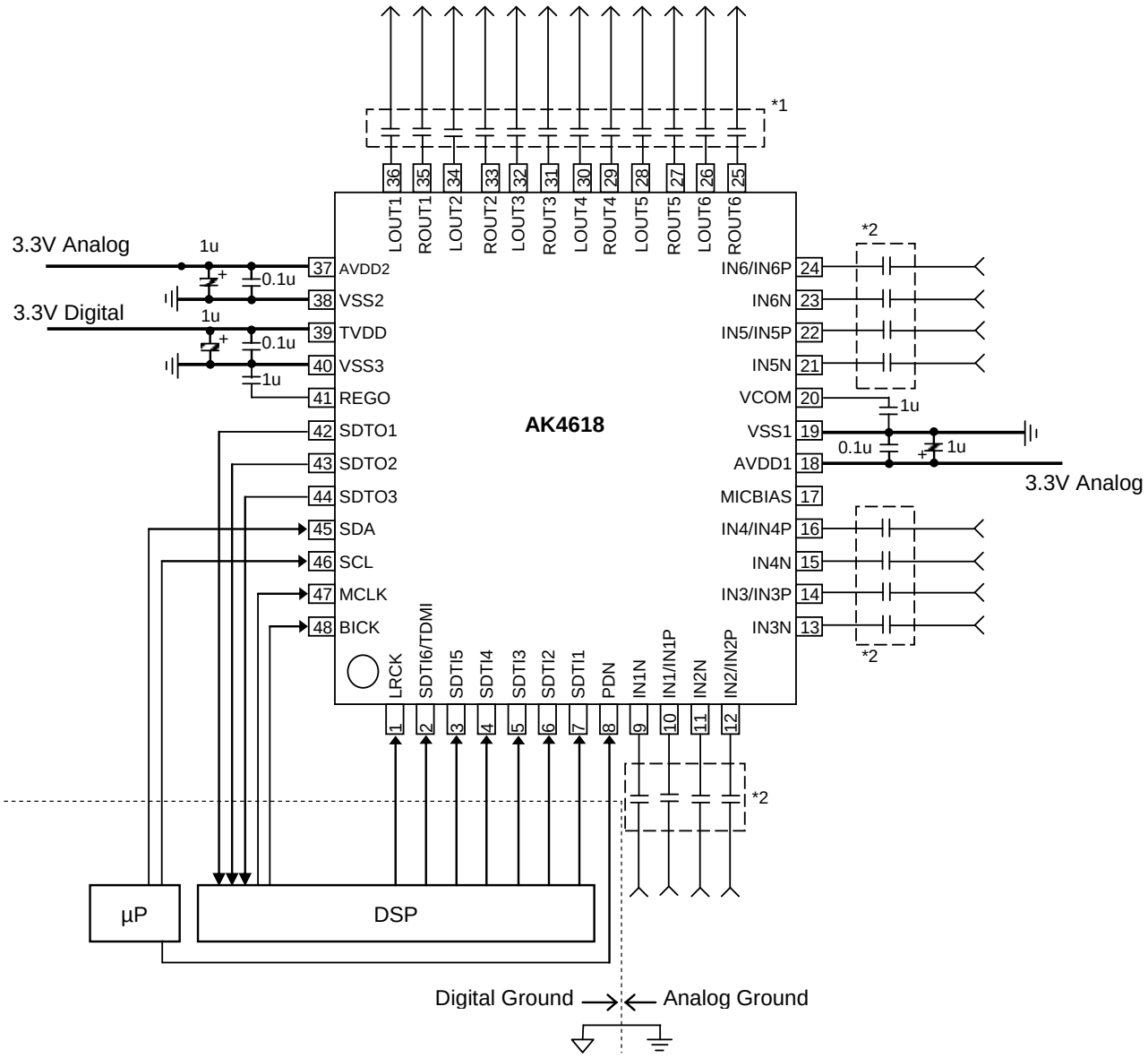


Figure 49. Typical Connection Diagram1

*1: Refer to Figure 52
*2: Refer to Figure 50, Figure 51

1. Grounding and Power Supply Decoupling

The AK4618 requires careful attention to power supply and grounding arrangements. AVDD1, AVDD2 and TVDD are usually supplied from analog supply in system. **VSS1 ~ 3 of the AK4618 must be connected to analog ground plane.** System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4618 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip and output the voltage AVDD1x1/2. A ceramic capacitor 1μF attached to the VCOM pin eliminates the effects of high frequency noise. This capacitor should be as close to the pin as possible. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4618.

3. Analog Inputs

The AK4618 supports single-ended and differential analog input. The single-ended input signal range scales with the supply voltage and nominally 0.81xAVDD1 Vpp (typ). The differential input signal range between IN+ and IN− scales with the supply voltage and nominally ±0.81xAVDD1 Vpp (typ). The power supply voltage range of the AK4618 is from VSS2 to AVDD1. The ADC output data format is 2's complement. The internal HPF removes the DC offset.

The AK4618 samples the analog inputs at 64fs (@ fs=48kHz). The digital filter removes noise above the stop band except for multiples of the sampling frequency of analog inputs. The AK4618 includes an anti-aliasing filter (RC filter) to attenuate a noise around the sampling frequency of analog inputs.

4. Analog Outputs

The single-ended output signal range is nominally 0.86 x AVDD2 Vpp centered around the VCOM voltage. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal output is VCOM voltage for 000000H(@24bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband, in single-ended input mode. There are no internal analog filters for differential output mode, therefore this noise should be removed by the external analog filters.

The DAC outputs have DC offsets of a few millivolts to VCOM voltage.

5. External Analog Inputs Circuit

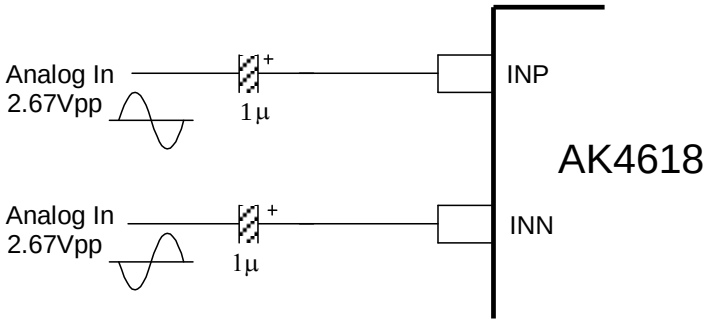


Figure 50. Input Buffer Circuit Example 1 (AC coupled differential input)
(IN1-6P/IN1-6N pins)

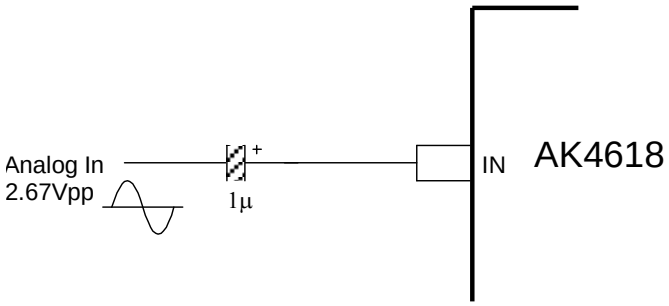


Figure 51. Input Buffer Circuit Example 2 (AC coupled single-ended input)
(IN1-6 pins)

6. External Analog Outputs Circuit

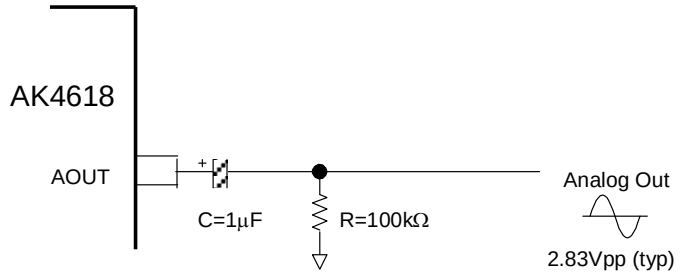


Figure 52. External Circuit Example (LOUT1-6, ROUT1-6 pins)

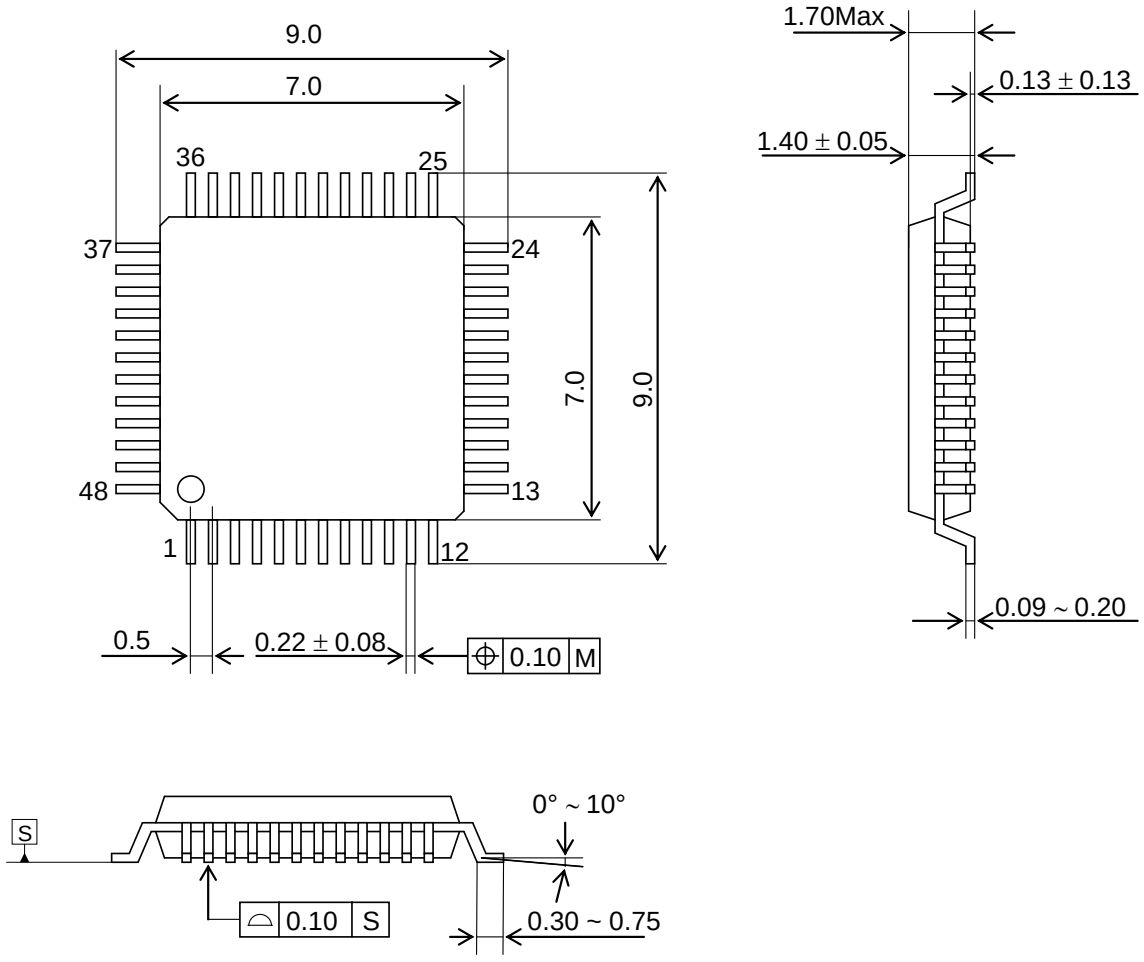
Note: The cut-offfrequency (fc) of HPF is determined by following equation.

$$fc = 1/(2 \times \pi \times R \times C)\ [Hz]$$

Where the C is the external AC coupling capacitor and the R is load resistance.
When C = 1μF and R = 100kΩ, then fs = 1.6Hz.

PACKAGE

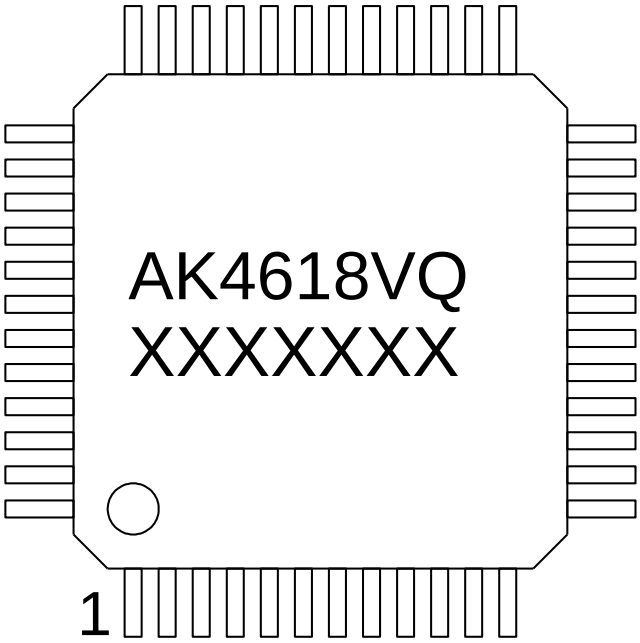
48-pin LQFP(Unit: mm)



■ Package & Lead frame material

Package molding compound:	Epoxy resin, Halogen (Br, Cl) free
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK4618VQ

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
15/01/23	00	First Edition		

IMPORTANT NOTICE

0. Asahi Kasei Microdevices Corporation (“AKM”) reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document (“Product”), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product’s quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.