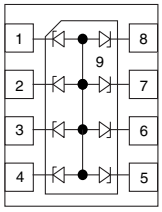
8-Line ESD-Protection Diode Array in LLP1713-9L



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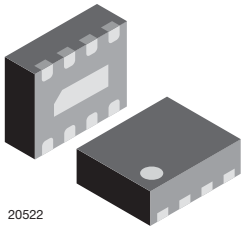
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FEATURES

- Ultra compact LLP1713-9L package
- Low package profile < 0.6 mm
- 8-line ESD-protection
- Low leakage current I_R < 1 µA
- Low load capacitance C_D = 10 pF
- ESD-immunity acc. IEC 61000-4-2
  ± 8 kV contact discharge
  ± 12 kV air discharge
- Working voltage range V_{RWM} = 5 V
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e4

RoHS COMPLIANT

HALOGEN FREE

GREEN (5-2008)

MARKING (example only)

20719

Dot = pin 1 marking
Y = type code (see table below)
XX = date code

ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VESD05A8C-HNH	VESD05A8C-HNH-GS08	3000	15 000

PACKAGE DATA

DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VESD05A8C-HNH	LLP1713-9L	F	3.7 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS VESD05A8C-HNH

PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	BiAs-mode: each input (pin 1 to pin 8) to ground (pin 9); acc. IEC 61000-4-5; t_p = 8/20 µs; single shot	I_{PPM}	2.5	A
Peak pulse power	BiAs-mode: each input (pin 1 to pin 8) to ground (pin 9); acc. IEC 61000-4-5; tp = 8/20 µs; single shot	P_{PP}	33	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses; BiAs-mode: each input (pin 1 to pin 8) to ground (pin 9)	V_{ESD}	± 8	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses; BiAs-mode: each input (pin 1 to pin 8) to ground (pin 9)		± 12	kV
Operating temperature	Junction temperature	T_J	-40 to +125	°C
Storage temperature		T_{STG}	-55 to +150	°C

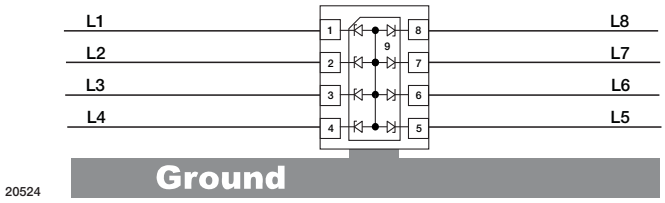
BiAs-MODE (8-line bidirectional asymmetrical protection mode)

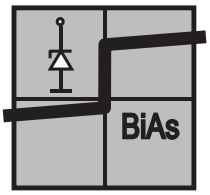
With the VESD05A8C-HNH up to 8 signal- or data-lines (L1 to L8) can be protected against voltage transients. With pin 9 connected to ground and pin 1 up to pin 8 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified maximum reverse working voltage (V_{RWM}) the protection diode between data line and ground offer a high isolation to the ground line. The protection device behaves like an open switch.

As soon as any positive transient voltage signal exceeds the break through voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The clamping voltage (V_C) is defined by the breakthrough voltage (V_{BR}) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device.

Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low forward voltage (V_F) clamps the negative transient close to the ground level.

Due to the different clamping levels in forward and reverse direction the VESD05A8C-HNH clamping behaviour is bidirectional and asymmetrical (BiAs).





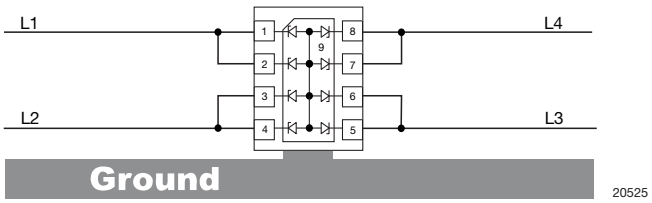
ELECTRICAL CHARACTERISTICS VESD05A8C-HNH						
PARAMETER	**TEST CONDITIONS/REMARKS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Protection paths	Number of lines which can be protected	N_{lines}	-	-	8	lines
Reverse working voltage	at I_R = 1 µA	V_{RWM}	5	-	-	V
Reverse current	at $V_R = V_{RWM}$ = 5 V	I_R	-	-	0.1	µA
Reverse breakdown voltage	at I_R = 1 mA	V_{BR}	6	-	8	V
Reverse clamping voltage	at I_{PP} = 2.5 A acc. IEC 61000-4-5	V_C	-	-	13	V
Forward clamping voltage	at I_F = 2.5 A acc. IEC 61000-4-5	V_F	-	-	4.5	V
Capacitance	at V_R = 0 V; f = 1 MHz	C_D	-	10	13	pF
	at V_R = 2.5 V; f = 1 MHz	C_D	-	5	7	pF

Notes

- Ratings at 25 °C, ambient temperature unless otherwise specified. BiAs mode: each input (pin 1 to pin 8) to ground (pin 9)

If a higher surge current or peak pulse current (I_{PP}) is needed, some protection diodes in the VESD05A8C-HNH can also be used in parallel in order to “multiply” the performance.
If two diodes are switched in parallel you get

- double surge power = double peak pulse current (2 x I_{PPM})
- half of the line inductance = reduced clamping voltage
- half of the line resistance = reduced clamping voltage
- double line capacitance (2 x C_D)
- double reverse leakage current (2 x I_R)



TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

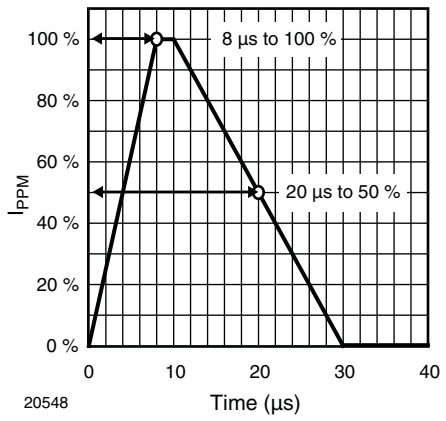


Fig. 1 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

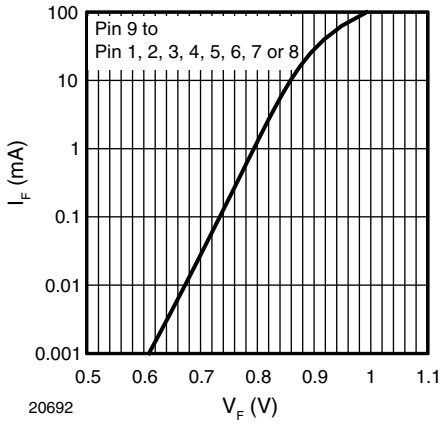


Fig. 4 - Typical Forward Current I_F vs. Forward Voltage V_F

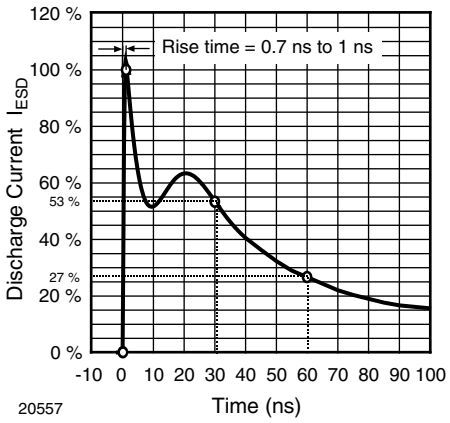


Fig. 2 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

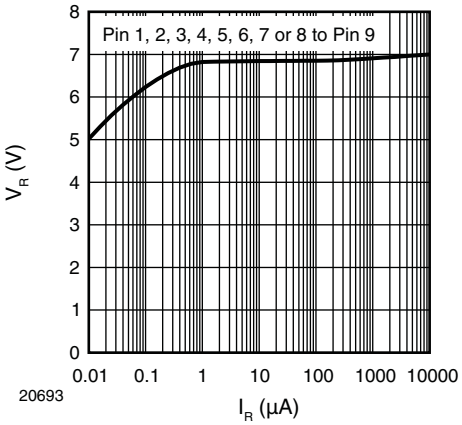


Fig. 5 - Typical Reverse Voltage V_R vs. Reverse Current I_R

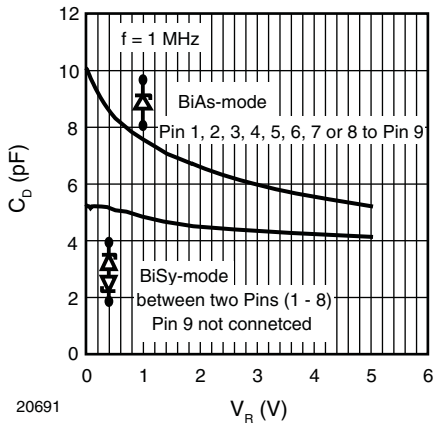


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

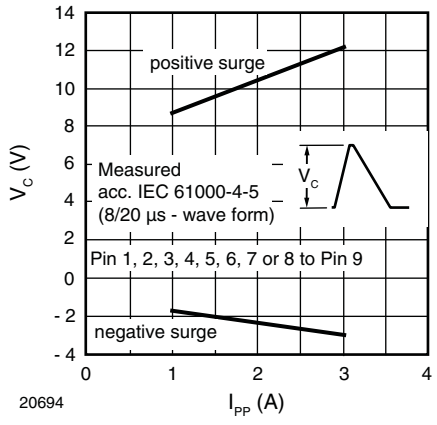
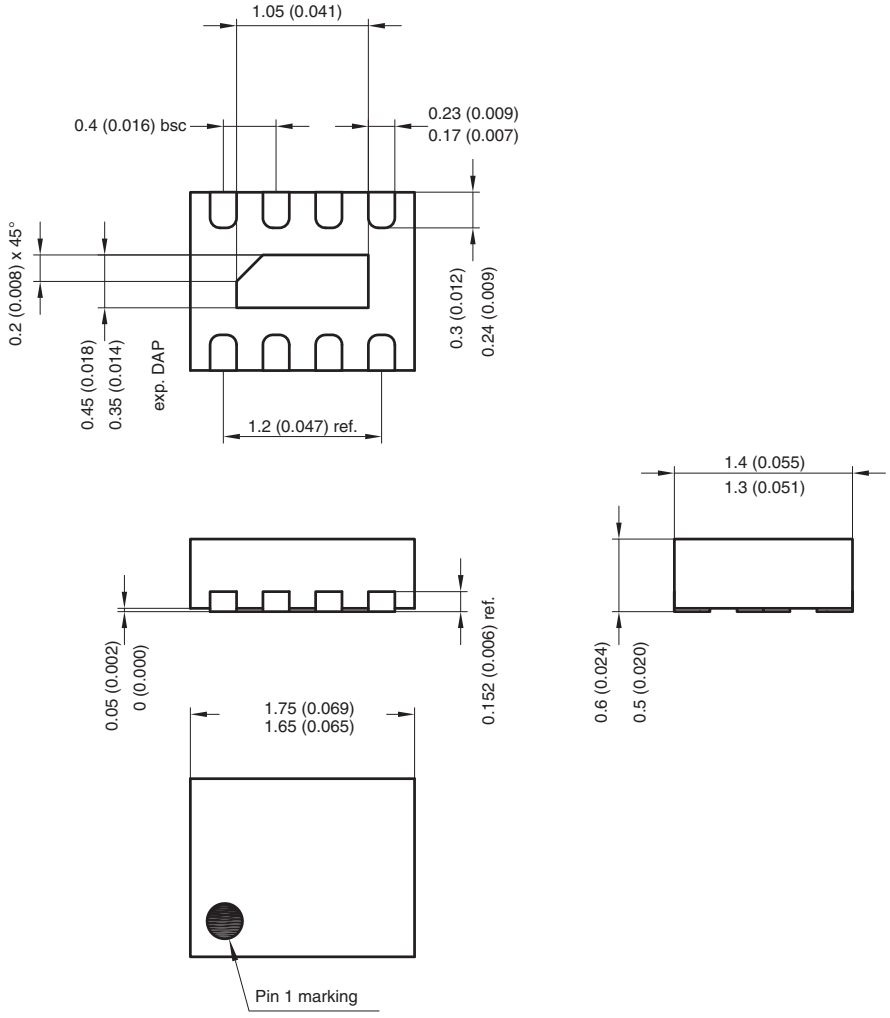
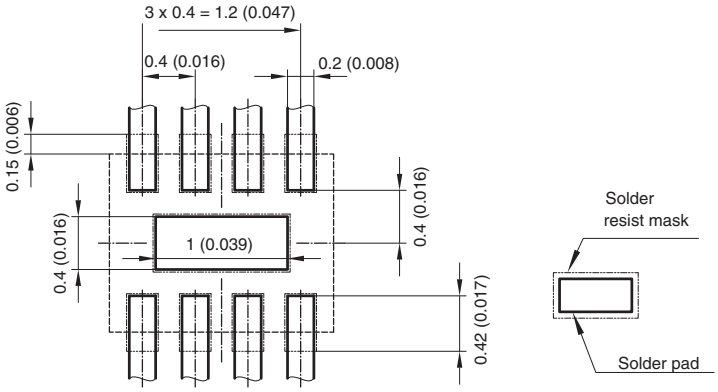


Fig. 6 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

PACKAGE DIMENSIONS in millimeters (inches): **LLP1713-9L**



Foot print recommendation:



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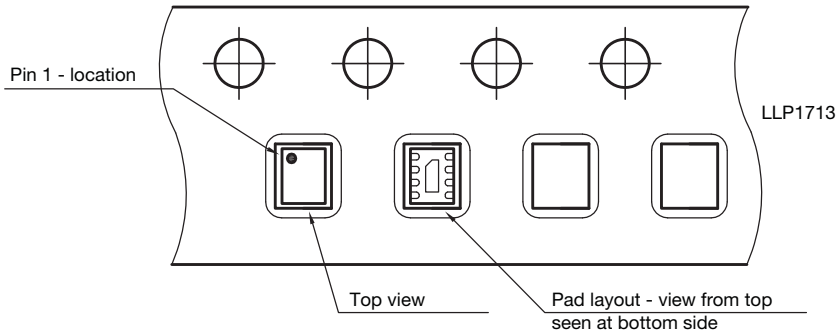

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