AOZ1024D

EZBuck™ 4A Synchronous Buck Regulator

Not Recommended For New Designs

General Description

The AOZ1024D is a synchronous high efficiency, simple to use, 4A buck regulator. The AOZ1024D works from a 4.5V to 16V input voltage range, and provides up to 4A of continuous output current with an output voltage adjustable down to 0.8V.

The AOZ1024D comes in a DFN 5 x 4 package and is rated over a -40°C to +85°C ambient temperature range.

Replacement Part: AOZ1034DI

Features

- 4.5V to 16V operating input voltage range
- Synchronous rectification: 100mΩ internal high-side switch and 20mΩ internal low-side switch
- High efficiency: up to 95%
- Internal soft start
- 1.5% initial output accuracy
- Output voltage adjustable to 0.8V
- 4A continuous output current
- Fixed 500kHz PWM operation
- Cycle-by-cycle current limit
- Pre-bias start-up
- Short-circuit protection
- Thermal shutdown
- Small size DFN 5 x 4 packages

Applications

- Point of load DC/DC conversion
- PCIe graphics cards
- Set top boxes
- DVD drives and HDD
- LCD panels
- Cable modems
- Telecom/networking/datacom equipment

Typical Application

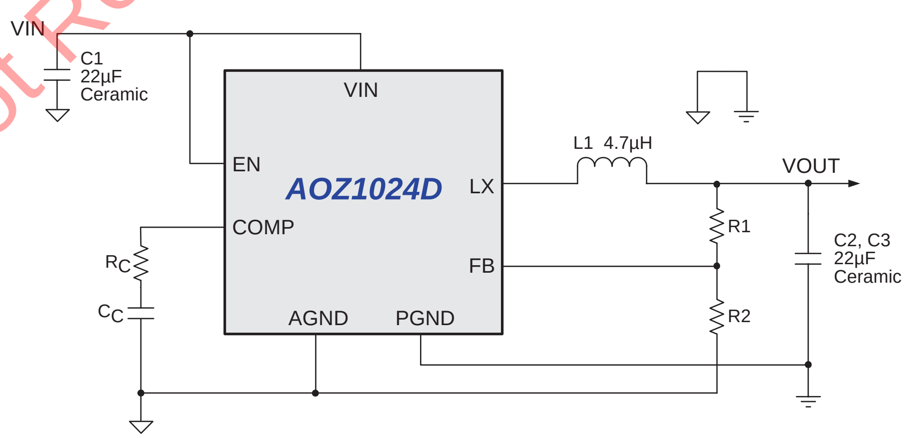


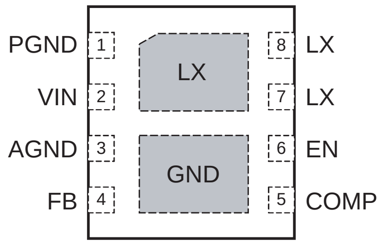
Figure 1. 3.3V/4A Synchronous Buck Regulator

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1024DI	-40°C to +85°C	DFN-8	Green

All AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration

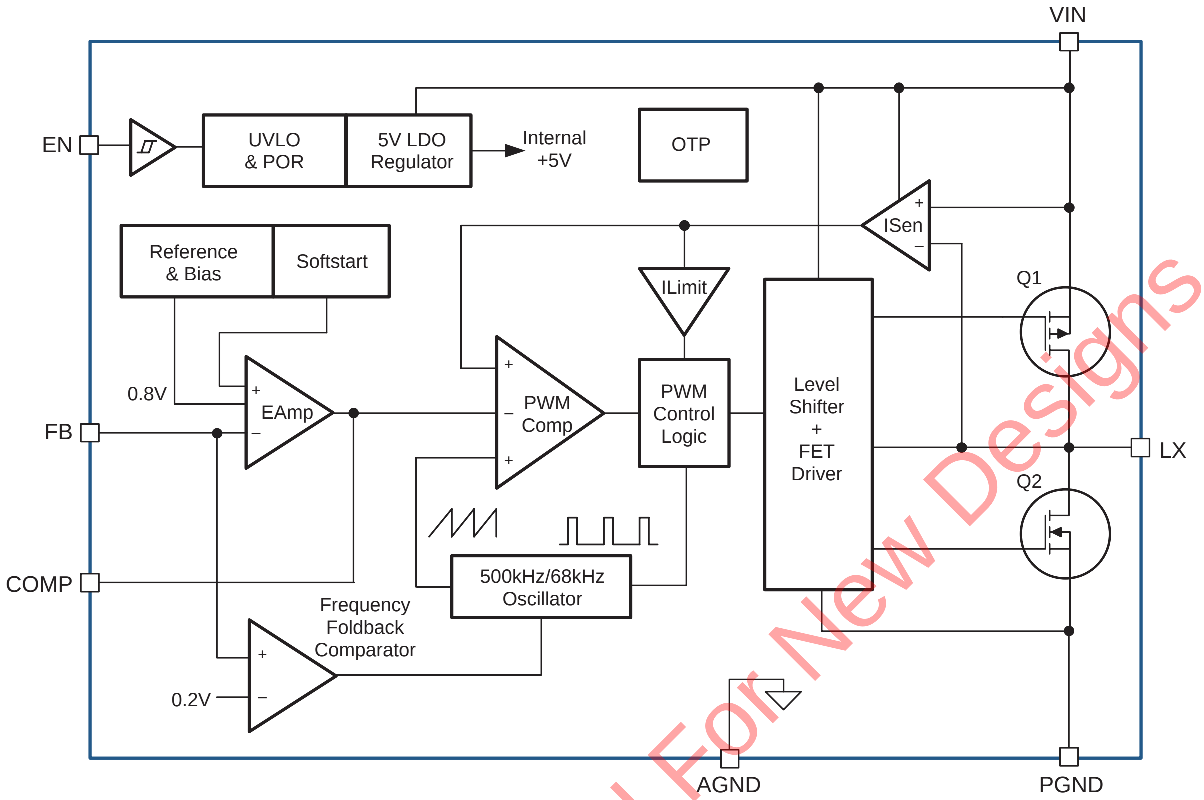


5 x 4 DFN
(Top Thru View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PGND	Power ground. Electrically needs to be connected to AGND.
2	V_{IN}	Supply voltage input. When V_{IN} rises above the UVLO threshold the device starts up.
3	AGND	Reference connection for controller section. Also used as thermal connection for controller section. Electrically needs to be connected to PGND.
4	FB	The FB pin is used to determine the output voltage via a resistor divider between the output and GND.
5	COMP	External loop compensation pin.
6	EN	The enable pin is active high. Connect in to V_{IN} if not used and do not leave it open.
7, 8	LX	PWM output connection to inductor.

Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	18V
LX to AGND	-0.7V to V_{IN}+0.3V
EN to AGND	-0.3V to V_{IN}+0.3V
FB to AGND	-0.3V to 6V
COMP to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +0.3V
PGOOD to AGND	-0.3V to 6V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating[(1)]	2.0kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommend Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

Parameter	Rating
Supply Voltage (V_{IN})	4.5V to 16V
Output Voltage Range	0.8V to V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance DFN-8 (Θ_{JA})[(2)]	50°C/W

Note:

2. The value of Θ_{JA} is measured with the device mounted on 1-in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified(3)

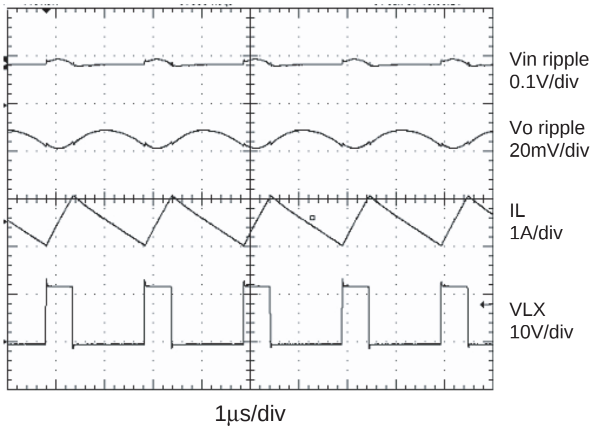
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Supply Voltage		**4.5**		**16**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} Rising V_{IN} Falling		**4.1** **3.7**		V
I_{IN}	Supply Current (Quiescent)	I_{OUT} = 0, VFB = 1.2V, V_{EN} > 1.2V		**1.6**	**2.5**	mA
I_{OFF}	Shutdown Supply Current	V_{EN} = 0V		**3**	**20**	µA
V_{FB}	Feedback Voltage		0.788	0.8	0.812	V
	Load Regulation			0.5		%
	Line Regulation			1		%
I_{FB}	Feedback Voltage Input Current				200	nA
V_{EN}	EN Input Threshold	Off Threshold On Threshold	 **2**		**0.6** 	V
V_{HYS}	EN Input Hysteresis			**100**		mV
MODULATOR						
f_O	Frequency		350	500	600	kHz
D_{MAX}	Maximum Duty Cycle		100			%
D_{MIN}	Minimum Duty Cycle				6	%
	Error Amplifier Voltage Gain			500		V / V
	Error Amplifier Transconductance			200		µA / V
PROTECTION						
I_{LIM}	Current Limit		5.0		6.0	A
	Over-Temperature Shutdown Limit	T_J Rising T_J Falling		150 100		°C
t_{SS}	Soft Start Interval		3	5	6.5	ms
OUTPUT STAGE						
	High-Side Switch On-Resistance	V_{IN} = 12V V_{IN} = 5V		97 166	130 200	mΩ
	Low-Side Switch On-Resistance	V_{IN} = 12V V_{IN} = 5V		18 30	23 36	mΩ

Note:
3. Specification in **BOLD** indicate an ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

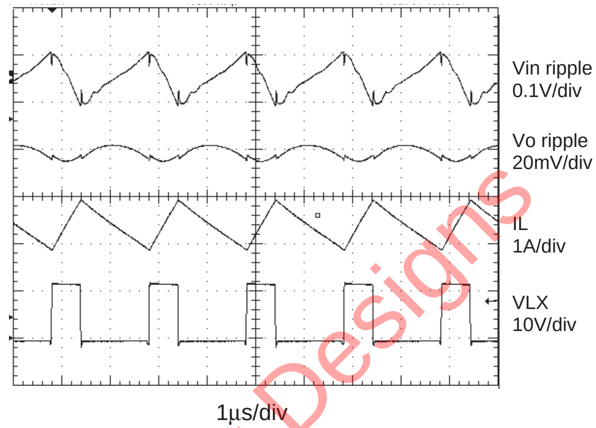
Typical Performance Characteristics

Circuit of Figure 1. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified.

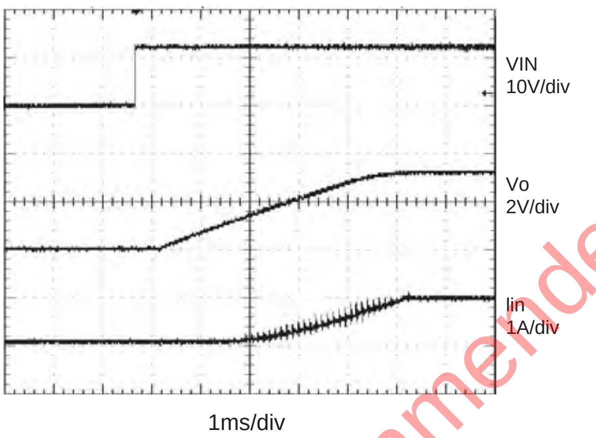
Light Load Operation



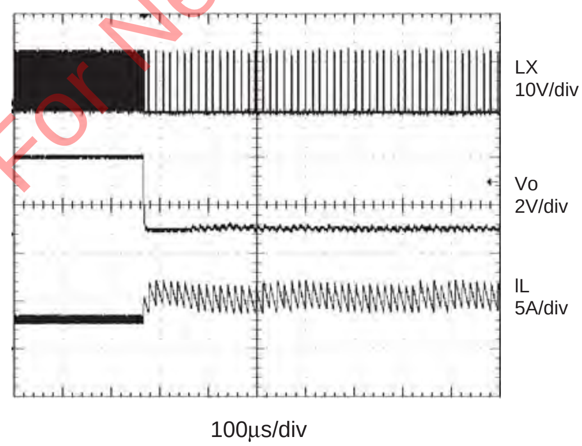
Full Load (CCM) Operation



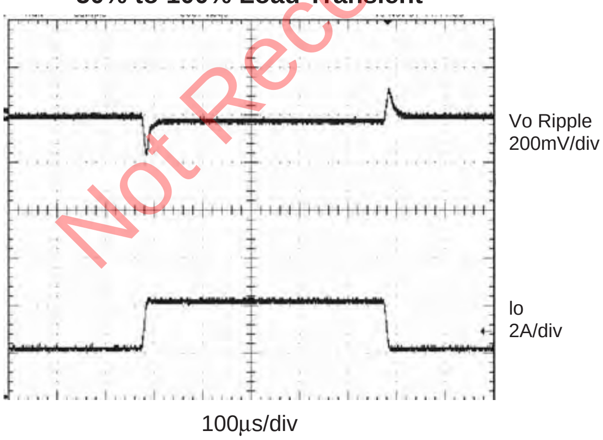
Startup to Full Load



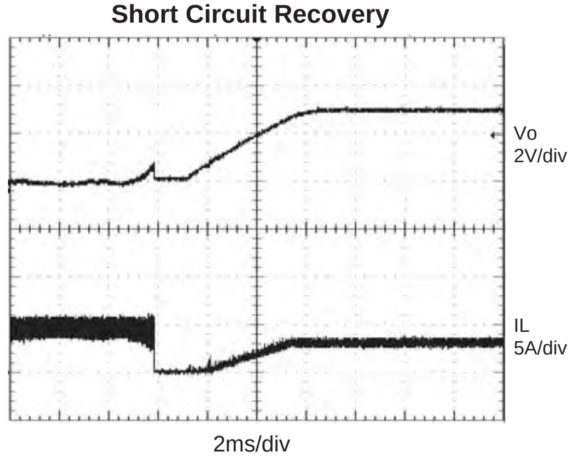
Short Circuit Protection



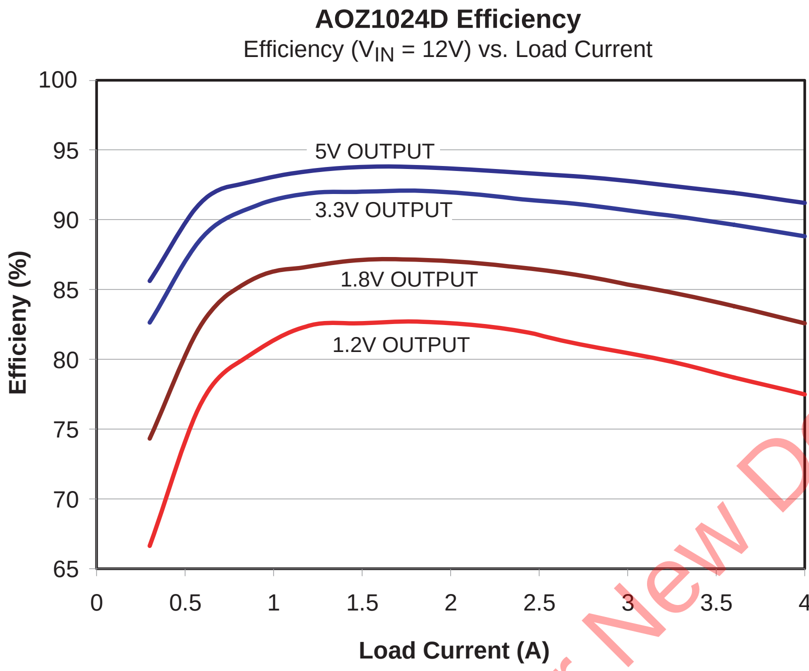
50% to 100% Load Transient



Short Circuit Recovery

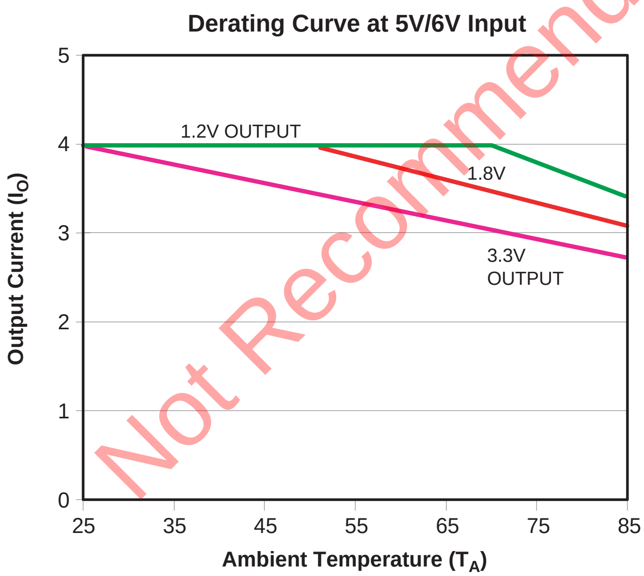


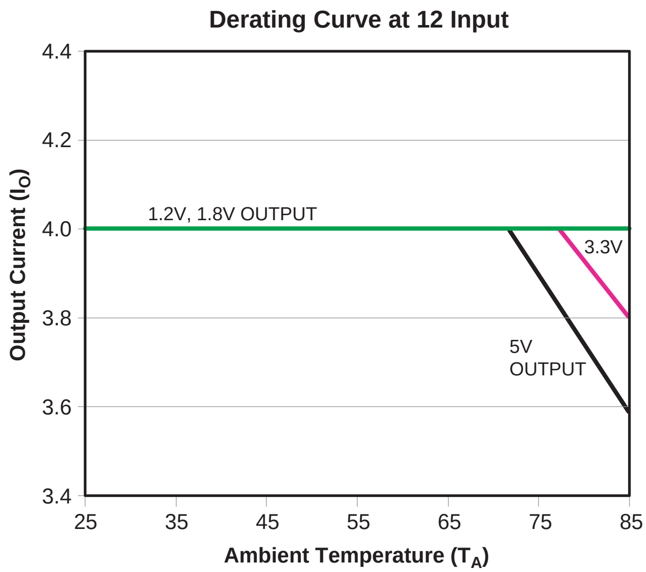
Efficiency



Thermal Derating Curves

For DFN package part under typical line and output voltage condition. Circuit of Figure 1. 25°C ambient temperature and natural convection (air speed<50LFM) unless otherwise specified.





Detailed Description

The AOZ1024D is a current-mode step down regulator with integrated high-side PMOS switch and a low-side NMOS switch. It operates from a 4.5V to 16V input voltage range and supplies up to 4A of load current. The duty cycle can be adjusted from 6% to 100% allowing a wide range of output voltage. Features include enable control, Power-On Reset, input under voltage lockout, output over voltage protection, active high power good state, fixed internal soft-start, and thermal shut down.

The AOZ1024D is available in a DFN 5x4 package.

Enable and Soft Start

The AOZ1024D has internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. A soft start process begins when the input voltage rises to 4.1V and voltage on the EN pin is HIGH. In the soft start process, the output voltage is typically ramped to regulation voltage in 4ms. The 4ms soft start time is set internally.

The EN pin of the AOZ1024D is active HIGH. Connect the EN pin to V_{IN} if enable function is not used. Pulling EN to ground will disable the AOZ1024D. Do not leave it open. The voltage on EN pin must be above 2V to enable the AOZ1024D. When voltage on the EN pin falls below 0.6V, the AOZ1024D is disabled. If an application circuit requires the AOZ1024D to be disabled, an open drain or open collector circuit should be used to interface to the EN pin.

Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1024D integrates an internal P-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal transconductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the internal low-side N-MOSFET switch to output. The internal adaptive FET driver guarantees no turn on overlap of both high-side and low-side switch.

Compared with regulators using freewheeling Schottky diodes, the AOZ1024D uses freewheeling NMOSFET to realize synchronous rectification. It greatly improves the converter efficiency and reduces power loss in the low-side switch.

The AOZ1024D uses a P-Channel MOSFET as the high-side switch. It saves the bootstrap capacitor normally seen in a circuit which is using an NMOS switch. It allows 100% turn-on of the high-side switch to achieve linear regulation mode of operation. The minimum voltage drop from V_{IN} to V_O is the load current x DC resistance of MOSFET + DC resistance of buck inductor. It can be calculated by equation below:

$$V_{O\_MAX} = V_{IN} - I_O \times R_{DSON}$$

where;

V_{O_MAX} is the maximum output voltage,

V_{IN} is the input voltage from 4.5V to 16V,

I_O is the output current from 0A to 2A, and

$R_{DS(ON)}$ is the on resistance of internal MOSFET, the value is between 97mΩ and 200mΩ depending on input voltage and junction temperature.

Switching Frequency

The AOZ1024D switching frequency is fixed and set by an internal oscillator. The practical switching frequency could range from 350kHz to 600kHz due to device variation.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin by using a resistor divider network (see Figure 1). The resistor divider network includes R_1 and R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R_1 with equation below:

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard values of R_1 and R_2 for the most commonly used output voltage values are listed in Table 1.

Table 1.

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	1.0	Open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.6	10
5.0	52.3	10

The combination of R_1 and R_2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Since the switch duty cycle can be as high as 100%, the maximum output voltage can be set as high as the input voltage minus the voltage drop on upper PMOS and inductor.

Protection Features

The AOZ1024D has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1024D employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4V and 2.5V internally. The peak inductor current is automatically limited cycle by cycle.

When the output is shorted to ground under fault conditions, the inductor current decays very slowly during a switching cycle because of V_O = 0V. To prevent catastrophic failure, a secondary current limit is designed inside the AOZ1024D. The measured inductor current is compared against a preset voltage which represents the current limit, between 5.0A and 6.0A. When the output current is more than current limit, the high side switch will be turned off. The converter will initiate a soft start once the over-current condition is resolved.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 4.1V, the converter starts operation. When input voltage falls below 3.7V, the converter will be shut down.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side PMOS if the junction temperature exceeds 150°C. The regulator will restart automatically under the control of soft-start circuit when the junction temperature decreases to 100ºC.

Application Information

The basic AOZ1024 application circuit is show in Figure 1. Component selection is explained below.

Input capacitor

The input capacitor must be connected to the V_{IN} pin and PGND pin of AOZ1024D to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if we let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 2 on the next page. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O.

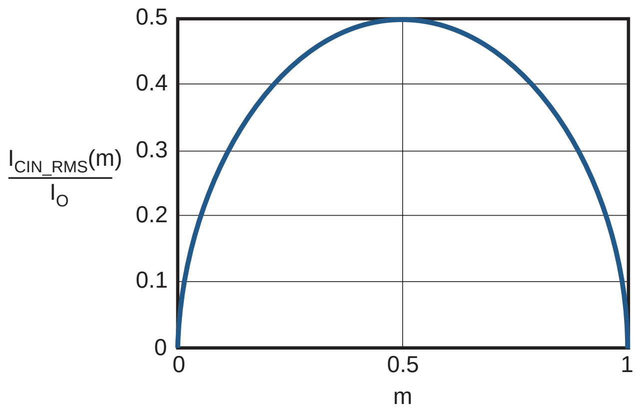


Figure 2. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than I_{CIN_RMS} at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. Depending on the application circuits, other low ESR tantalum capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures are based on certain amount of life time. Further de-rating may be necessary in practical design.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires a larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20–30% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor need to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise, but they cost more than unshielded inductors. The choice depends on EMI requirement, price, and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O}\right)$$

where,

C_O is output capacitor value, and

ESR_{CO} is the equivalent series resistance of the output capacitor.

When a low ESR ceramic capacitor is used as the output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum capacitors are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Loop Compensation

The AOZ1024D employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole can be calculated by:

$$f_{P1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

C_O is the output filter capacitor,

R_L is load resistor value, and

ESR_{CO} is the equivalent series resistance of output capacitor.

The compensation design is actually to shape the converter control loop transfer function to get desired gain and phase. Several different types of compensation network can be used for the AOZ1024D. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1024D, FB pin and COMP pin are the inverting input and the output of internal error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_2 \times G_{VEA}}$$

where;

G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V,

G_{VEA} is the error amplifier voltage gain, which is 500 V/V, and

C_2 is compensation capacitor in Figure 1.

The zero given by the external compensation network, capacitor C_2 and resistor R_3, is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover is the also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high because of system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be equal or less than 1/10 of switching frequency. The AOZ1024D operates at a frequency range from 350kHz to 600kHz. It is recommended to choose a crossover frequency equal or less than 40kHz.

$$f_C = 40kHz$$

The strategy for choosing R_C and CC is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_3:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_2}{G_{EA} \times G_{CS}}$$

where;

f_C is the desired crossover frequency. For best performance, f_C is set to be about 1/10 of the switching frequency;

V_{FB} is 0.8V,

G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V, and

G_{CS} is the current sense circuit transconductance, which is 6.68 A/V.

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected cross-over frequency. C_2 can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{P1}}$$

The previous equation can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Thermal Management and Layout Consideration

In the AOZ1024D buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the V_{IN} pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low-side NMOSFET. Current flows in the second loop when the low-side NMOSFET is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ1024D.

In the AOZ1024D buck regulator circuit, the major power dissipating components are the AOZ1024D and the output inductor. The total power dissipation of converter circuit can be measured by input power – output power.

$$P_{total} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of the inductor can be approximately calculated by output current and DCR of inductor.

$$P_{inductor} = I_O^2 \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ1024D and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total} - P_{inductor\_loss}) \times \Theta_{JA}$$

The maximum junction temperature of AOZ1024D is 150°C, which limits the maximum load current capability. Please see the thermal de-rating curves for maximum load current of the AOZ1024D under different ambient temperature.

The thermal performance of the AOZ1024D is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

The AOZ1024D is standard DFN5*4 package. Several layout tips are listed below for the best electric and thermal performance. Figure 3 on the next page illustrates a PCB layout example of AOZ1024D.

1. The LX pins are connected to internal PFET and NFET drains. They are low resistance thermal conduction path and most noisy switching node. Connected a large copper plane to LX pin to help thermal dissipation. For full load (4A) application, also connect the LX pads to the bottom layer by thermal vias to enhance the thermal dissipation.
2. Do not use thermal relief connection to the V_{IN} and the PGND pin. Pour a maximized copper area to the PGND pin and the VIN pin to help thermal dissipation.
3. Input capacitor should be connected to the V_{IN} pin and the PGND pin as close as possible.
4. A ground plane is preferred. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin.
5. Make the current trace from LX pins to L to C_O to the PGND as short as possible.
6. Pour copper plane on all unused board area and connect it to stable DC nodes, like V_{IN}, GND or V_{OUT}.
7. Keep sensitive signal trace far away form the LX pins.

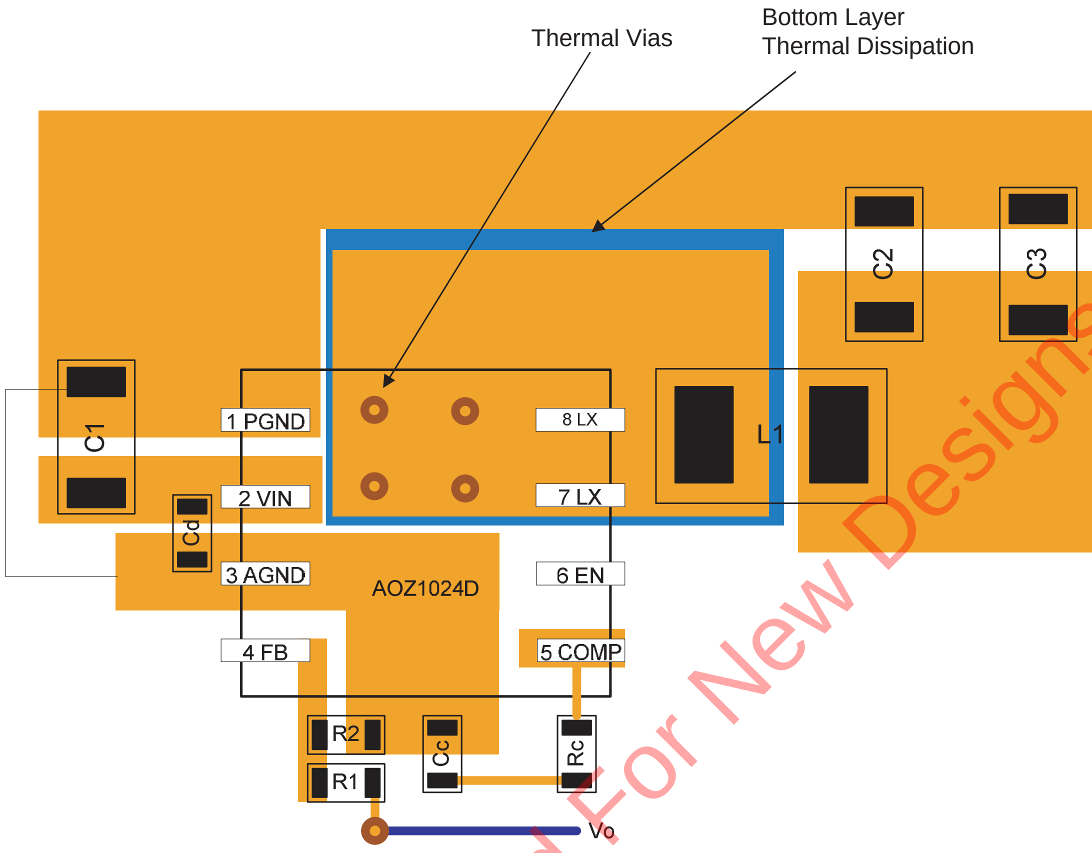
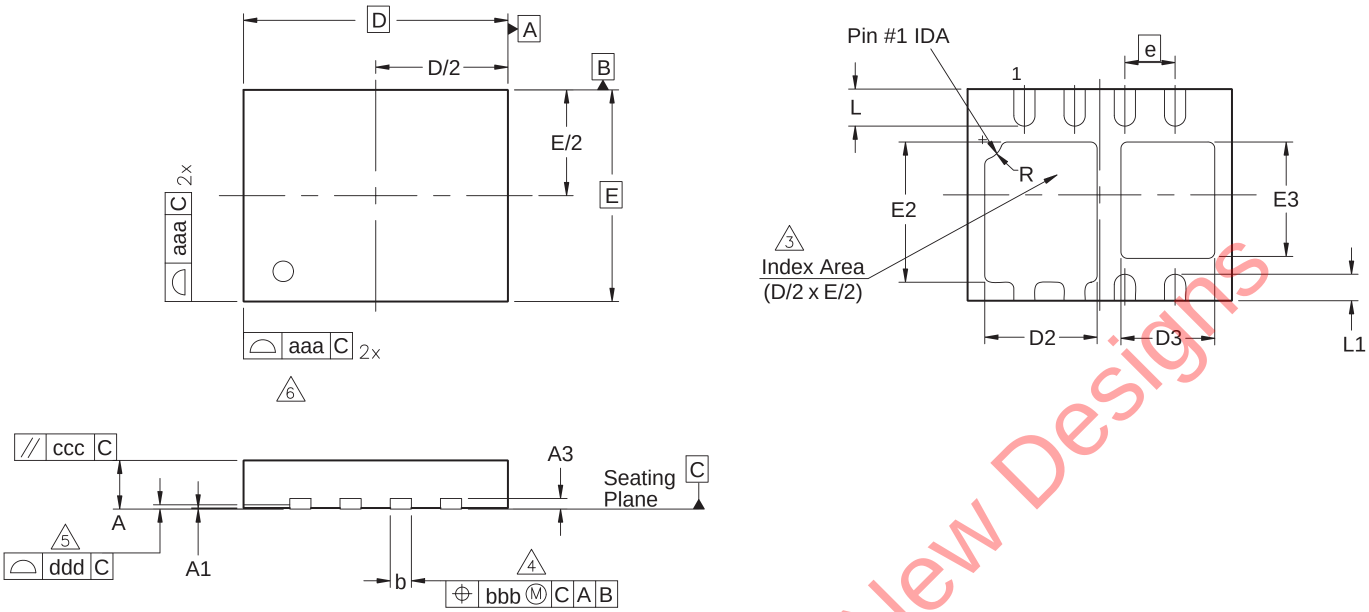
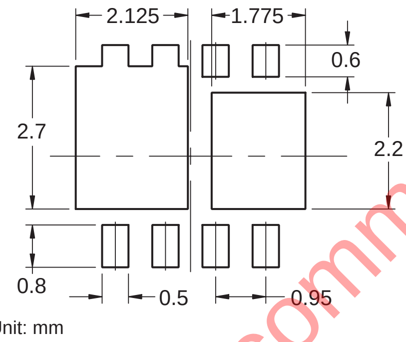


Figure 3. AOZ1024D (DFN 5x4) PCB Layout

Package Dimensions, DFN 5x4



Recommended Land Pattern



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.35	0.40	0.45
D		5.00 BSC	
D2	1.975	2.125	2.225
D3	1.625	1.775	1.875
E		4.00 BSC	
E2	2.500	2.650	2.750
E3	2.050	2.200	2.300
e		0.95 BSC	
L	0.600	0.700	0.800
L1	0.400	0.500	0.600
R		0.30 REF	
aaa	–	0.15	–
bbb	–	0.10	–
ccc	–	0.10	–
ddd	–	0.08	–

Dimensions in inches

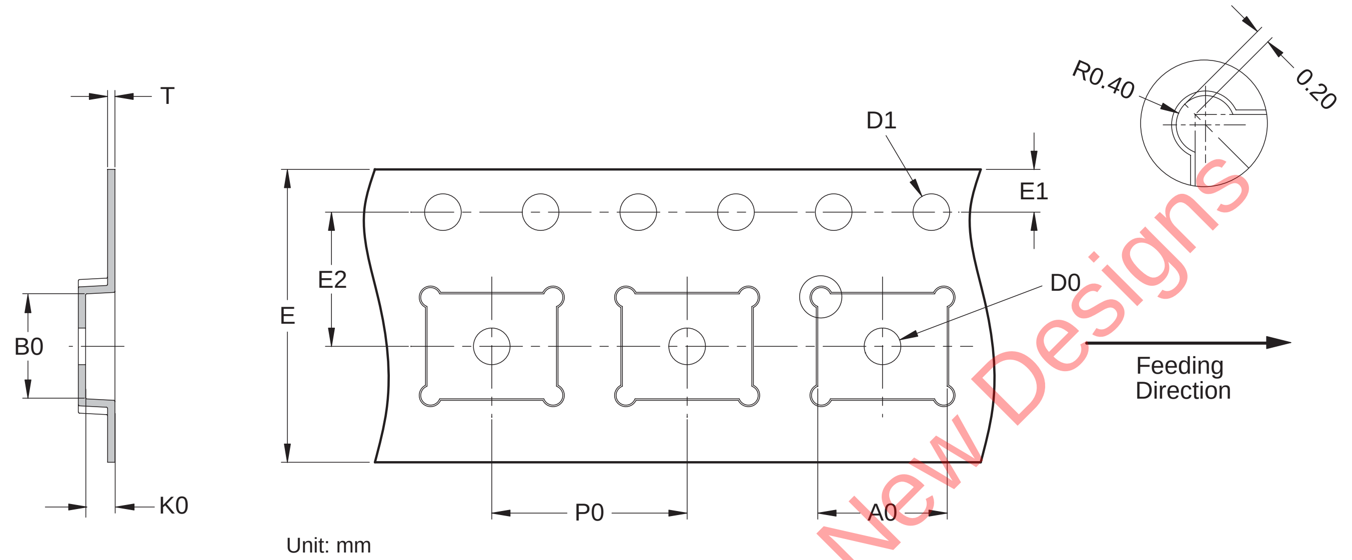
Symbols	Min.	Nom.	Max.
A	0.031	0.035	0.039
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.014	0.016	0.018
D		0.197 BSC	
D2	0.078	0.084	0.088
D3	0.064	0.070	0.074
E		0.157 BSC	
E2	0.098	0.104	0.108
E3	0.081	0.087	0.091
e		0.037 BSC	
L	0.024	0.028	0.031
L1	0.016	0.020	0.024
R		0.012 REF	
aaa	–	0.006	–
bbb	–	0.004	–
ccc	–	0.004	–
ddd	–	0.003	–

Notes:

1. Dimensions and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters.
3. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SP-002.
4. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all other bottom surface metallization.
6. Drawing shown are for illustration only.

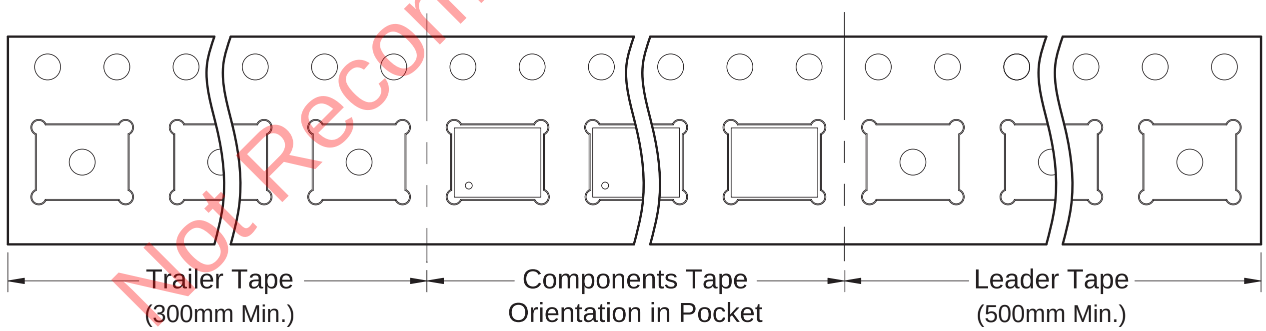
Tape Dimensions, DFN 5x4

Tape

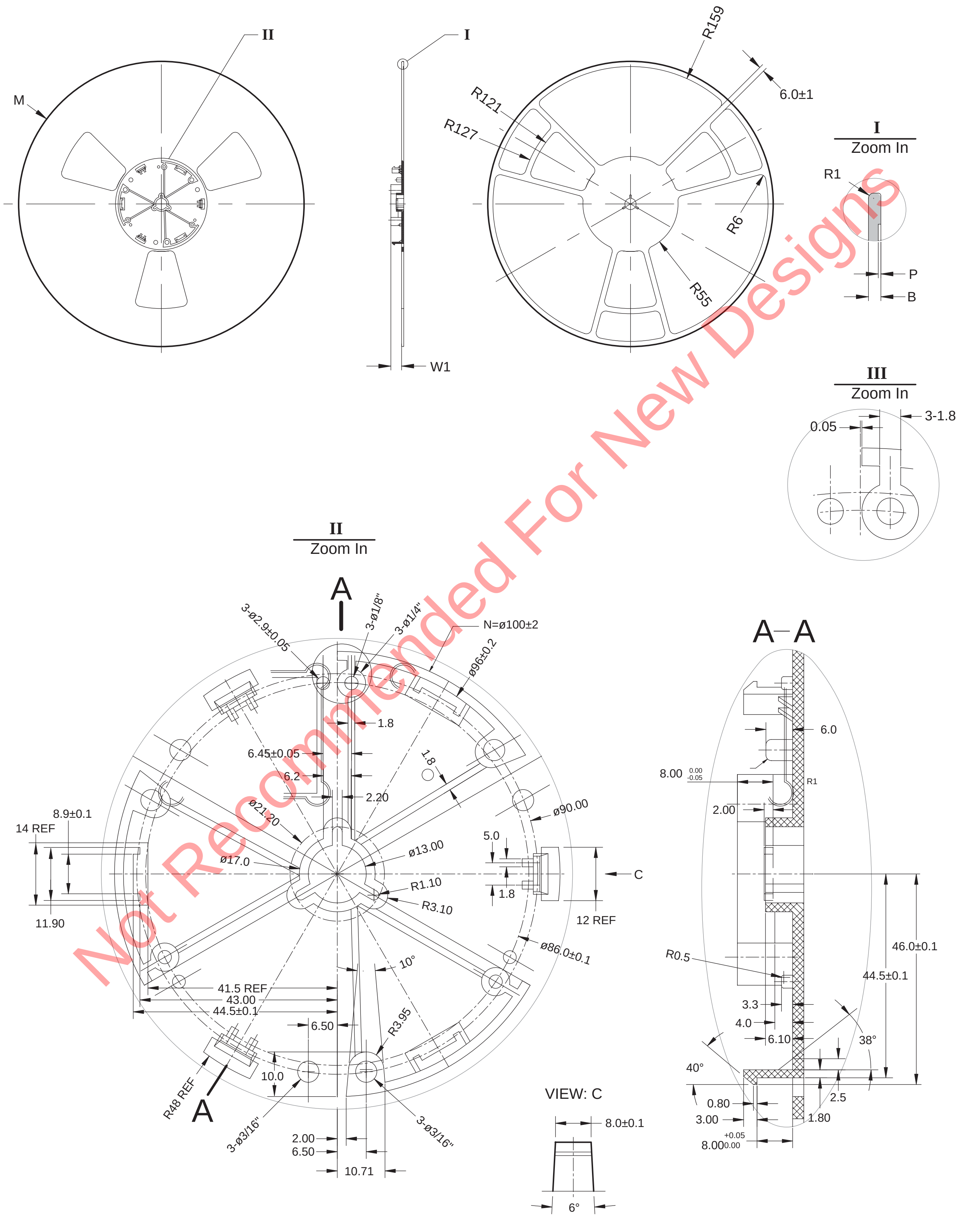


Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 5x4 (12 mm)	5.30 ±0.10	4.30 ±0.10	1.20 ±0.10	1.50 Min. Typ.	1.50 +0.10 / –0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.20	2.00 ±0.10	0.30 ±0.05

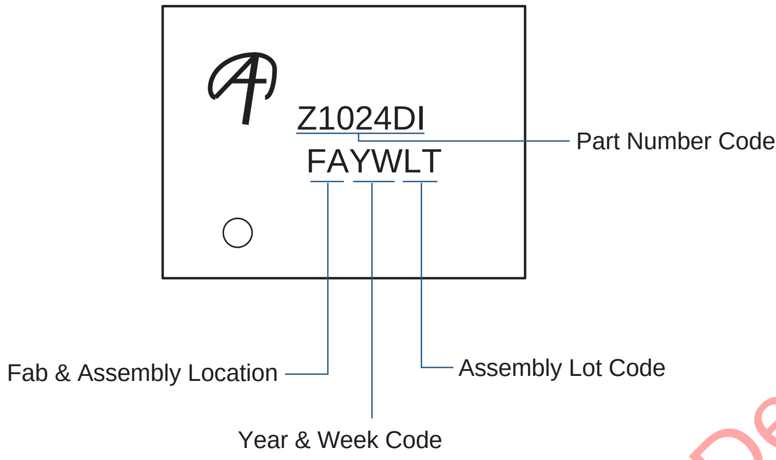
Leader/Trailer and Orientation



Reel Dimensions, DFN 5x4



AOZ1024D Package Marking



This data sheet contains preliminary data; supplementary data may be published at a later date. Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.