ZL30250, ZL30251

3-Input, 3-Output Any-to-Any Clock Multiplier and Frequency Synthesizer

Product Brief

August 2014

Features

- **4 Input Clocks**
  - One crystal/CMOS input
  - Two differential/CMOS inputs
  - One single-ended/CMOS input
  - Any input frequency from 9.72MHz to 1250MHz (9.72MHz to 300MHz for CMOS)
  - Clock selection by pin or register control
- **Low-jitter Fractional-N APLL and 3 Outputs**
  - Any output frequency from <1Hz to 1035MHz
  - High-resolution fractional frequency conversion with 0ppm error
  - Easy-to-configure, encapsulated design requires no external VCXO or loop filter components
  - Each output has independent dividers
  - Output jitter is typically 0.16 to 0.28ps RMS (12kHz-20MHz integration band)
  - Outputs are CML or 2xCMOS, can interface to LVDS, LVPECL, HSTL, SSTL and HCSL
  - In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)
  - Per-output supply pin with CMOS output voltages from 1.5V to 3.3V

Ordering Information

ZL30250LDG1	32 Pin QFN	Trays
ZL30250LDF1	32 Pin QFN	Tape and Reel
ZL30251LDG1	32 Pin QFN	Trays
ZL30251LDF1	32 Pin QFN	Tape and Reel

Matte Tin

Package size: 5 x 5 mm

-40°C to +85°C

  - Precise output alignment circuitry and per-output phase adjustment
  - Per-output enable/disable and glitchless start/stop (stop high or low)
- **General Features**
  - Automatic self-configuration at power-up from external (ZL30250) or internal (ZL30251) EEPROM; up to four configs, pin-selectable
  - Numerically controlled oscillator mode
  - Spread-spectrum modulation mode
  - SPI or I^2C processor Interface
  - Tiny 5x5mm QFN package
  - Easy-to-use evaluation software

Applications

- Frequency conversion and frequency synthesis in a wide variety of equipment types

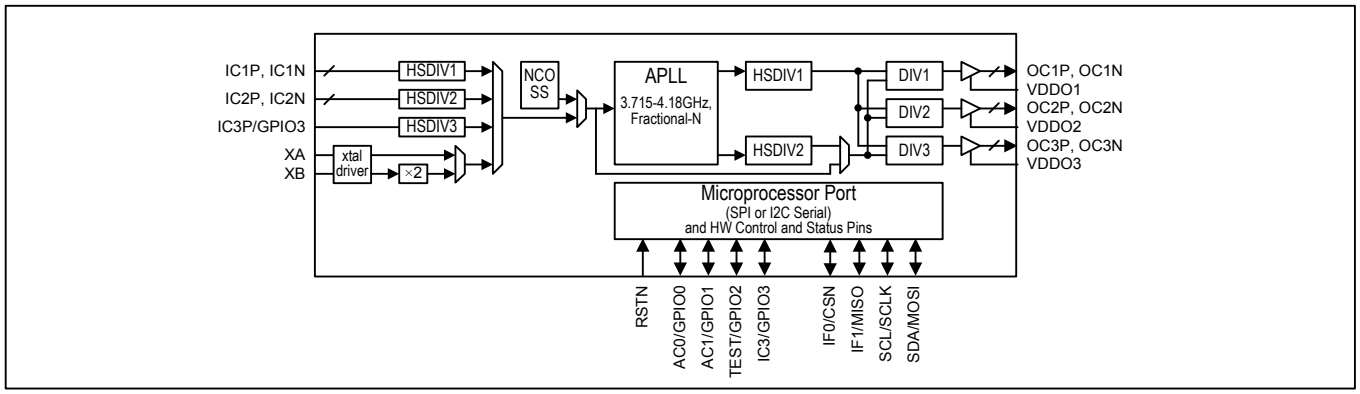

Figure 1 - Functional Block Diagram

1. Application Examples

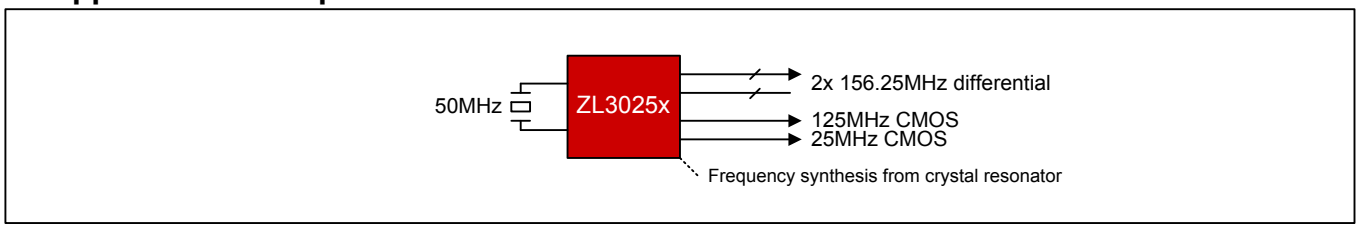

Figure 2 – Ethernet Frequency Synthesis Application

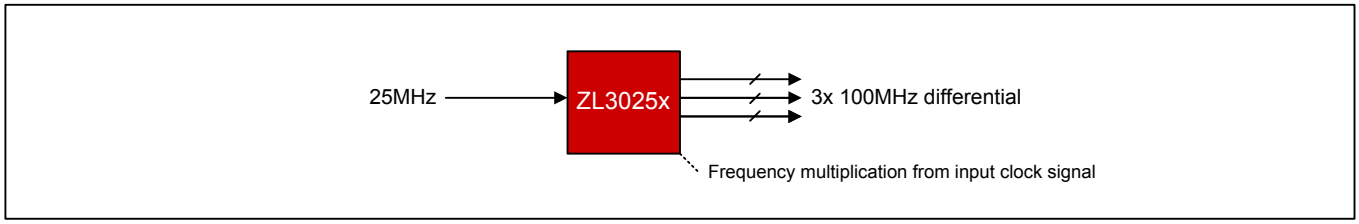

Figure 3 – PCI Express Frequency Multiplication Application

2. Detailed Features

2.1 Input Clock Features

- Four input clocks: one crystal/CMOS, two differential/CMOS, one single-ended/CMOS
- Input clocks can be any frequency from 9.72MHz up to 1250MHz (differential) or 300MHz (CMOS)

2.2 APLL Features

- Very high-resolution fractional scaling (i.e. non-integer multiplication)
- Any-to-any frequency conversion with 0ppm error
- Two high-speed dividers (integers 4 to 15, half divides 4.5 to 7.5)
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components
- Bypass mode supports system testing

2.3 Output Clock Features

- Three low-jitter output clocks
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1035MHz (250MHz max for CMOS and HSTL outputs)
- Output jitter is typically 0.16 to 0.28ps RMS (12kHz to 20MHz integration band)
- In CMOS mode, an additional divider allows the OCxN pin to be an integer divisor of the OCxP pin (Example: OC3P 125MHz, OC3N 25MHz)
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Can produce PCIe clocks (PCIe gen. 1, 2 and 3)
- Sophisticated output-to-output phase alignment
- Per-output phase adjustment with high resolution and unlimited range
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

2.4 General Features

- SPI or I^2C serial microprocessor interface
- Automatic self-configuration at power-up from external (ZL30250) or internal (ZL30251) EEPROM memory; pin control to specify one of four stored configurations
- Numerically controlled oscillator (NCO) mode allows system software to steer frequency with resolution better than 0.01ppb
- Spread-spectrum modulation mode (meets PCI Express requirements)
- Four general-purpose I/O pins each with many possible status and control options
- Reference can be fundamental-mode crystal, low-cost XO or clock signal from elsewhere in the system

2.5 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the ZL30250 or ZL30251 quick and easy
- Generates configuration scripts to be stored in external (ZL30250) or internal (ZL30251) EEPROM
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without a ZL30250 or ZL30251 evaluation board

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