Design Advisory: USB timing marginality on XS1-U series devices

1 Problem

In a small number of cases, xCORE-XS1 USB devices may exhibit a timing marginality which can cause the USB interface to fail to enumerate correctly. This issue is exacerbated by increased core voltage and lower operating temperature. The marginality is caused by a non-optimal delay setting in the XUD module `sc_xud`. Versions of this module between 2.3.0 and 2.6.0 (inclusive) are affected.

2 Resolution

Customers who observe this issue are advised to update their `sc_xud` module to the latest release (version 2.6.1 or higher), which can be downloaded as a zip archive from the following location:

https://www.xmos.com/published/sc_xud.zip?version=all

The USB application affected should be cleaned and rebuilt to ensure the updated `sc_xud` module is used.

3 Impacted XMOS Part Numbers

The following part numbers are covered by this design advisory:

▶ XS1-U6A-64-FB96

▶ XS1-U8A-64-FB96

▶ XS1-U8A-128-FB217

▶ XS1-U10A-128-FB217

▶ XS1-U12A-128-FB217

▶ XS1-U16A-128-FB217

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