PSMN9R5-100BS

N-channel 100 V 9.6 mΩ standard level MOSFET in D2PAK

Rev. 2 — 2 March 2012 Product data sheet

1. Product profile

1.1 General description

Standard level N-channel MOSFET in a D2PAK package qualified to 175C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive

1.3 Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	100	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1	-	-	89	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	211	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 15$ A; $T_j = 25$ °C; see Figure 13	-	8.16	9.6	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 60$ A; $V_{DS} = 50$ V; see Figure 14;see Figure 15	-	23	-	nC
$Q_{G(tot)}$	total gate charge		-	82	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 89$ A; $V_{sup} \leq 100$ V; unclamped; $R_{GS} = 50$ Ω	-	-	177	mJ

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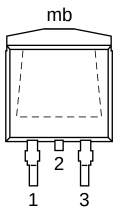
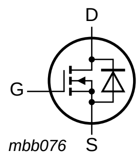
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		



SOT404 (D2PAK)



[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

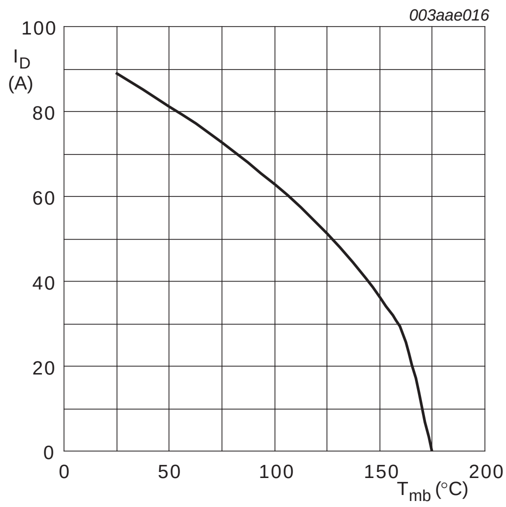
Type number	Package		
	Name	Description	Version
PSMN9R5-100BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

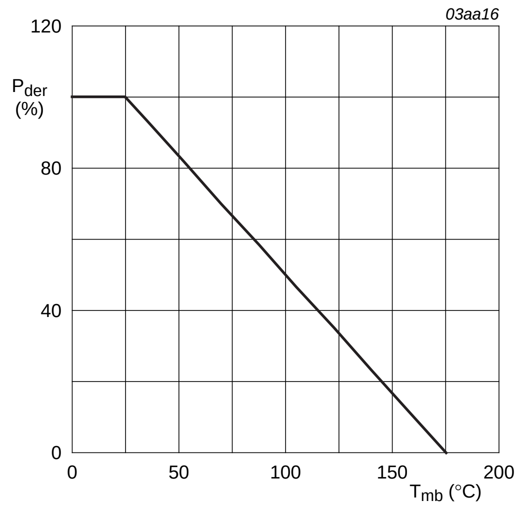
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	100	V
V_{DGR}	drain-gate voltage	$T_j \leq 175$ °C; $T_j \geq 25$ °C; $R_{GS} = 20$ kΩ	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 100$ °C; see Figure 1	-	63	A
		$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1	-	89	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C; see Figure 3	-	355	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	211	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	-	89	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C	-	355	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 89$ A; $V_{sup} \leq 100$ V; unclamped; $R_{GS} = 50$ Ω	-	177	mJ



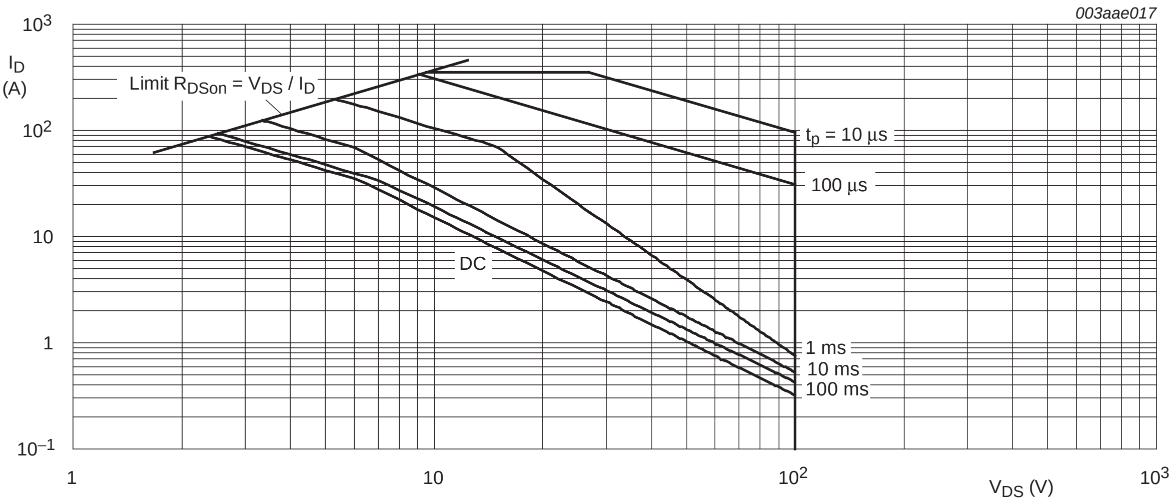
$V_{GS} \geq 10\ V$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25\,^{\circ}C; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.38	0.71	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W

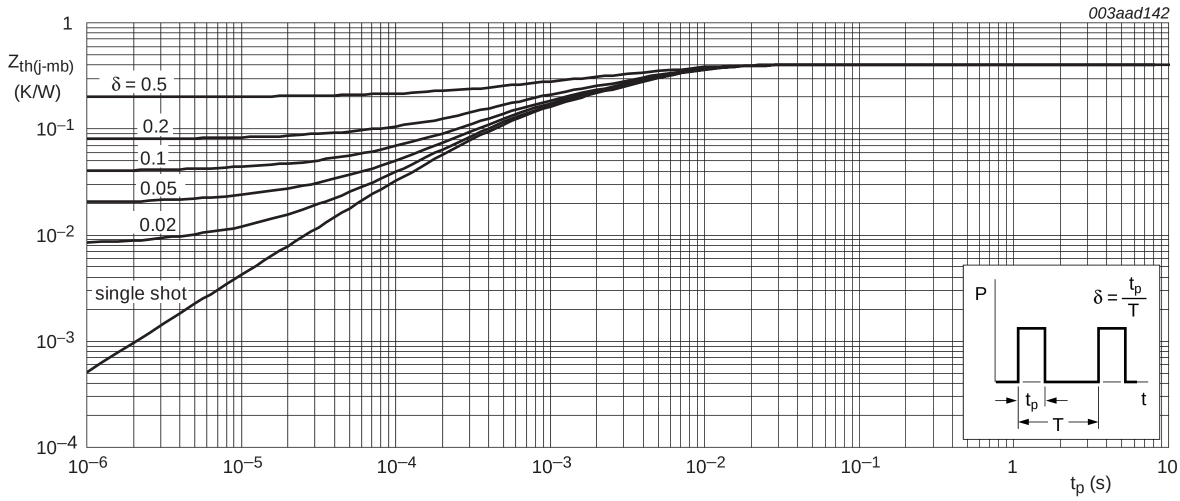


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

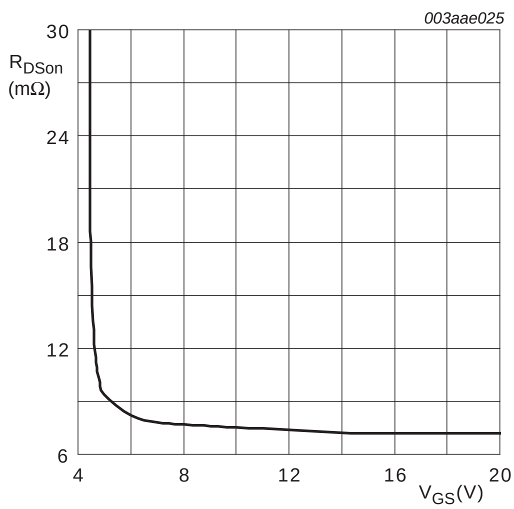
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	90	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 10; see Figure 11	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10; see Figure 11	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 10; see Figure 11	-	-	4.8	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	-	-	100	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	4	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A; T_j = 100 °C; see Figure 12	-	-	17.3	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 175 °C; see Figure 12	-	23.5	27.4	mΩ
		V_{GS} = 10 V; I_D = 15 A; T_j = 25 °C; see Figure 13	-	8.16	9.6	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz	-	0.7	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; see Figure 14	-	67	-	nC
		I_D = 60 A; V_{DS} = 50 V; V_{GS} = 10 V; see Figure 14; see Figure 15	-	82	-	nC
Q_{GS}	gate-source charge		-	21	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	I_D = 60 A; V_{DS} = 50 V; V_{GS} = 3 V; see Figure 14	-	13.1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge	I_D = 60 A; V_{DS} = 50 V; V_{GS} = 10 V; see Figure 14	-	7.8	-	nC
Q_{GD}	gate-drain charge	I_D = 60 A; V_{DS} = 50 V; V_{GS} = 10 V; see Figure 14; see Figure 15	-	23	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	V_{DS} = 50 V; see Figure 14; see Figure 15	-	4.5	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 16	-	4454	-	pF
C_{oss}	output capacitance		-	302	-	pF
C_{rss}	reverse transfer capacitance		-	185	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 0.8 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 4.7 Ω; T_j = 25 °C	-	22	-	ns
t_r	rise time		-	25.2	-	ns
$t_{d(off)}$	turn-off delay time		-	52.2	-	ns
t_f	fall time		-	22.8	-	ns

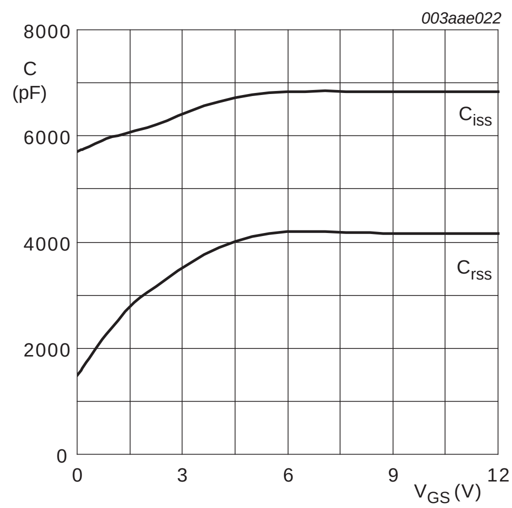
Table 6. Characteristics *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 17	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = 100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V	-	61.5	-	ns
Q_r	recovered charge		-	157	-	nC



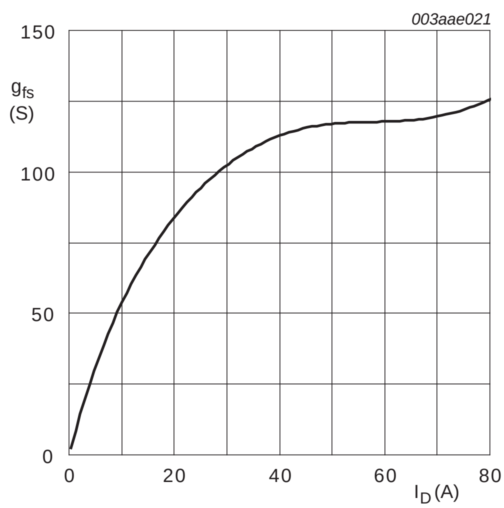
$T_j = 25\ °C; I_D = 20\ A$

Fig 5. Drain-source on-state resistance as a function of gate-source voltage; typical values



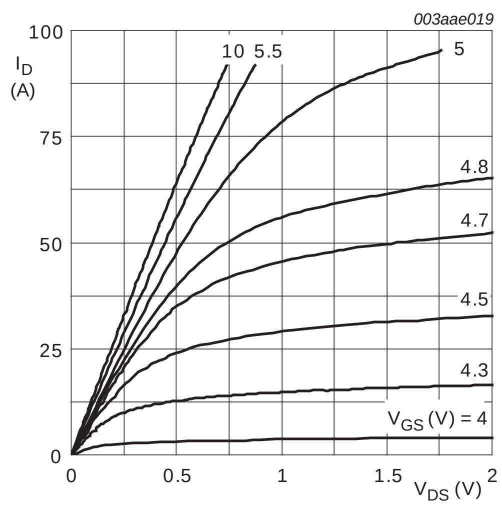
$V_{DS} = 0 V; f = 1 MHz$

Fig 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



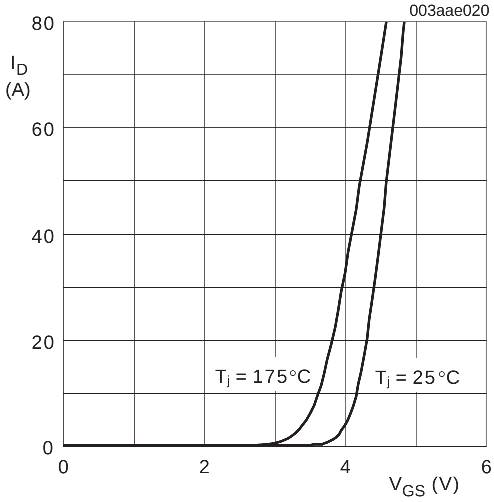
$T_j = 25°C; V_{DS} = 25 V$

Fig 7. Forward transconductance as a function of drain current; typical values



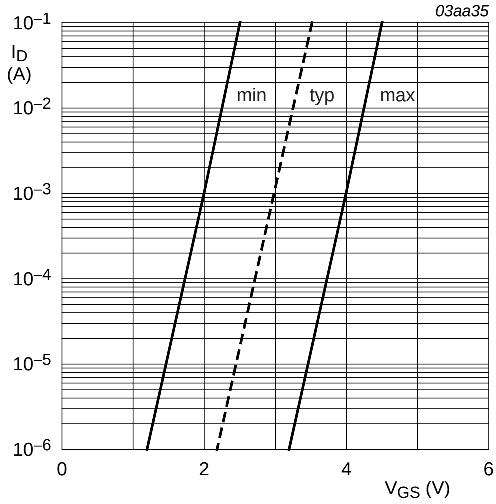
$T_j = 25°C$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



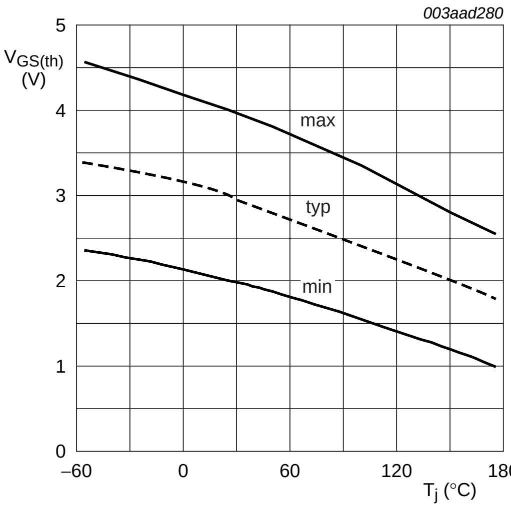
$$V_{DS} > I_D \times R_{DSon}$$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



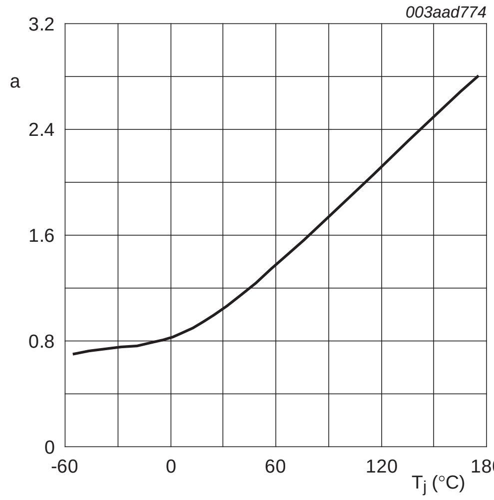
$$T_j = 25\,°C; V_{DS} = 5V$$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



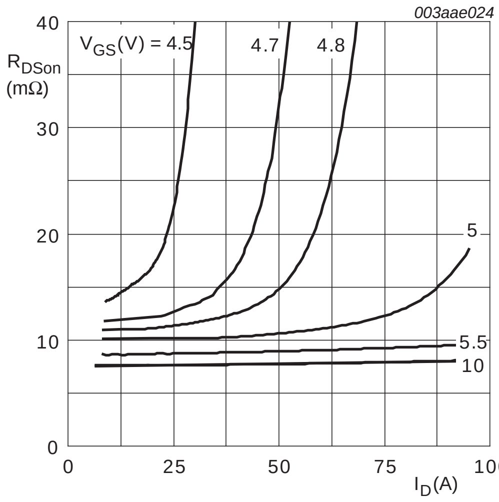
$$I_D = 1\ \mathrm{mA};\ V_{DS} = V_{GS}$$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25\,°C$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

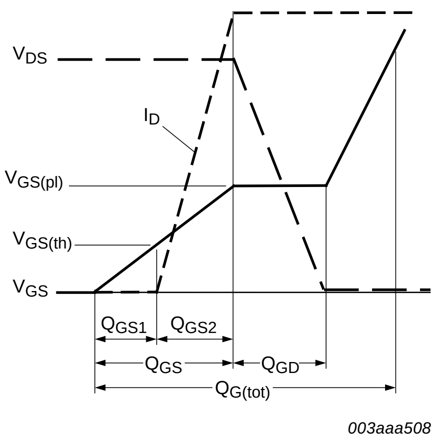
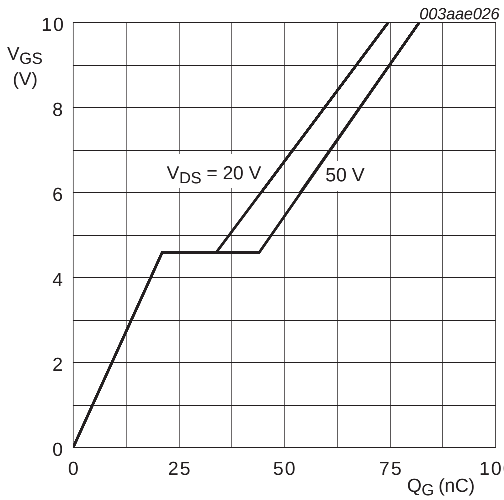
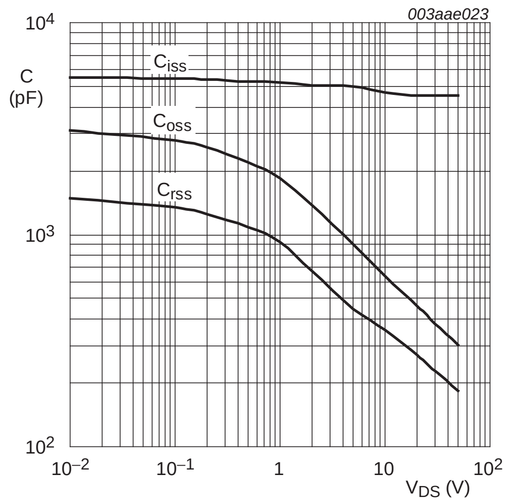


Fig 14. Gate charge waveform definitions



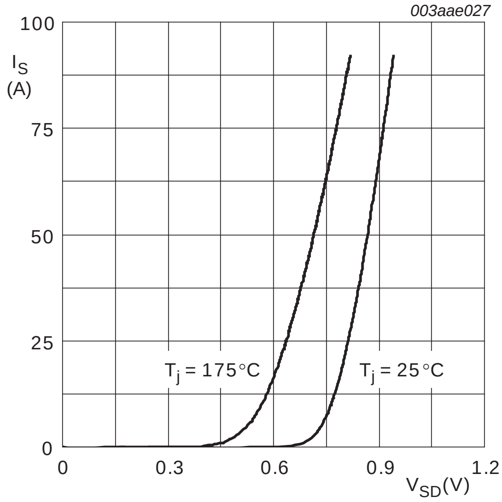
$T_j = 25\ °C$; $I_D = 60\ A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\ V$; f = 1 MHz

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

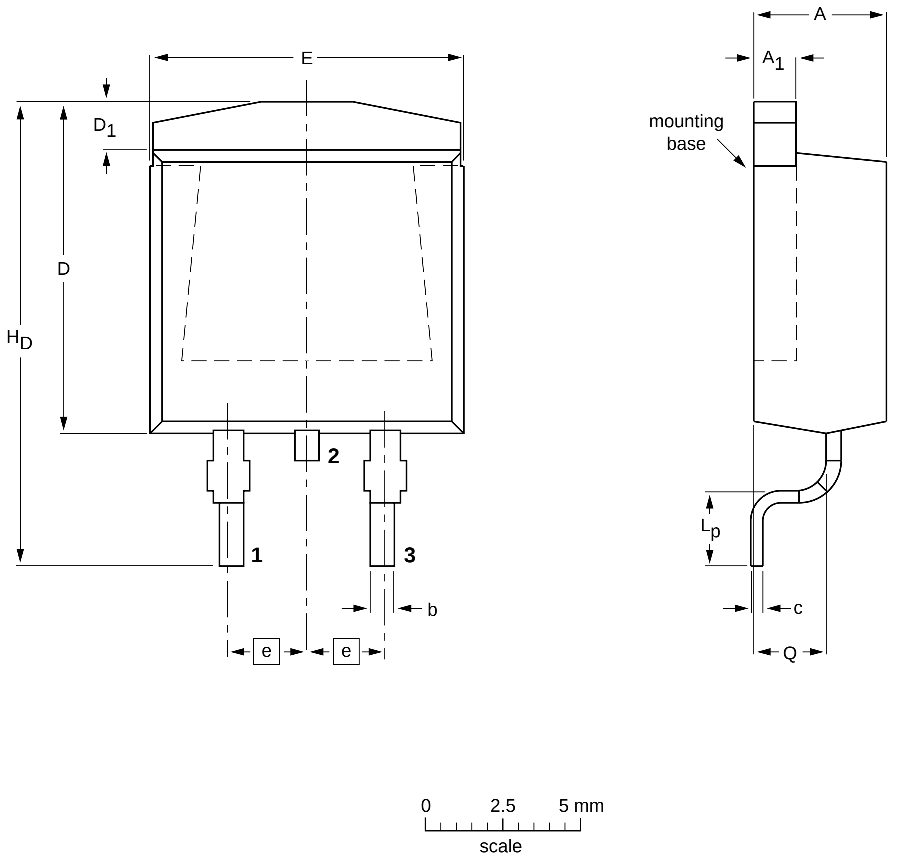


$V_{GS} = 0V$

Fig 17. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig 18. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN9R5-100BS v.2	20120302	Product data sheet	-	PSMN9R5-100BS v.1
Modifications:	• Status changed from objective to product. • Various changes to content.			
PSMN9R5-100BS v.1	20111025	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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For sales office addresses, please send an email to:salesaddresses@nexperia.com

11. Contents

Date of release: 02 March 2012