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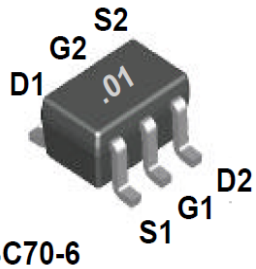
April 2016

FDG6301N_F085

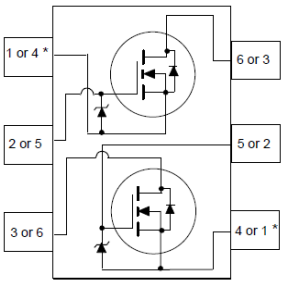
Dual N-Channel, Digital FET

Features

- 25 V, 0.22 A continuous, 0.65 A peak.
- $R_{DS(ON)}$ = 4 Ω @ V_{GS}= 4.5 V,
- $R_{DS(ON)}$ = 5 Ω @ V_{GS}= 2.7 V.
- Very low level gate drive requirements allowing directop-eration in 3 V circuits ($V_{GS(th)}$ < 1.5 V).
- Gate-Source Zener for ESD ruggedness (>6kV Human Body Model).
- Compact industry standard SC70-6 surface mount package.
- Qualified to AEC Q101
- RoHS Compliant



SC70-6



Applications

- Low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	8	V
I_D	Drain Current Continuous	0.22	A
	Pulsed	0.65	
P_D	Power Dissipation	0.3	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model(100 pF / 1500 W)	6.0	kV
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	415	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDG6301N	FDG6301N_F085	SC70-6	7”	8mm	3000 units

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. $R_{\theta JA}$ = 415 °C/W on minimum pad mounting on FR-4 board in still air

2: A suffix as “…F085P” has been temporarily introduced in order to manage a double source strategy as Fairchild has officially announced in Aug 2014.

3: Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%.

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	25	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 20V, V_{GS} = 0V, T_J = 55°C	-	-	10	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	0.65	0.85	1.5	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 0.22A, V_{GS}= 4.5V	-	2.6	4	Ω
		I_D = 0.19A, V_{GS}= 2.7V	-	3.7	5	Ω
		I_D = 0.22A, V_{GS}= 4.5V, T_J = 125°C	-	5.3	7	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5V, V_{DS} = 5V	0.22	-	-	
g_{FS}	Forward Transconductance	I_D = 0.22A, V_{DS}= 5V	-	0.2	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz	-	9.5	-	pF
C_{oss}	Output Capacitance		-	6	-	pF
C_{rss}	Reverse Transfer Capacitance		-	1.3	-	pF
$Q_{g(TOT)}$	Total Gate Charge at -4.5V	V_{GS} = 0 to 4.5V, V_{DD} = 5V, I_D = 0.22A	-	0.29	0.4	nC
Q_{gs}	Gate to Source Gate Charge		-	0.12	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge		-	0.03	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 5V, I_D = 0.5A, V_{GS} = 4.5V, R_{GEN} = 50Ω	-	5	10	ns
t_r	Rise Time		-	4.5	10	ns
$t_{d(off)}$	Turn-Off Delay Time		-	4	8	ns
t_f	Fall Time		-	3.2	7	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Source Current		-	-	0.25	A
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 0.25A, V_{GS} = 0V	-	0.8	1.2	V

Typical Characteristics

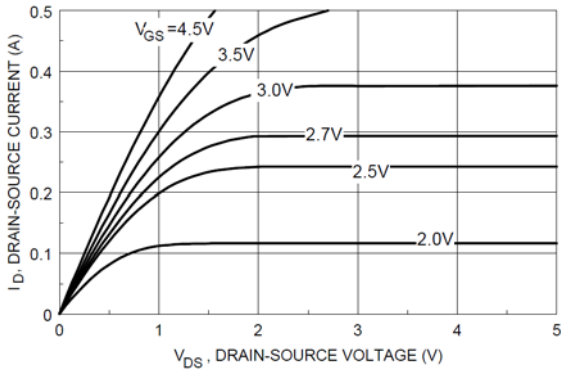


Figure 1. On-Region Characteristics.

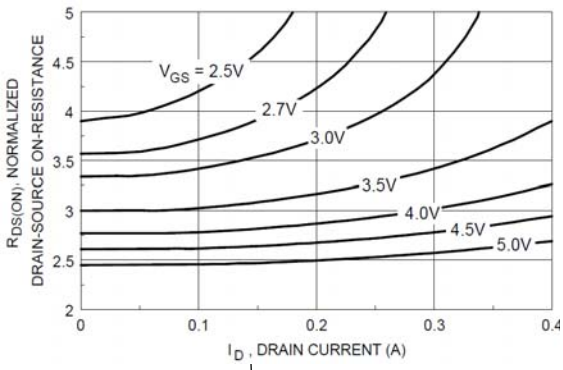


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

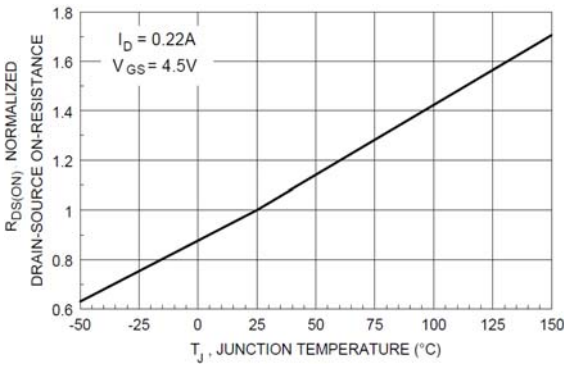


Figure 3. On-Resistance Variation with Temperature.

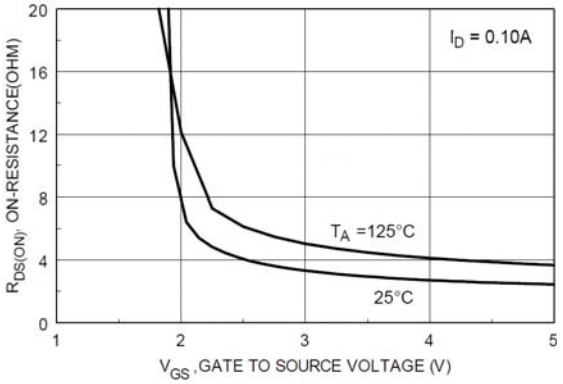


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

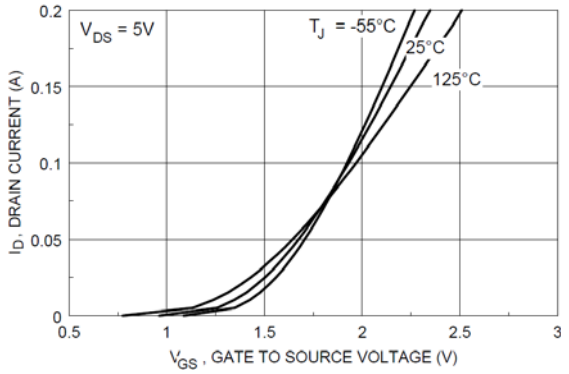


Figure 5. Transfer Characteristics.

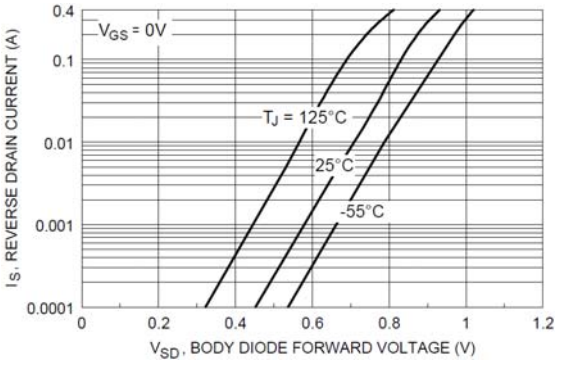


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

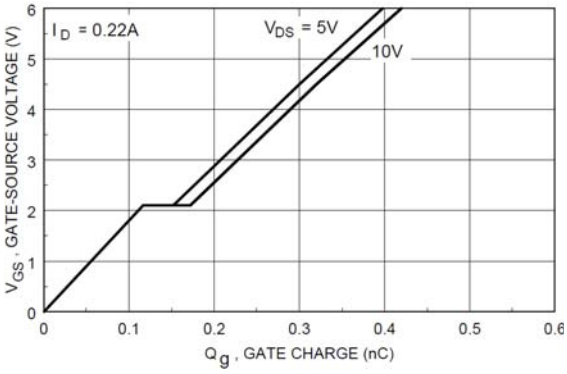


Figure 7. Gate Charge Characteristics.

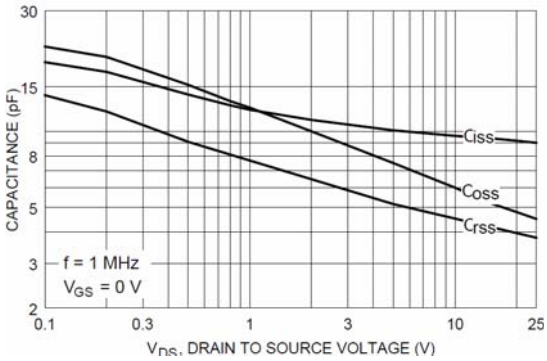


Figure 8. Capacitance Characteristics.

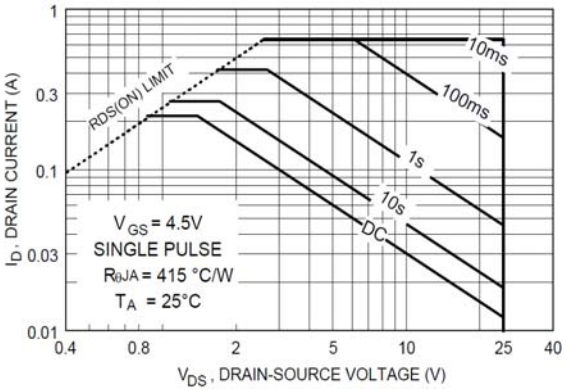


Figure 9. Maximum Safe Operating Area.

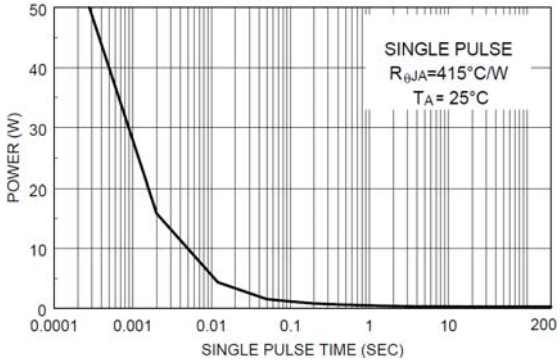


Figure 10. Single Pulse Maximum Power Dissipation.

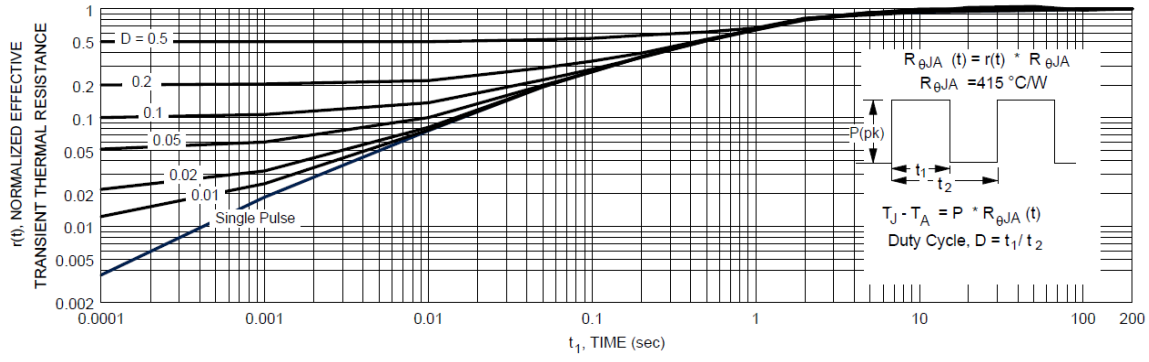
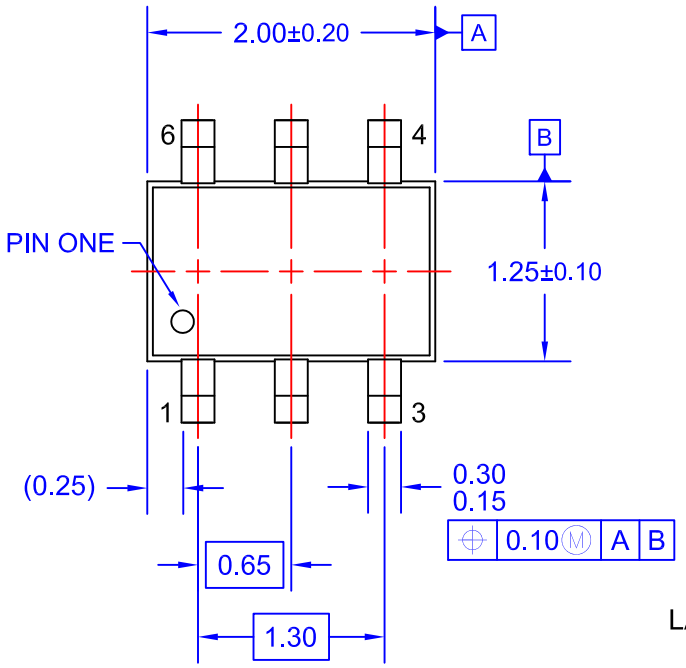
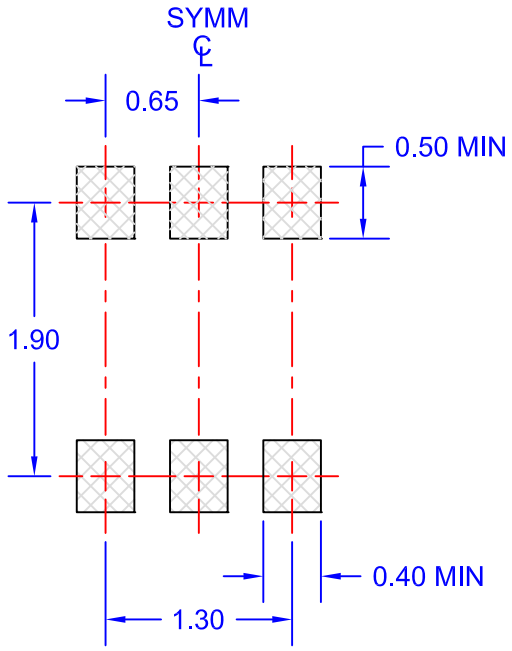
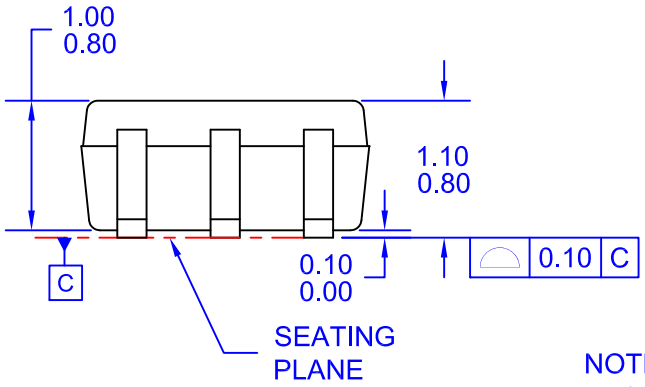


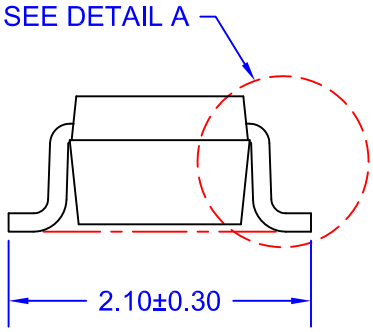
Figure 11. Transient Thermal Response Curve.





LAND PATTERN RECOMMENDATION





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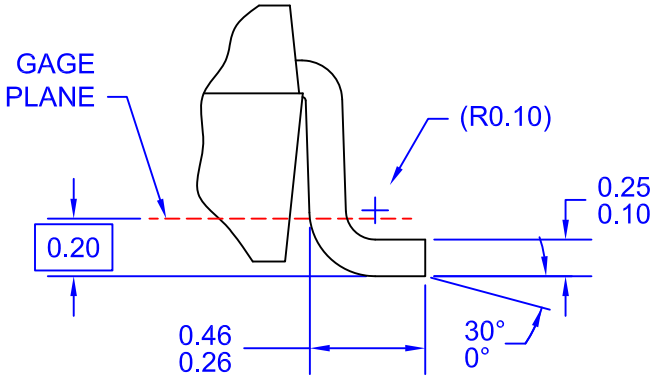
A) THIS PACKAGE CONFORMS TO EIAJ SC-88, 1996.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009

E) DRAWING FILENAME: MKT-MAA06AREV7



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