Pb-Free and RoHS Compliant

October 25, 2005 FN4115.4

Triple 8-Bit, 40MSPS, RGB, 3-Channel D/A Converter

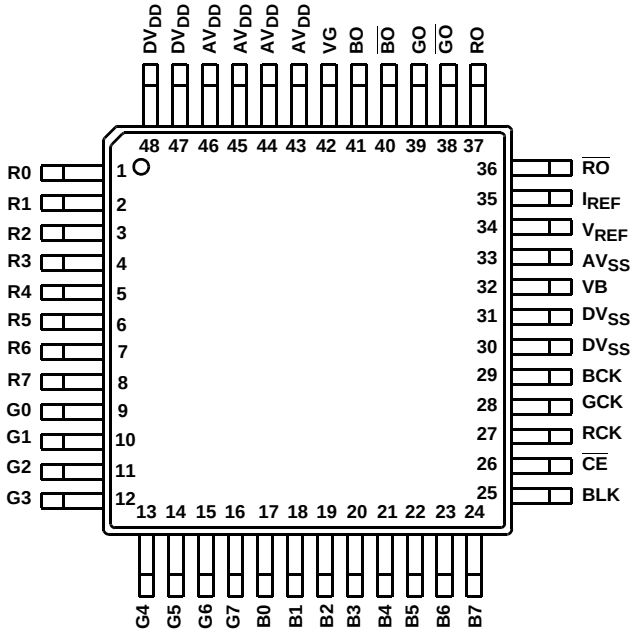
The HI1178 is a triple 8-bit, high-speed, CMOS D/A converter designed for video band use. It has three separate, 8-bit, pixel inputs, one each for red, green, and blue video data. A single 5.0V power supply and pixel clock input is all that is required to make the device operational. A bias voltage generator is internal. Each channel clock input can be controlled individually, or connected together as one. The HI1178 also has BLANK video control signal.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI1178JCQ	-40 to 85	48 Ld MQFP	Q48.12x12-S

Pinout

HI1178
(MQFP)
TOP VIEW



Features

- Resolution . . . . . Triple 8-Bit
- Maximum Conversion Speed 40MHz
- RGB 3-Channel Input/Output
- Differential Linearity Error . . . . . +0.3 LSB
- Low Power Consumption . . . . . 240mW (200Ω Load for $2V_{P-P}$ Output)
- Single Power Supply . . . . . +5V
- Low Glitch Noise
- Direct Replacement for Sony CXD1178

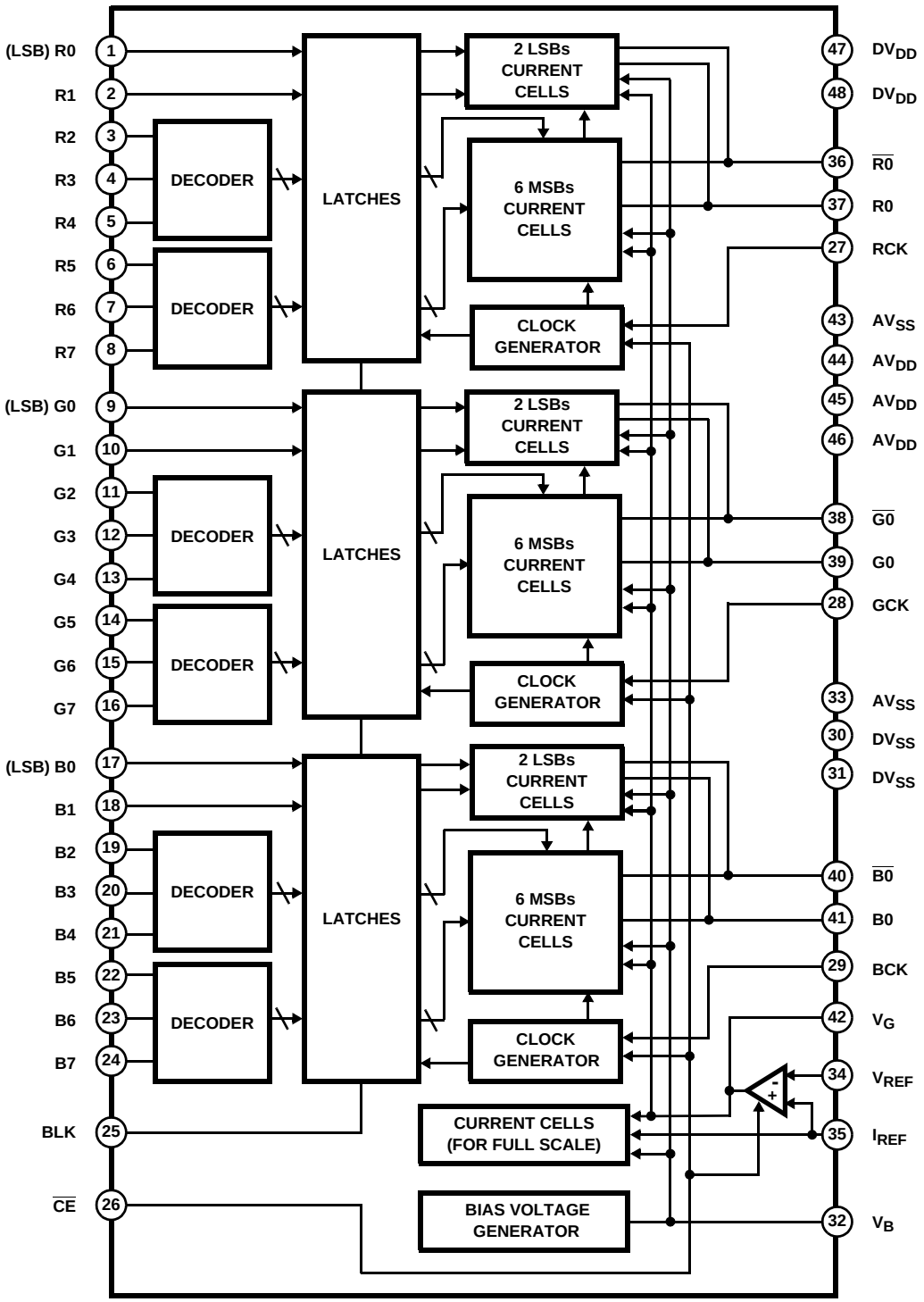
Applications

- Digital TV
- Graphics Display
- High Resolution Color Graphics
- Video Reconstruction
- Instrumentation
- Image Processing
- I/Q Modulation

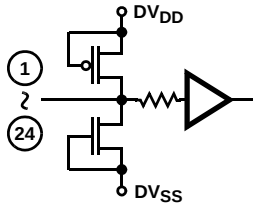
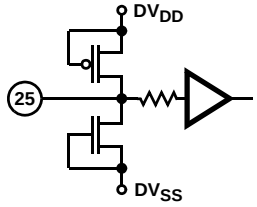
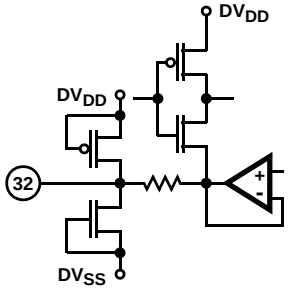
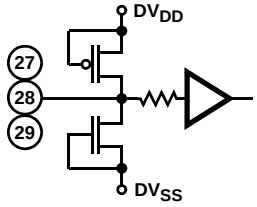
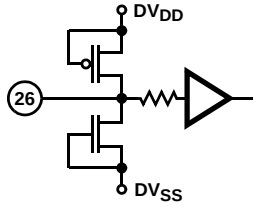
Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

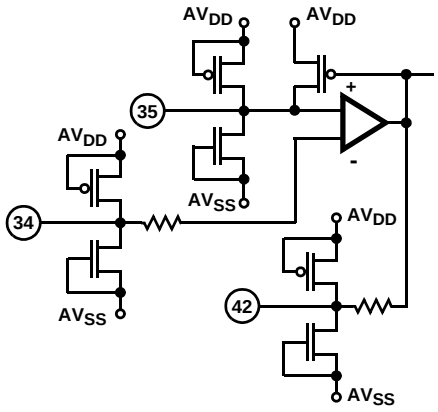
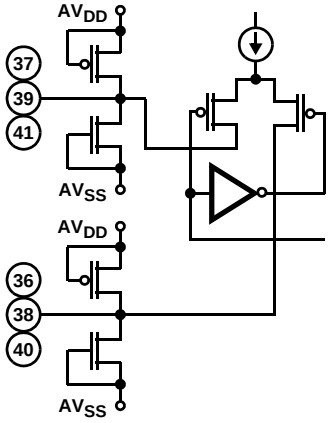
Functional Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 8	R0 to R7		Digital input.
9 to 16	G0 to G7		
17 to 24	B0 to B7		
25	BLK		Blanking pin. No signal at “H” (Output 0V). Output condition at “L”.
32	V_B		Connect a capacitor of about 0.1µF.
27	RCK		Clock pin. Moreover all input pins are TTL-CMOS compatible.
28	CLK		
29	BCK		
30, 31	DV_{SS}		Digital GND.
33	AV_{SS}		Analog GND.
26	$\overline{CE}$		Chip enable pin. No signal (Output 0V) at “H” and minimizes power consumption.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
35	I_{REF}		Connect a resistance 16 times “16R” that of output resistance value “R”.
34	V_{REF}		Set full scale output value.
42	V_G		Connect a capacitor of about 0.1μF.
43 to 46	AV_{DD}		Analog V_{DD}.
37	RO		Current output pin. Voltage output can be obtained by connecting a resistance.
39	GO		
41	BO		
36	$\overline{RO}$		Inverted current output pin. Normally dropped to analog GND.
38	$\overline{GO}$		
40	$\overline{BO}$		
47, 48	DV_{DD}		Digital V_{DD}.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Input Voltage (V_{IN}). . . . . V_{DD} to V_{SS}
Output Current (I_{OUT}) . . . . . V_{DD} to V_{SS}
Digital Input Voltage (CLK) . . . . . 0mA to 15mA
(Every Each Channel)

Operating Conditions

Temperature Range (T_{OPR}) . . . . . -40^oC to 85^oC
Supply Voltage
AV_{DD}, AV_{SS} . . . . . 4.75V to 5.25V
DV_{DD}, DV_{SS} . . . . . 4.75V to 5.25V
Reference Input Voltage (V_{REF}) 2V
Clock Pulse Width
t_{PW1} . . . . . .12.5ns (Min)
t_{PW0} . . . . . .12.5ns (Min)

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
MQFP Package 94
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range (T_{STG}) . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications f_{CLK} = 40MHz, V_{DD} = 5V, R_{OUT} = 200Ω, V_{REF} = 2.0V, $T_A = 25^oC$

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		n		-	8	-	bit
Maximum Conversion Speed		f_{MAX}		40	-	-	MSPS
Linearity Error		E_L		-2.5	-	2.5	LSB
Differential Linearity Error		E_D		-0.3	-	0.3	LSB
Full Scale Output Voltage		V_{FS}		1.8	2.0	2.2	V
Full Scale Output Ratio (Note 1)		F_{SR}		0	1.5	3	%
Full Scale Output Current		I_{FS}		-	10	15	mA
Offset Output Voltage		V_{OS}		-	-	1	mV
Power Supply Current		I_{DD}	14.3MHz, at Color Bar Data Input	-	-	48	mA
Digital Input Current	H Level	I_{IH}		-	-	5	μA
	L Level	I_{IL}		-5	-	-	μA
Set Up Time		t_S		5	-	-	ns
Hold Time		t_H		10	-	-	ns
Propagation Delay Time		t_{PD}		-	10	-	ns
Glitch Energy		GE	R_{OUT} = 75Ω	-	30	-	pV/s
Crosstalk		CT	1MHz Sine Wave Output	-	57	-	dB

NOTE:

1. Full scale output ratio = $\left| \frac{\text{Full Scale Voltage of Channel}}{\text{Average of the Full Scale Voltage of the Channels}} - 1 \right| \times 100(\%)$

I/O Chart (When Full Scale Output Voltage at 2.00V)

INPUT CODE								OUTPUT CODE
MSB							LSB	
1	1	1	1	1	1	1	1	2.0V
				•				
				•				
				•				
1	0	0	0	0	0	0	0	1.0V
				•				
				•				
				•				
0	0	0	0	0	0	0	0	0V

Timing Diagram

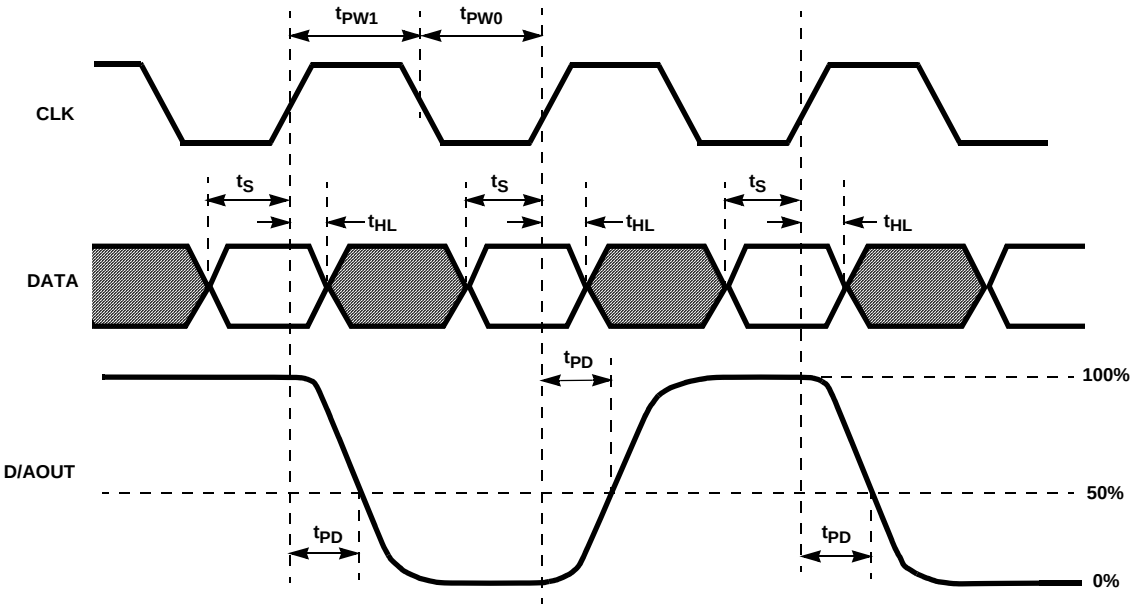


FIGURE 1.

Test Circuits

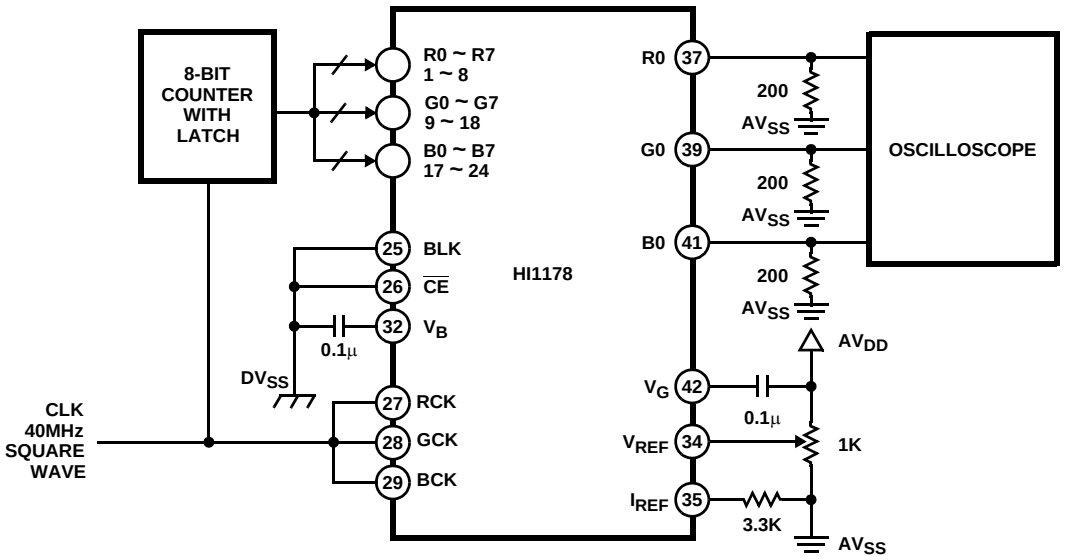


FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT

Test Circuits (Continued)

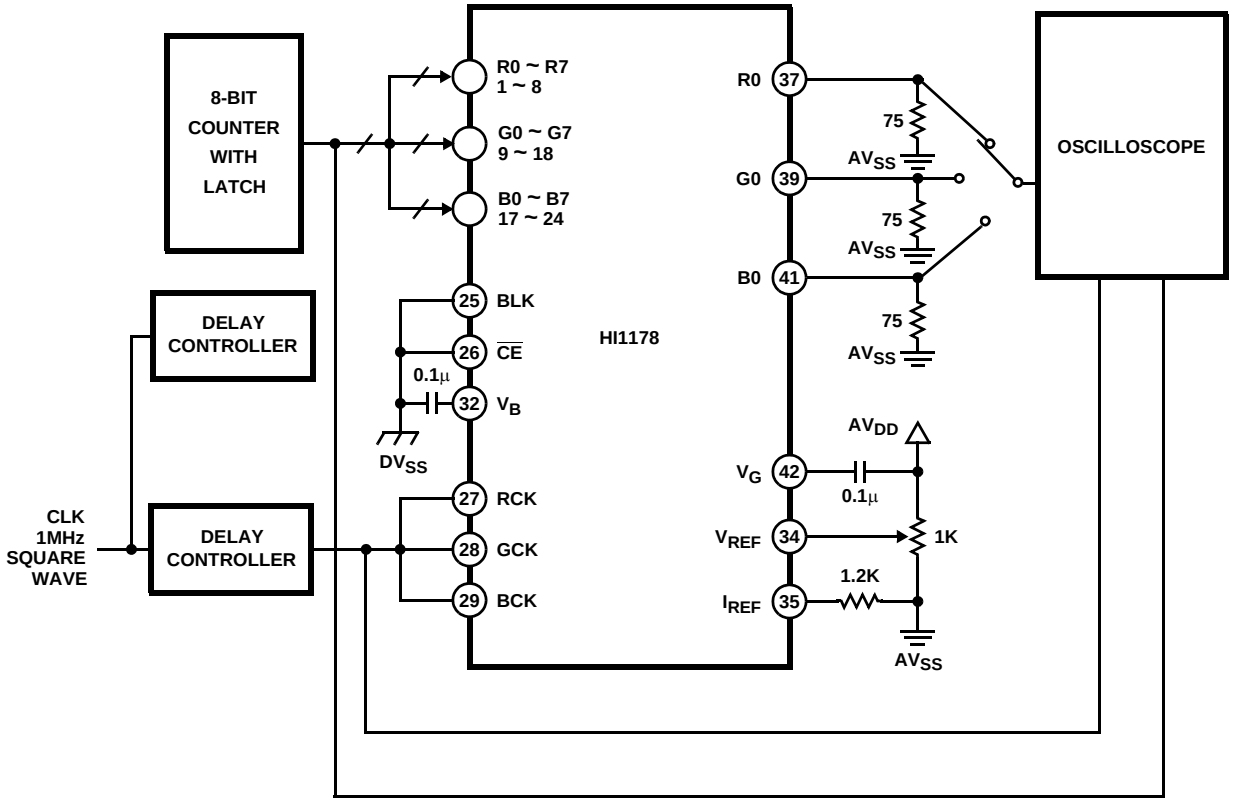


FIGURE 3. SETUP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

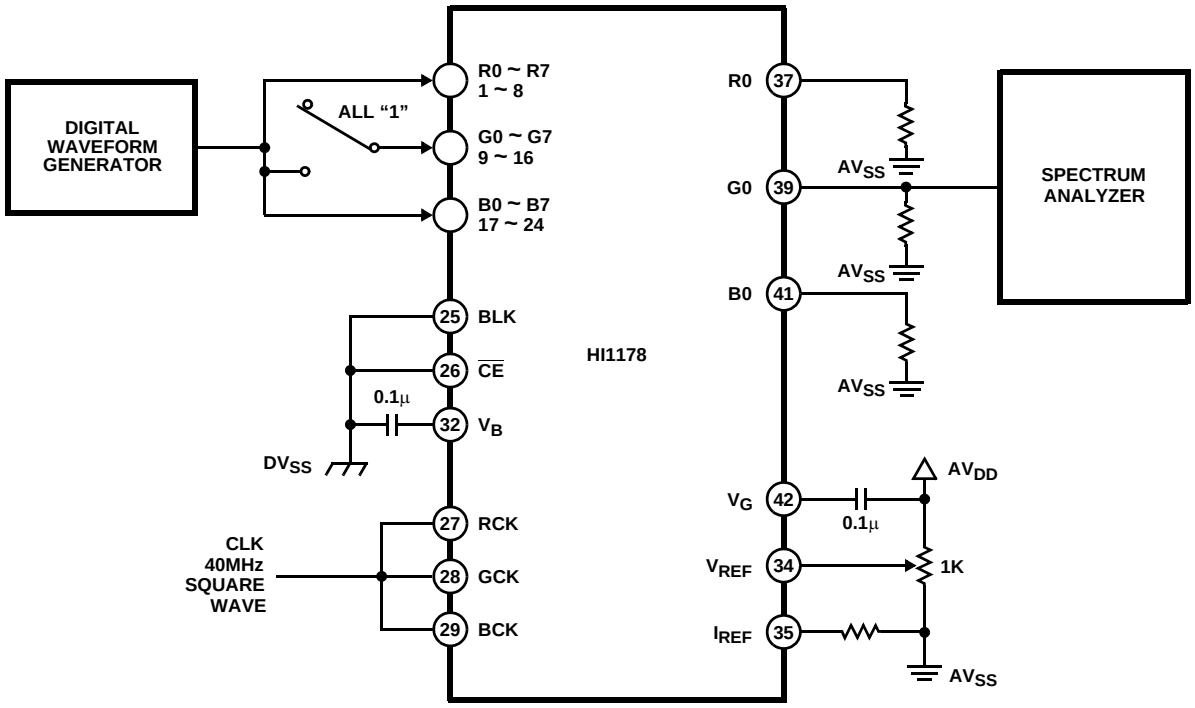


FIGURE 4. CROSSTALK TEST CIRCUIT

Test Circuits (Continued)

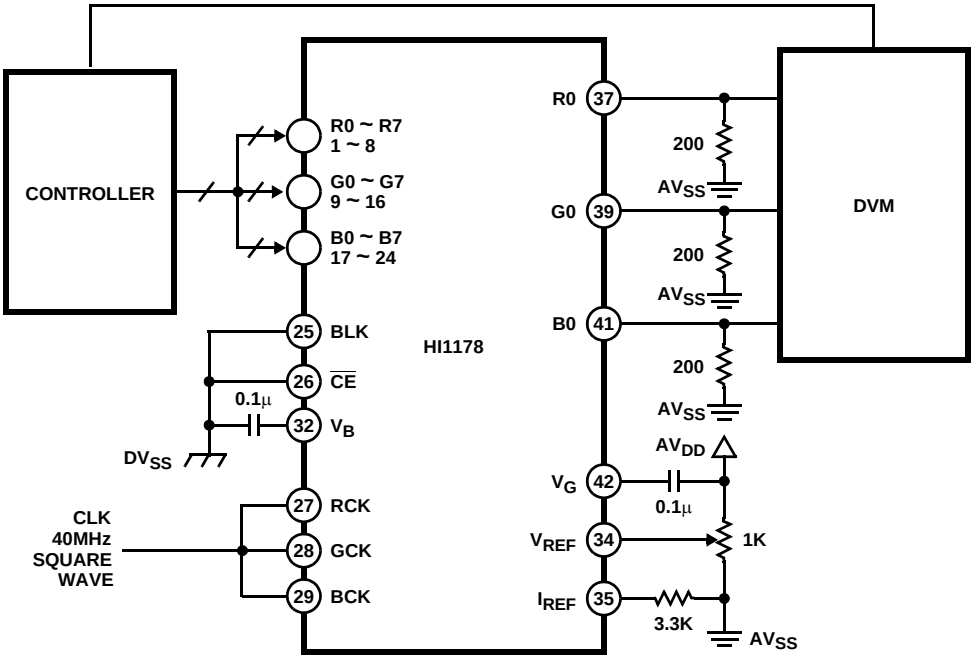


FIGURE 5. DC CHARACTERISTICS TEST CIRCUIT

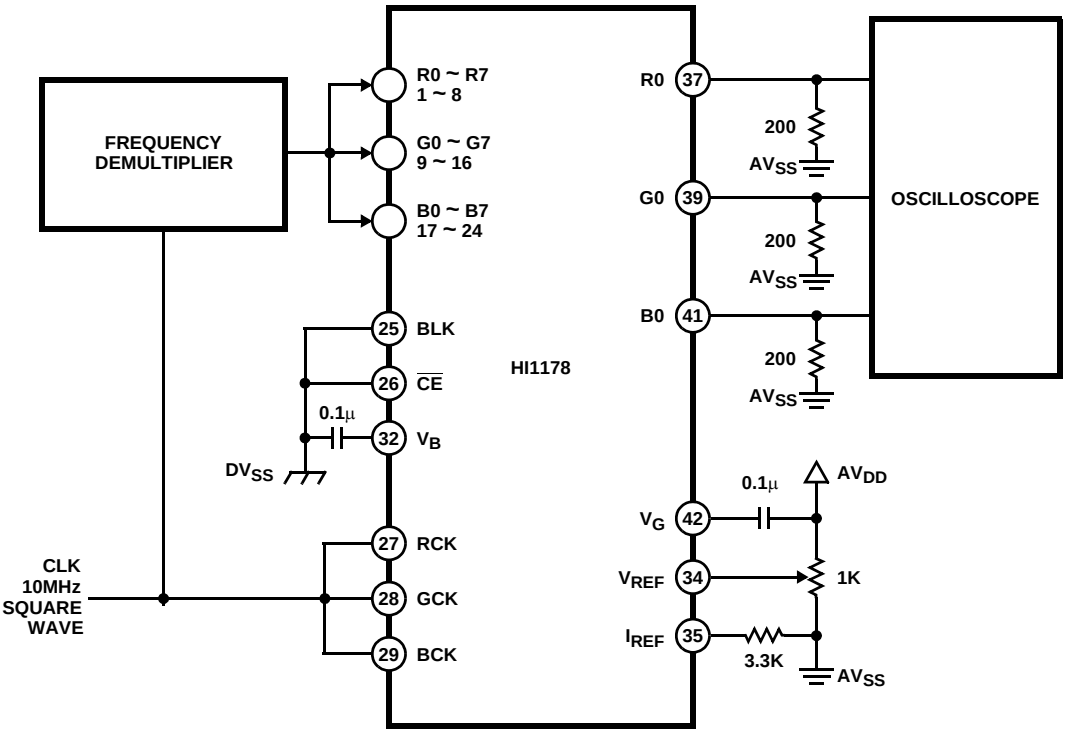


FIGURE 6. PROPAGATION DELAY TIME TEST CIRCUIT

Typical Performance Curves

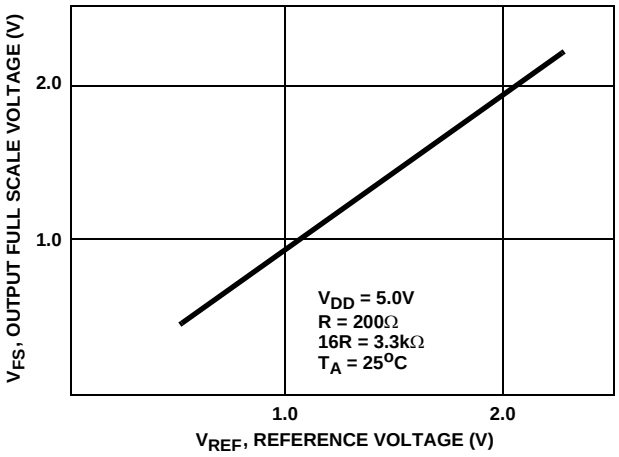


FIGURE 7. OUTPUT FULL SCALE VOLTAGE vs REFERENCE VOLTAGE

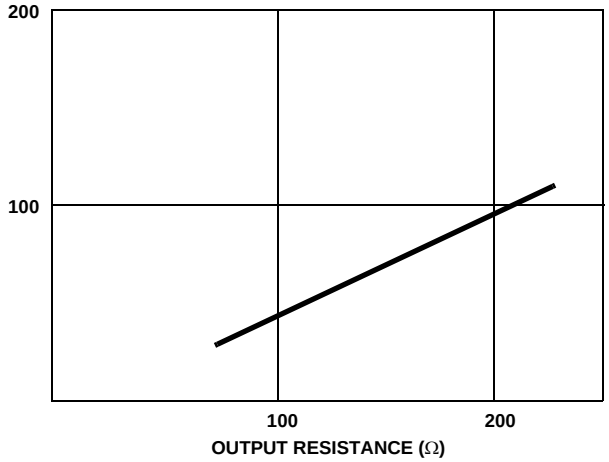


FIGURE 8. GLITCH ENERGY vs OUTPUT RESISTANCE

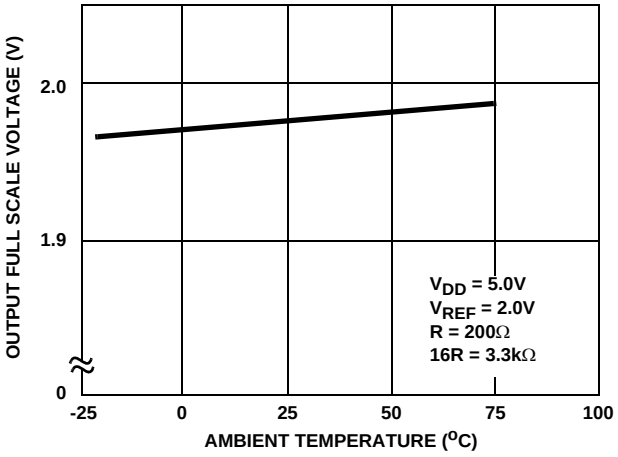


FIGURE 9. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

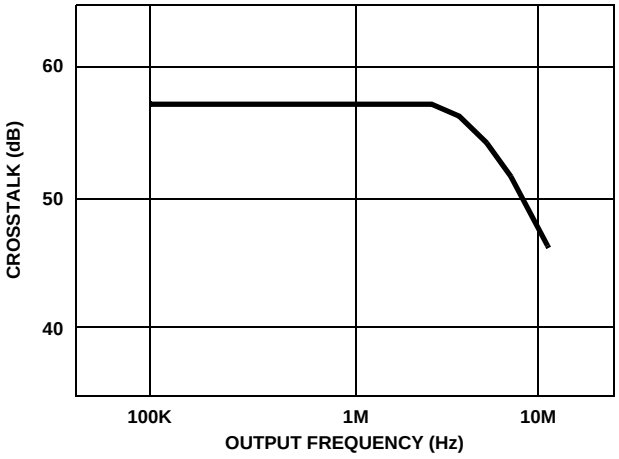


FIGURE 10. CROSSTALK vs OUTPUT FREQUENCY

Application Circuit

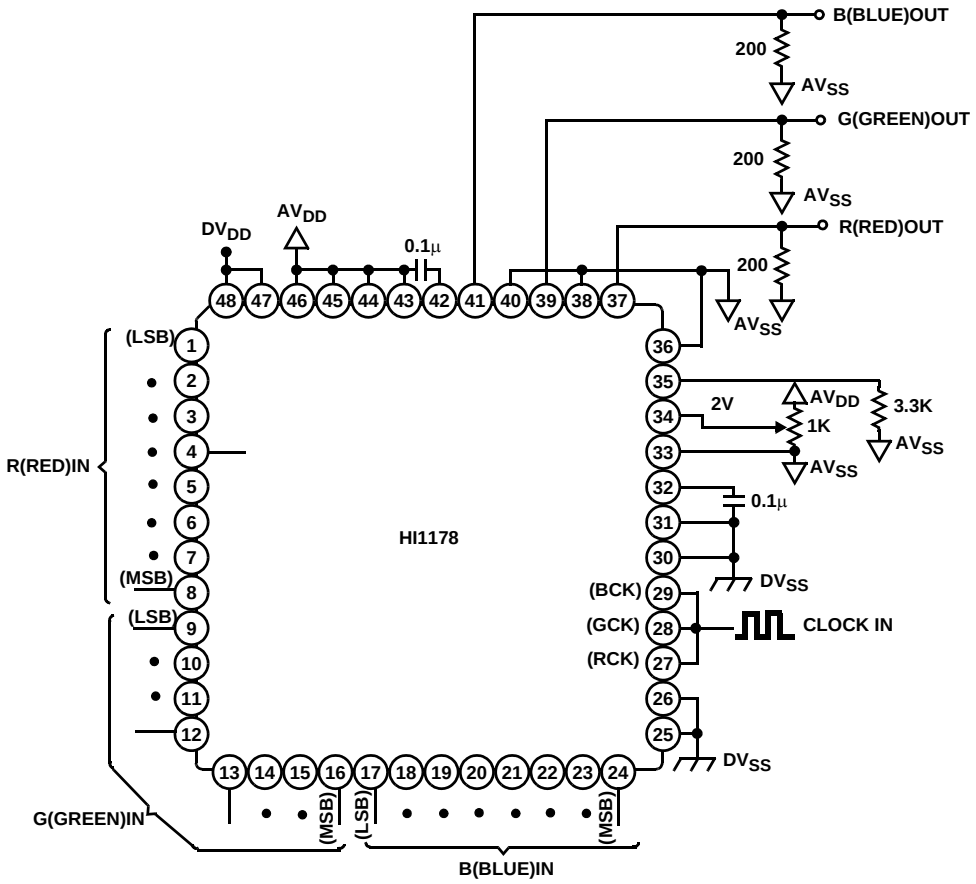


FIGURE 11.

Notes On Operation

- How to select the output resistance

  The HI1178 is a current-output D/A converter. To obtain the output voltage, connect the resistance to IO pin (RO, GO, BO). For specifications we have:

Output Full Scale Voltage	V_{FS} = less than 2.0 [V]
Output Full Scale Current	I_{FS} = less than 15 [mA]

  Calculate the output resistance value from the relation of $V_{FS} = I_{FS}$ X R. Also, 16 times resistance of the output resistance is connected to reference current pin I_{REF}. In some cases, however, this turns out to be a value that does not actually exist. In such a case a value close to it can be used as a substitute. Here please note that V_{FS} becomes $V_{FS} = V_{REF}$ X 16R/R'. R is the resistance connected to IO while R' is connected to I_{REF}. Increasing the resistance value can curb power consumption. On the other hand glitch energy and data settling time will inversely increase. Set the most suitable value according to the desired application.

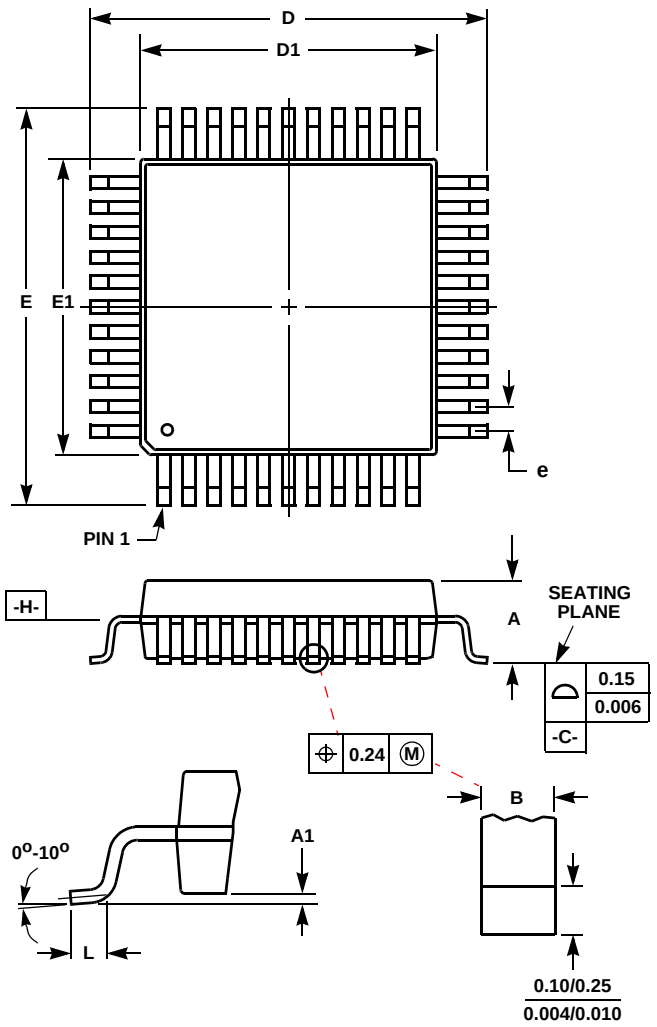
- Phase Relation Between Data and Clock

  To obtain the expected performance as a D/A converter, it is necessary to set properly the phase relation between data and clock applied from the exterior. Be sure to satisfy the provisions of the set up time (t_S) and hold time (t_H) as stipulated in the Electrical Characteristics.

- V_{DD}, V_{SS}

  To reduce noise effects separate analog and digital systems in the device periphery. For V_{DD} pins, both digital and analog, bypass respective GNDs by using a ceramic capacitor of 0.1µF, as close as possible to the pin.

Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q48.12x12-S

48 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.081	0.100	2.05	2.55	-
A1	0.000	0.011	0.00	0.30	-
B	0.008	0.017	0.20	0.45	5
D	0.587	0.618	14.90	15.70	2
D1	0.469	0.488	11.90	12.40	3, 4
E	0.587	0.618	14.90	15.70	2
E1	0.469	0.488	11.90	12.40	3, 4
L	0.028	0.043	0.70	1.10	-
N	48		48		6
e	0.032 BSC		0.80 BSC		-

Rev. 0 2/96

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. “N” is the number of terminal positions.