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74ABT16952
16-Bit Registered Transceiver with 3-STATE Outputs

General Description

The ABT16952 is a 16-bit registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-STATE output enable signals are provided for each register. The output pins are guaranteed to source 32 mA and to sink 64 mA.

Features

■ Separate clock, clock enable and 3-STATE output enable provided for each register

■ A and B output sink capability of 64 mA source capability of 32 mA

■ Guaranteed latchup protection

■ High impedance glitch free bus loading during entire power up and power down cycle

■ Nondestructive hot insertion capability

Ordering Code:

Order Number	Package Number	Package Description
74ABT16952CSSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16952CMTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the letter suffix "X" to the ordering code.

Pin Descriptions

Pin Names	Description
A_0–A_{15}	Data Register A Inputs/
	B-Register 3-STATE Outputs
B_0–B_{15}	Data Register B Inputs/
	A-Register 3-STATE Outputs
$CPAB_n$, $CPBA_n$	Clock Pulse Inputs
$\overline{CEA}_n$, $\overline{CEB}_n$	Clock Enable
$\overline{OEAB}_n$, $\overline{OEBA}_n$	Output Enable Inputs
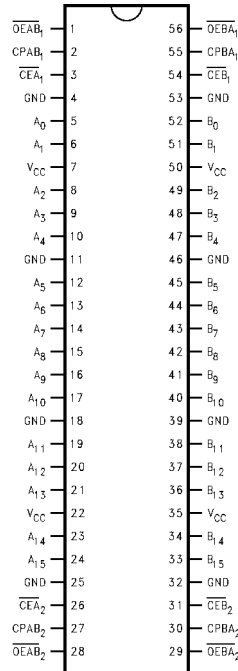
Output Control

$\overline{OE}$	Internal Q	Output	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

Register Function Table

(Applies to A or B Register)

Inputs			Internal	Function
D	CP	$\overline{CE}$	Q	
X	X	H	NC	Hold Data
L	⤒	L	L	Load Data
H	⤒	L	H	

H = HIGH Voltage Level   Z = HIGH Impedance
L = LOW Voltage Level   ⤒ = LOW-to-HIGH Transition
X = Immaterial   NC = No Change

Connection Diagram

$\overline{OEAB}_1$	1	56	$\overline{OEBA}_1$
$CPAB_1$	2	55	$CPBA_1$
$\overline{CEA}_1$	3	54	$\overline{CEB}_1$
GND	4	53	GND
A_0	5	52	B_0
A_1	6	51	B_1
V_{CC}	7	50	V_{CC}
A_2	8	49	B_2
A_3	9	48	B_3
A_4	10	47	B_4
GND	11	46	GND
A_5	12	45	B_5
A_6	13	44	B_6
A_7	14	43	B_7
A_8	15	42	B_8
A_9	16	41	B_9
A_{10}	17	40	B_{10}
GND	18	39	GND
A_{11}	19	38	B_{11}
A_{12}	20	37	B_{12}
A_{13}	21	36	B_{13}
V_{CC}	22	35	V_{CC}
A_{14}	23	34	B_{14}
A_{15}	24	33	B_{15}
GND	25	32	GND
$\overline{CEA}_2$	26	31	$\overline{CEB}_2$
$CPAB_2$	27	30	$CPBA_2$
$\overline{OEAB}_2$	28	29	$\overline{OEBA}_2$

Block Diagram

n for either byte 1 or byte 2

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.
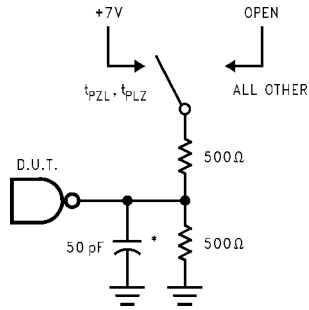
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	2.5			V	Min	I_{OH} = −3 mA (A_n, B_n)
		2.0					I_{OH} = −32 mA (A_n, B_n)
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA (A_n, B_n)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current			1	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) (Note 4)
				1			V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current			−1	µA	Max	V_{IN} = 0.5V (Non-I/O Pins) (Note 4)
				−1			V_{IN} = 0.0V (Non-I/O Pins)
$I_{IH} + I_{OZH}$	Output Leakage Current			10	µA	0V–5.5V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
$I_{IL} + I_{OZL}$	Output Leakage Current			−10	µA	0V–5.5V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEA}$ or $\overline{OEB}$ = 2.0V
I_{OS}	Output Short-Circuit Current	−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	µA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCH}	Power Supply Current			1.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current			60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current			1.0	mA	Max	Outputs 3-STATE; All Others GND
I_{CCT}	Additional I_{CC}/Input			2.5	mA	Max	V_I = V_{CC} − 2.1V; All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load (Note 4)			0.18	mA/ MHz	Max	Outputs OPEN $\overline{OEA}$ or $\overline{OEB}$ = GND, Non-I/O = GND or V_{CC} One Bit toggling, 50% duty cycle (Note 3)

Note 3: For 8-bit toggling, I_{CCD} <1.4 mA/MHz.

Note 4: Guaranteed, but not tested.

AC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$ $C_L = 50$ pF		Units
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	200		200		MHz
t_{PLH}	Propagation Delay	1.5	5.3	1.5	5.3	ns
t_{PHL}	$CPAB_n$ or $CPBA_n$ to A_n or B_n	1.5	5.3	1.5	5.3	
t_{PZH}	Output Enable Time	1.5	5.5	1.5	5.5	ns
t_{PZL}	$\overline{OEAB}_n$ or $\overline{OEBA}_n$ to A_n or B_n	1.5	5.5	1.5	5.5	
t_{PHZ}	Output Disable Time	1.5	6.0	1.5	6.0	ns
t_{PLZ}	$\overline{OEAB}_n$ or $\overline{OEBA}_n$ to A_n or B_n	1.5	6.0	1.5	6.0	

AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$ $V_{CC} = 4.5V$ to $5.5V$ $C_L = 50$ pF		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH	2.5		2.5		ns
$t_S(L)$	or LOW A_n or B_n to $\overline{CPAB}_n$ or $CPBA_n$	2.5		2.5		
$t_H(H)$	Hold Time, HIGH	1.5		1.5		ns
$t_H(L)$	or LOW A_n or B_n to $\overline{CPAB}_n$ or $CPBA_n$	1.5		1.5		
$t_S(H)$	Setup Time, HIGH	2.5		2.5		ns
$t_S(L)$	or LOW $\overline{CEA}_n$ or $\overline{CEB}_n$ to $\overline{CPAB}_n$ or $\overline{CPBA}_n$	2.5		2.5		
$t_H(H)$	Hold Time, HIGH	1.5		1.5		ns
$t_H(L)$	or LOW $\overline{CEA}_n$ or $\overline{CEB}_n$ to $\overline{CPAB}_n$ or $\overline{CPBA}_n$	1.5		1.5		
$t_W(H)$	Pulse Width,	3.0		3.0		ns
$t_W(L)$	HIGH or LOW to $\overline{CPAB}_n$ or $\overline{CPBA}_n$	3.0		3.0		

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25°C$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$ (Non I/O Pins)
$C_{I/O}$ (Note 5)	Output Capacitance	11	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 5: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading

FIGURE 1. Standard AC Test Load
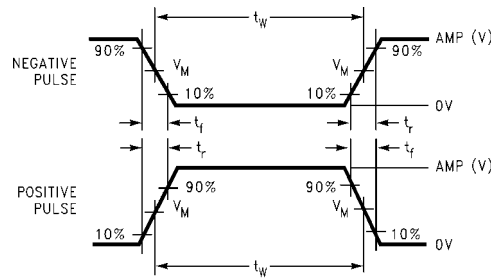
$V_M = 1.5V$

FIGURE 2. Test Input Signal Levels

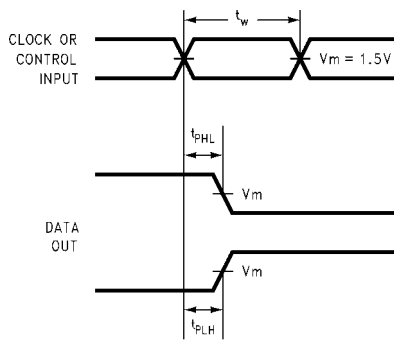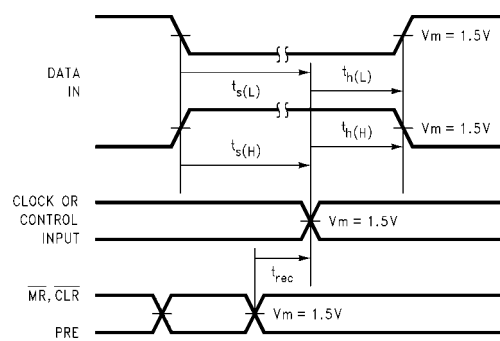| Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Input Signal Requirements

AC Waveforms
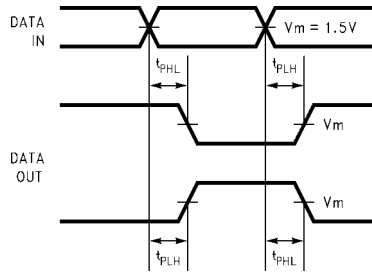
FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions
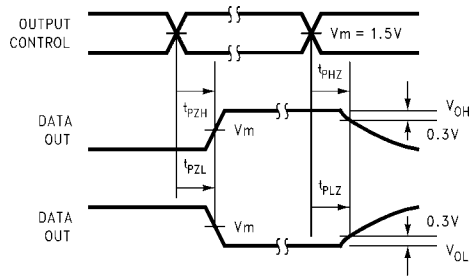
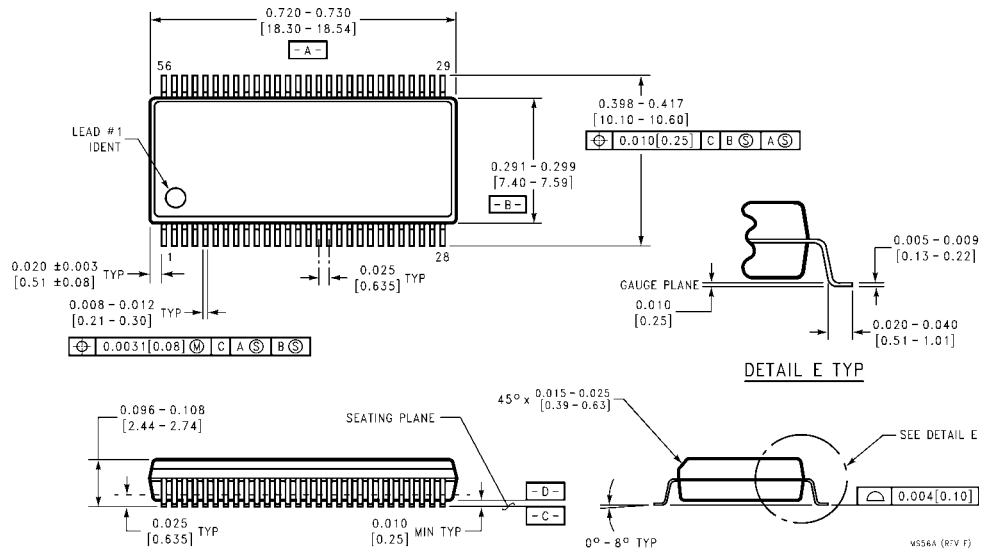FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times


FIGURE 5. Propagation Delay, Pulse Width Waveforms

FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

*Includes jig and probe capacitance

74ABT16952

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Physical Dimensions inches (millimeters) unless otherwise noted

0.720 – 0.730
[18.30 – 18.54]
– A –

56   29

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]
⊕ 0.010[0.25] C B Ⓢ A Ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

0.020 ±0.003 TYP
[0.51 ±0.08]

1

0.008 – 0.012 TYP
[0.21 – 0.30]

0.025 TYP
[0.635]

28

⊕ 0.0031[0.08] Ⓜ C A Ⓢ B Ⓢ

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE
0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

– D –
– C –

0.025 TYP
[0.635]

0.010 MIN TYP
[0.25]

0° – 8° TYP

◁ 0.004[0.10]

MS56A (REV F)

56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

LAND PATTERN RECOMMENDATION

DETAIL A
TYPICAL
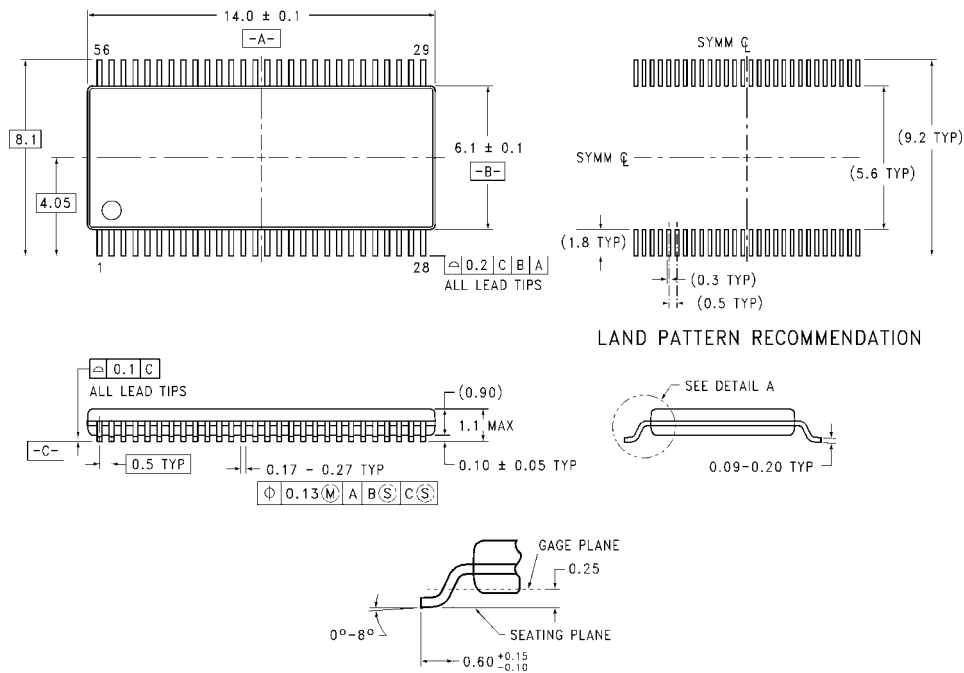
MTD56 (REV B)

56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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