Data Sheet

SCA100T-D07 2-AXIS HIGH PERFORMANCE ANALOG ACCELEROMETER

Features

- Measurement range ±12g
- Measurement bandwidth 400 Hz
- Low noise ratiometric analog voltage outputs
- Excellent bias stability over temperature and time
- Digital SPI temperature output
- Comprehensive failure detection features
  - True self test by deflecting the sensing element's proof mass with electrostatic force.
  - Continuous sensing element interconnection failure check.
  - Continuous memory parity check.
- RoHS and lead free soldering process compliant
- Robust design, high shock durability (20000g)

Applications

SCA100T-D07 is targeted to inertial sensing applications with high stability and tough environmental requirements. Typical application include

- IMU, AHRS
- Avionics
- UAV
- Navigation and guidance instruments
- Platform stabilization
- Vibration monitoring
- Oil & Gas surveying and drilling
- Train and Rail industry

General Description

The SCA100T-D07 is a 3D-MEMS-based dual axis accelerometer that enables tactical grade performance for Inertial Measurement Units (IMUs) operating in tough environmental conditions. The measuring axes of the sensor are parallel to the mounting plane and orthogonal to each other. Wide measurement range and bandwidth, low repeatable temperature behavior, low output noise, together with a very robust sensing element and packaging design, make the SCA100T-D07 the ideal choice for challenging inertial sensing applications.

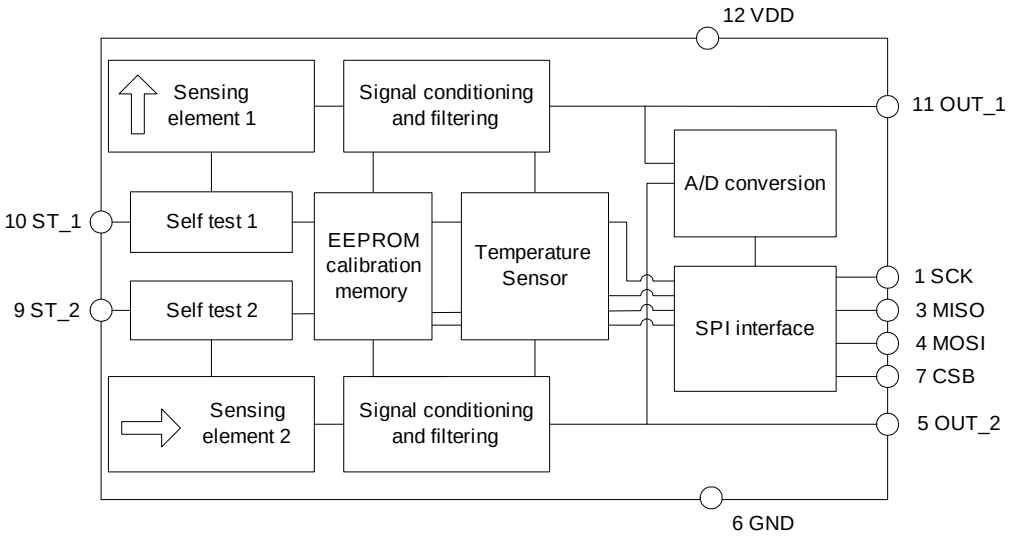

Figure 1. Functional block diagram

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1 Electrical Specifications

The product version specific performance specifications are listed in the table SCA100T performance characteristics below. Vdd=5.00V and ambient temperature unless otherwise specified.

1.1 Absolute Maximum Ratings

Supply voltage (V_{DD})	-0.3 V to +5.5V
Voltage at input / output pins	-0.3V to (V_{DD} + 0.3V)
Storage temperature	-55°C to +125°C
Operating temperature	-40°C to +125°C
Mechanical shock	Drop from 1 meter onto a concrete surface (20000g). Powered or non-powered

1.2 Performance Characteristics

1.3 Parameter	Condition	Min(1	Typical	Max(1	Units
Measuring range	Nominal	-12		+12	g
Frequency response	–3dB LP	250	400	550	Hz
Offset (Output at 0g)	Ratiometric output	Vdd/2		Vdd/2	V
Offset Digital Output			1024		LSB
Offset Calibration error		-45		45	mg
Offset Temperature Dependency	-25…+85°C	-200		200	mg
	-40…+125°C	-300		300	mg
Offset Temperature Hysteresis	-40…+125°C	-50		50	mg
Sensitivity			0.17		V/g
Sensitivity Digital Output			70		LSB / g
Sensitivity Calibration error		-2		+2	%
Sensitivity Temperature Dependency	-25…+85°C	-2		+2	%
	-40…+125°C	-2.5		+2.5	%
Linearity error	-15…+85ºC	-60		60	mg
	+25ºC	-25		25	mg
Digital Output Resolution		11		11	Bits
Output Noise Density	From DC...100Hz		95	120	$\mu g / \sqrt{\text{Hz}}$
Ratiometric error	Vdd = 4.75...5.25V	-2		+2	%
Cross-axis sensitivity	Max.	-3.5		+3.5	%

Note 1. Min/Max values are +/-3 sigma of test population

1.4 Electrical Characteristics

Parameter	Condition	Min.	Typ	Max.	Units
Supply voltage Vdd		4.75	5.0	5.25	V
Current consumption	Vdd = 5 V; No load		4	5	mA
Operating temperature		-40		+125	°C
Analog resistive output load	Vout to Vdd or GND	10			kΩ
Analog capacitive output load	Vout to Vdd or GND			20	nF
Start-up delay	Reset and parity check			10	ms

1.5 SPI Interface DC Characteristics

Parameter	Conditions	Symbol	Min	Typ.	Max	Unit
Input terminal CSB						
Pull up current	V_{IN} = 0 V	I_{PU}	13	22	35	µA
Input high voltage		V_{IH}	4		Vdd+0.3	V
Input low voltage		V_{IL}	-0.3		1	V
Hysteresis		V_{HYST}		0.23*Vdd		V
Input capacitance		C_{IN}		2		pF
Input terminal MOSI, SCK						
Pull down current	V_{IN} = 5 V	I_{PD}	9	17	29	µA
Input high voltage		V_{IH}	4		Vdd+0.3	V
Input low voltage		V_{IL}	-0.3		1	V
Hysteresis		V_{HYST}		0.23*Vdd		V
Input capacitance		C_{IN}		2		pF
Output terminal MISO						
Output high voltage	I > -1mA	V_{OH}	Vdd-0.5			V
Output low voltage	I < 1 mA	V_{OL}			0.5	V
Tri-state leakage	0 < V_{MISO} < Vdd	I_{LEAK}		5	100	pA

1.6 SPI Interface AC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Units
Output load	@500kHz			1	nF
SPI clock frequency				500	kHz
Internal A/D conversion time			150		µs
Data transfer time	@500kHz		38		µs

1.7 SPI Interface Timing Specifications

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Terminal CSB, SCK						
Time from CSB (10%) To SCK (90%)		T_{LS1}	120			ns
Time from SCK (10%) To CSB (90%)		T_{LS2}	120			ns
Terminal SCK						
SCK low time	Load capacitance at MISO < 2 nF	T_{CL}	1			µs
SCK high time	Load capacitance at MISO < 2 nF	T_{CH}	1			µs
Terminal MOSI, SCK						
Time from changing MOSI (10%, 90%) to SCK (90%). Data setup time		T_{SET}	30			ns
Time from SCK (90%) to changing MOSI (10%,90%). Data hold time		T_{HOL}	30			ns
Terminal MISO, CSB						
Time from CSB (10%) to stable MISO (10%, 90%).	Load capacitance at MISO < 15 pF	T_{VAL1}	10		100	ns
Time from CSB (90%) to high impedance state of MISO.	Load capacitance at MISO < 15 pF	T_{LZ}	10		100	ns
Terminal MISO, SCK						
Time from SCK (10%) to stable MISO (10%, 90%).	Load capacitance at MISO < 15 pF	T_{VAL2}			100	ns
Terminal CSB						
Time between SPI cycles, CSB at high level (90%)		T_{LH}	15			µs
When using SPI commands RDAX, RDAY, and RWTR: Time between SPI cycles, CSB at high level (90%)		TLH	150			µs

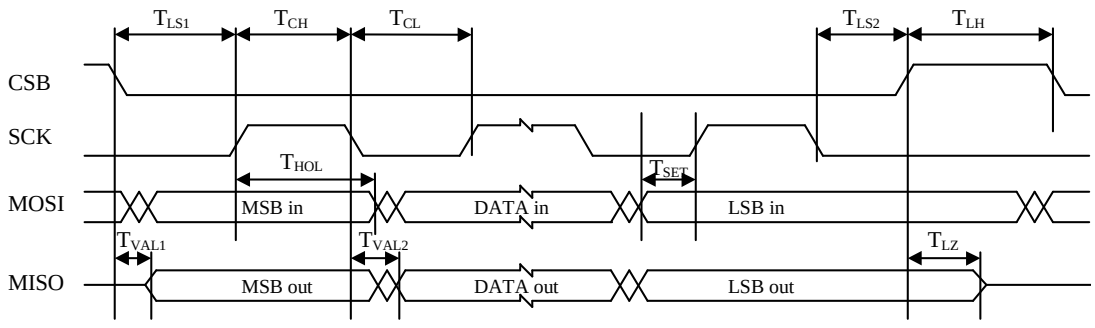

Figure 2. Timing diagram for SPI communication

1.8 Electrical Connection

If the SPI interface is not used SCK (pin1), MISO (pin3), MOSI (pin4) and CSB (pin7) must be left floating. Self-test can be activated applying logic “1” (positive supply voltage level) to ST_1 or ST_2 pins (pins 10 or 9). Self-test must not be activated for both channels at the same time. If ST feature is not used pins 9 and 10 must be left floating or connected to GND. Acceleration signals are provided from pins OUT_1 and OUT_2.

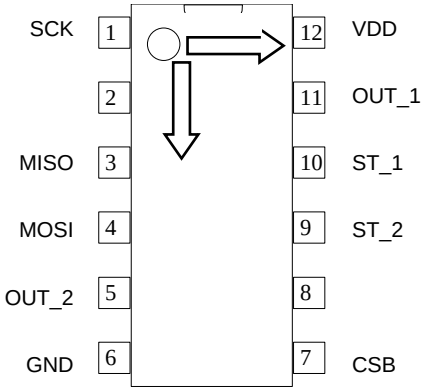

Figure 3. SCA100T electrical connection

No.	Node	I/O	Description
1	SCK	Input	Serial clock
2	NC	Input	No connect, left floating
3	MISO	Output	Master in slave out; data output
4	MOSI	Input	Master out slave in; data input
5	Out_2	Output	Y axis Output (Ch 2)
6	GND	Supply	Ground
7	CSB	Input	Chip select (active low)
8	NC	Input	No connect, left floating
9	ST_2	Input	Self test input for Ch 2
10	ST_1	Input	Self test input for Ch 1
11	Out_1	Output	X axis Output (Ch 1)
12	VDD	Supply	Positive supply voltage (+5V DC)

1.9 Typical Performance Characteristics

Typical offset and sensitivity temperature dependencies of the SCA100T are presented in following diagrams. These results represent the typical performance of SCA100T components. The mean value and 3 sigma limit (mean ± 3× standard deviation) and specification limits are presented in following diagrams. The 3 sigma limits represents 99.73% of the SCA100T population.

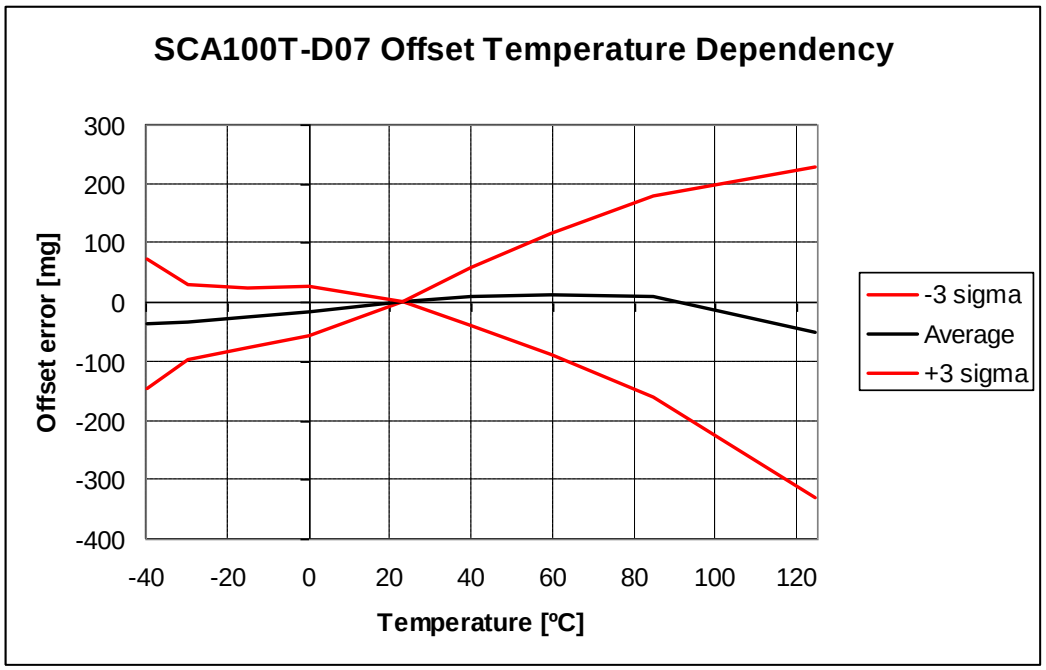

Figure 4. Typical temperature behavior of SCA100T-D07 offset

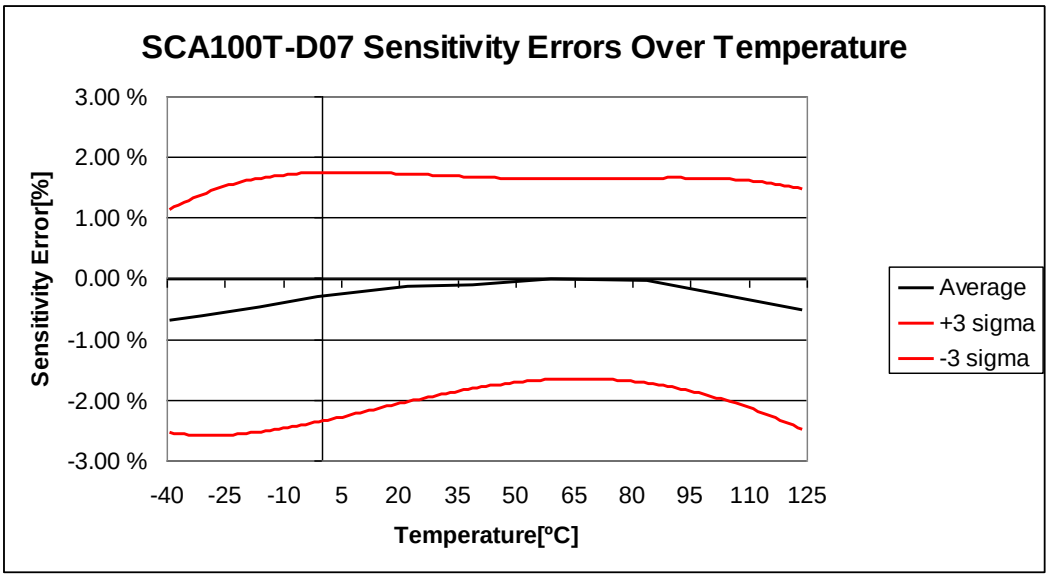

Figure 5. Typical temperature behavior of SCA100T-D07 sensitivity

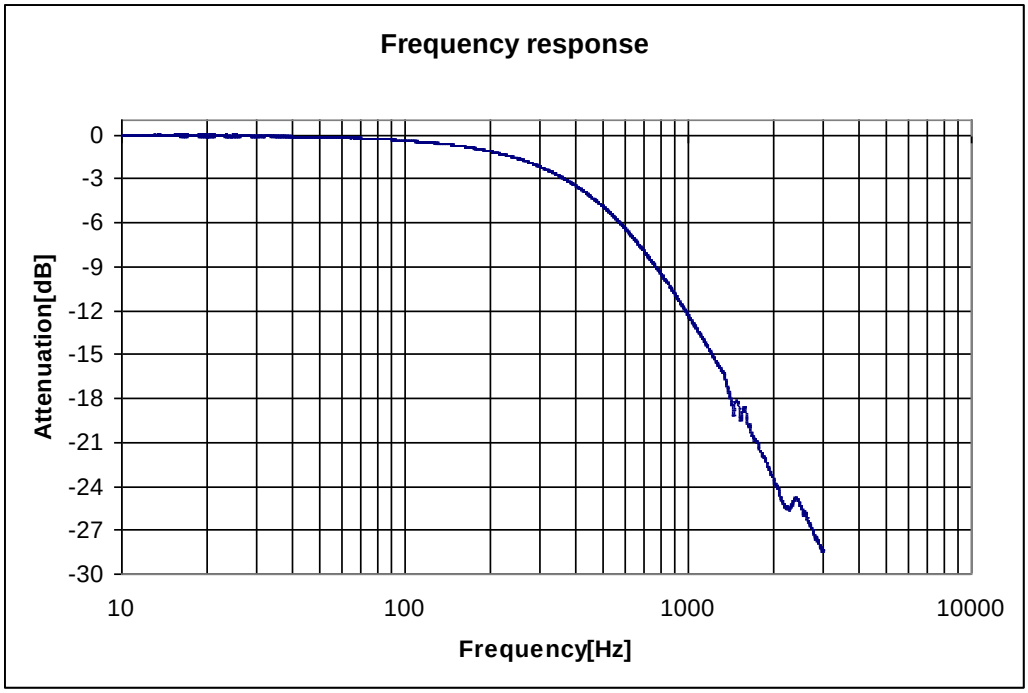

Figure 6. Frequency response of SCA100T-D07

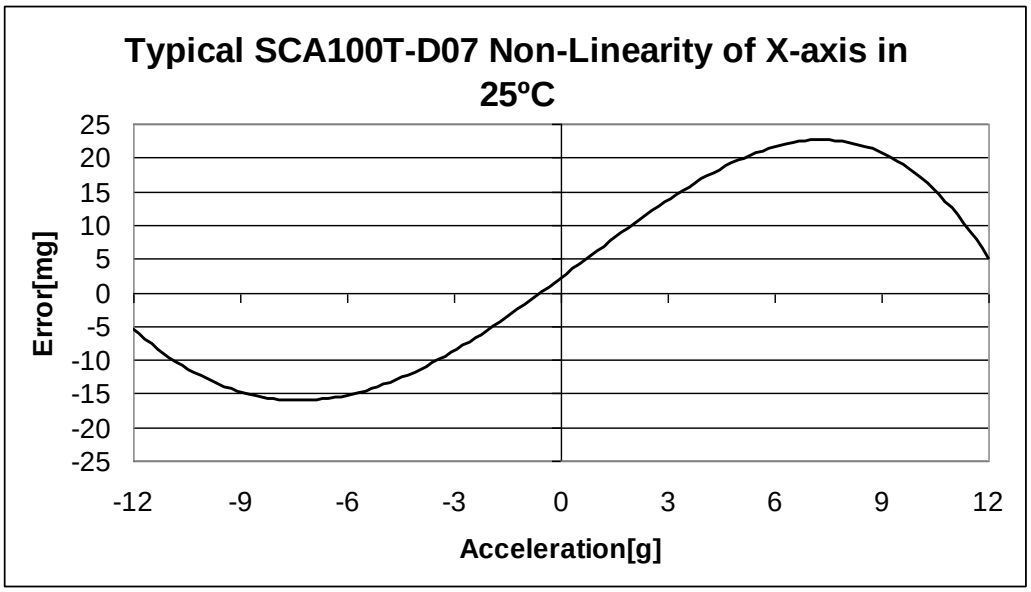

Figure 7. Typical non-linearity of SCA100T-D07 fitted to straight line in room temperature

2 Functional Description

2.1 Measuring Directions

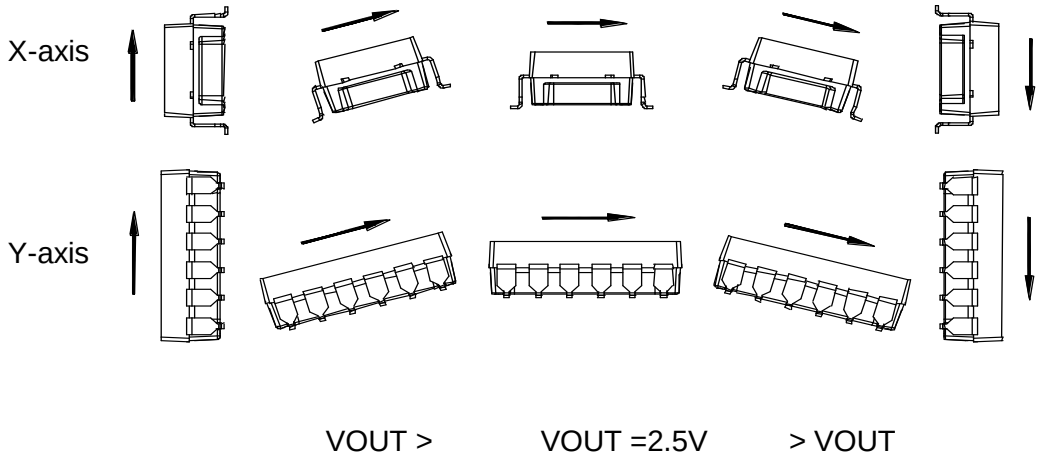

Figure 8. The measuring directions of the SCA100T

2.2 Ratiometric Output

Ratiometric output means that the zero offset point and sensitivity of the sensor are proportional to the supply voltage. If the SCA100T supply voltage is fluctuating the SCA100T output will also vary. When the same reference voltage for both the SCA100T sensor and the measuring part (A/D-converter) is used, the error caused by reference voltage variation is automatically compensated for.

2.3 SPI Serial Interface

A Serial Peripheral Interface (SPI) system consists of one master device and one or more slave devices. The master is defined as a micro controller providing the SPI clock and the slave as any integrated circuit receiving the SPI clock from the master. The ASIC in Murata Electronics' products always operates as a slave device in master-slave operation mode.

The SPI has a 4-wire synchronous serial interface. Data communication is enabled by a low active Slave Select or Chip Select wire (CSB). Data is transmitted by a 3-wire interface consisting of wires for serial data input (MOSI), serial data output (MISO) and serial clock (SCK).

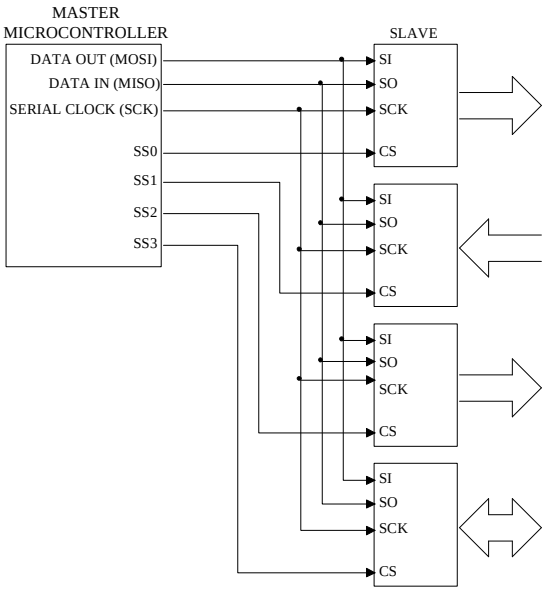

Figure 9. Typical SPI connection

The SPI interface in Murata products is designed to support any micro controller that uses SPI bus. Communication can be carried out by either a software or hardware based SPI. Please note that in the case of hardware based SPI, the received acceleration data is 11 bits. The data transfer uses the following 4-wire interface:

MOSI	master out slave in	µP → SCA100T
MISO	master in slave out	SCA100T → µP
SCK	serial clock	µP → SCA100T
CSB	chip select (low active)	µP → SCA100T

Each transmission starts with a falling edge of CSB and ends with the rising edge. During transmission, commands and data are controlled by SCK and CSB according to the following rules:

- commands and data are shifted; MSB first, LSB last
- each output data/status bits are shifted out on the falling edge of SCK (MISO line)
- each bit is sampled on the rising edge of SCK (MOSI line)
- after the device is selected with the falling edge of CSB, an 8-bit command is received. The command defines the operations to be performed
- the rising edge of CSB ends all data transfer and resets internal counter and command register
- if an invalid command is received, no data is shifted into the chip and the MISO remains in high impedance state until the falling edge of CSB. This reinitializes the serial communication.
- data transfer to MOSI continues immediately after receiving the command in all cases where data is to be written to SCA100T's internal registers
- data transfer out from MISO starts with the falling edge of SCK immediately after the last bit of the SPI command is sampled in on the rising edge of SCK
- maximum SPI clock frequency is 500kHz
- maximum data transfer speed for RDAX and RDAY is 5300 samples per sec / channel

SPI command can be either an individual command or a combination of command and data. In the case of combined command and data, the input data follows uninterruptedly the SPI command and the output data is shifted out parallel with the input data.

The SPI interface uses an 8-bit instruction (or command) register. The list of commands is given in Table below.

Command name	Command format	Description:
MEAS	00000000	Measure mode (normal operation mode after power on)
RWTR	00001000	Read temperature data register
STX	00001110	Activate Self test for X-channel
STY	00001111	Activate Self test for Y-channel
RDAX	00010000	Read X-channel acceleration
RDAY	00010001	Read Y-channel acceleration

Measure mode (MEAS) is standard operation mode after power-up. During normal operation, the MEAS command is the exit command from Self test.

Read temperature data register (RWTR) reads temperature data register during normal operation without affecting the operation. The temperature data register is updated every 150 µs. The load operation is disabled whenever the CSB signal is low, hence CSB must stay high at least 150 µs prior to the RWTR command in order to guarantee correct data. The data transfer is presented in Figure 10 below. The data is transferred MSB first. In normal operation, it does not matter what data is written into temperature data register during the RWTR command and hence writing all zeros is recommended.

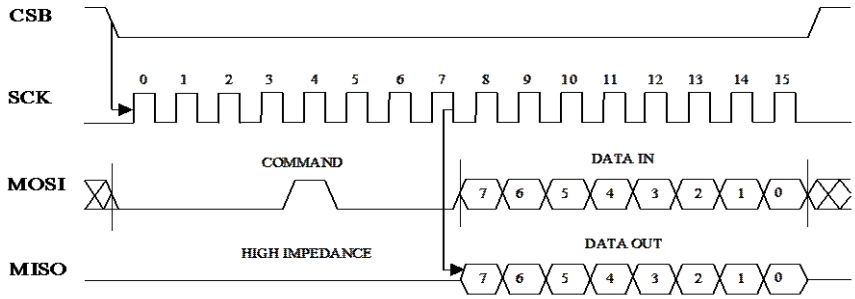

Figure 1. *Command and 8 bit temperature data transmission over the SPI*

Self test for X-channel (STX) activates the self test function for the X-channel (Channel 1). The internal charge pump is activated and a high voltage is applied to the X-channel acceleration sensor element electrode. This causes the electrostatic force that deflects the beam of the sensing element and simulates the acceleration to the positive direction. The self-test is de-activated by giving the MEAS command. **The self test function must not be activated for both channels at the same time.**

Self test for Y-channel (STY) activates the self test function for the Y-channel (Channel 2). The internal charge pump is activated and a high voltage is applied to the Y-channel acceleration sensor element electrode.

Read X-channel acceleration (RDAX) accesses the AD converted X-channel (Channel 1) acceleration signal stored in acceleration data register X.

Read Y-channel acceleration (RDAY) accesses the AD converted Y-channel (Channel 2) acceleration signal stored in acceleration data register Y.

During normal operation, acceleration data registers are reloaded every 150 µs. The load operation is disabled whenever the CSB signal is low, hence CSB must stay high at least 150 µs prior the RDAX command in order to guarantee correct data. Data output is an 11-bit digital word that is fed out MSB first and LSB last.

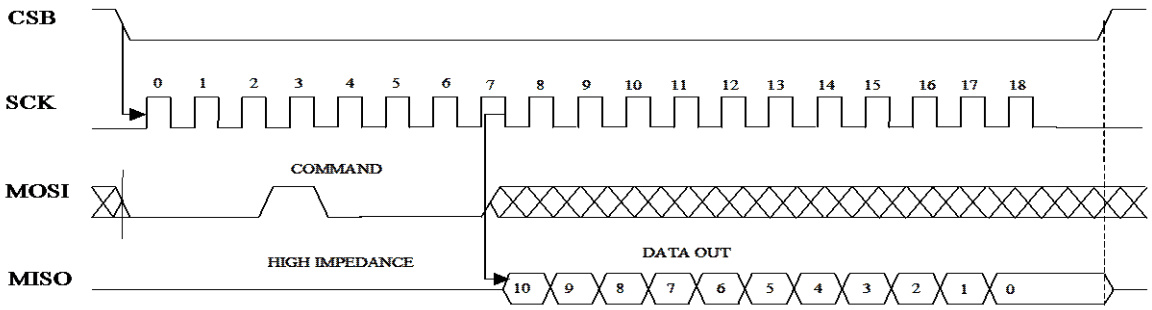

Figure 10. Command and 11 bit acceleration data transmission over the SPI

2.4 Self Test and Failure Detection Modes

To ensure reliable measurement results the SCA100T has continuous interconnection failure and calibration memory validity detection. A detected failure forces the output signal close to power supply ground or VDD level, outside the normal output range. The normal output ranges are: analog 0.25-4.75 V (@Vdd=5V) and SPI 102...1945 counts.

The calibration memory validity is verified by continuously running parity check for the control register memory content. In the case where a parity error is detected, the control register is automatically re-loaded from the EEPROM. If a new parity error is detected after re-loading data both analog output voltages are forced to go close to ground level (<0.25 V) and SPI outputs go below 102 counts.

The SCA100T also includes a separate self test mode. The true self test simulates acceleration, or deceleration, using an electrostatic force. The electrostatic force simulates acceleration that is high enough to deflect the proof mass to the extreme positive position, and this causes the output signal to go to the maximum value. The self test function is activated either by a separate on-off command on the self test input, or through the SPI.

The self-test generates an electrostatic force, deflecting the sensing element's proof mass, thus checking the complete signal path. The true self test performs following checks:

- Sensing element movement check
- ASIC signal path check
- PCB signal path check
- Micro controller A/D and signal path check

The created deflection can be seen in both the SPI and analogue output. The self test function is activated digitally by a STX or STY command, and de-activated by a MEAS command. Self test can be also activated applying logic"1" (positive supply voltage level) to ST pins (pins 9 & 10) of SCA100T. The self test Input high voltage level is 4 – Vdd+0.3 V and input low voltage level is 0.3 – 1 V. **The self test function must not be activated for both channels at the same time**.

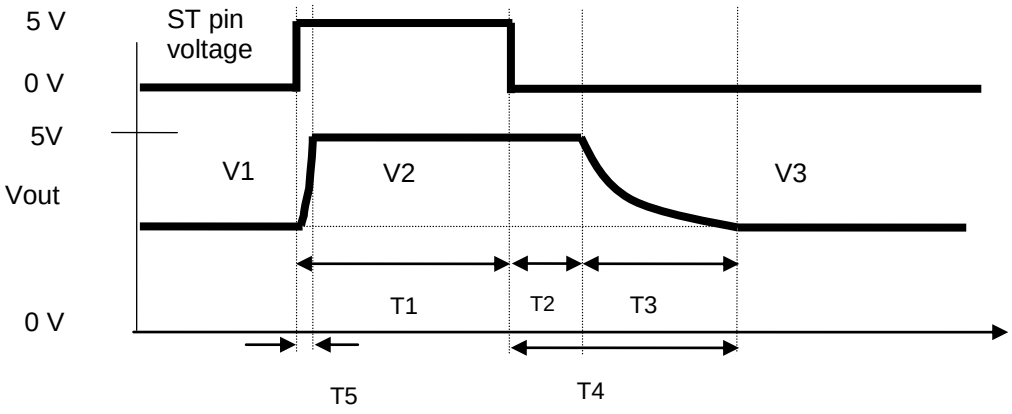

Figure 11. Self test wave forms

V1 = initial output voltage before the self test function is activated.
V2 = output voltage during the self test function.
V3 = output voltage after the self test function has been de-activated and after stabilization time Please note that the error band specified for V3 is to guarantee that the output is within 5% of the initial value after the specified stabilization time. After a longer time (max. 1 second) V1=V3.
T1 = Pulse length for Self test activation
T2 = Saturation delay
T3 = Recovery time
T4 = Stabilization time =T2+T3
T5 = Rise time during self test.

Self test characteristics:

T1 [ms]	T2 [ms]	T3 [ms]	T4 [ms]	T5 [ms]	V2:	V3:
20-100	Typ. 25	Typ. 30	Typ. 55	Typ. 15	Min 0.95*VDD (4.75V @Vdd=5V)	0.95*V1-1.05*V1

2.5 Temperature Measurement

The SCA100T has an internal temperature sensor, which is used for internal offset compensation. The temperature information is also available for additional external compensation. The temperature sensor can be accessed via the SPI interface and the temperature reading is an 8-bit word (0…255). The transfer function is expressed with the following formula:

$$T = \frac{Counts - 197}{-1.083}$$

Where:

Counts	Temperature reading
T	Temperature in °C

The temperature measurement output is not calibrated. The internal temperature compensation routine uses relative results where absolute accuracy is not needed. If the temperature measurement results are used for additional external compensation then one point calibration in the system level is needed to remove the offset. With external one point calibration the accuracy of the temperature measurement is about ±1 °C.

3 Application Information

3.1 Recommended Circuit Diagrams and Printed Circuit Board Layouts

The SCA100T should be powered from a well regulated 5 V DC power supply. Coupling of digital noise to the power supply line should be minimized. 100nF filtering capacitor between VDD pin 12 and GND plane must be used.

The SCA100T has a ratiometric output. To get the best performance use the same reference voltage for both the SCA100T and Analog/Digital converter.

Use low pass RC filters with 5.11 kΩ and 10nF on the SCA100T outputs to minimize clock noise.

Locate the 100nF power supply filtering capacitor close to VDD pin 12. Use as short a trace length as possible. Connect the other end of capacitor directly to the ground plane. Connect the GND pin 6 to underlying ground plane. Use as wide ground and power supply planes as possible. Avoid narrow power supply or GND connection strips on PCB.

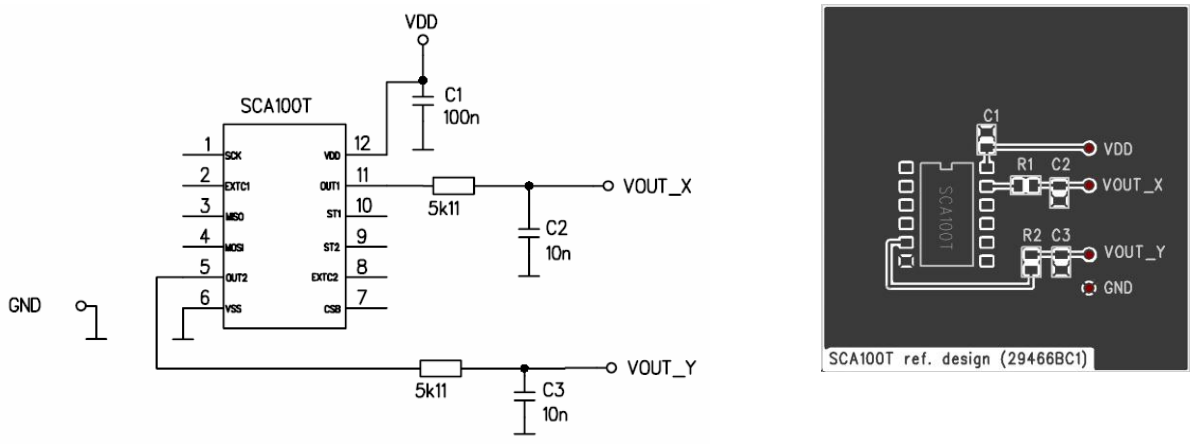

Figure 12. Analog connection and layout example

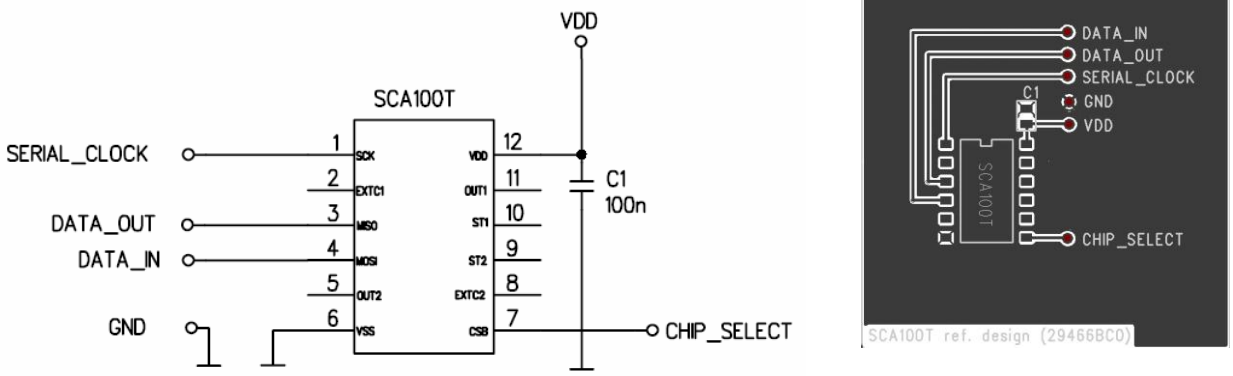

Figure 13. SPI connection example

3.2 Recommended Printed Circuit Board Footprint

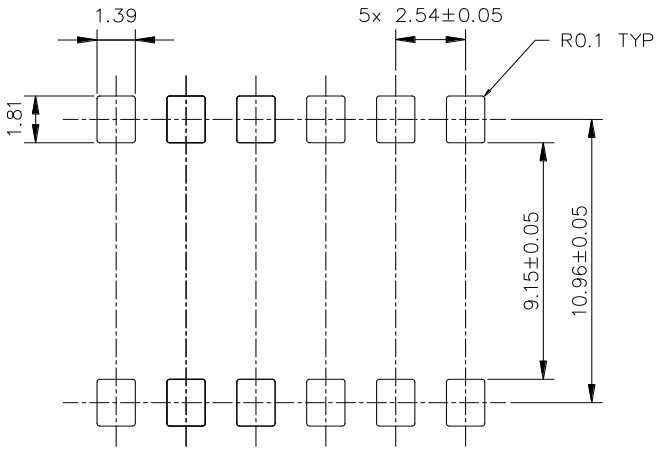

Figure 14. Recommended PCB footprint

4 Mechanical Specifications and Reflow Soldering

4.1 Mechanical Specifications

Lead frame material:	Copper
Plating:	Nickel followed by Gold
Solderability:	JEDEC standard: JESD22-B102-C
RoHS compliance:	RoHS compliant lead free component.
Co-planarity error:	0.1mm max.
Part weight:	<1.2 g

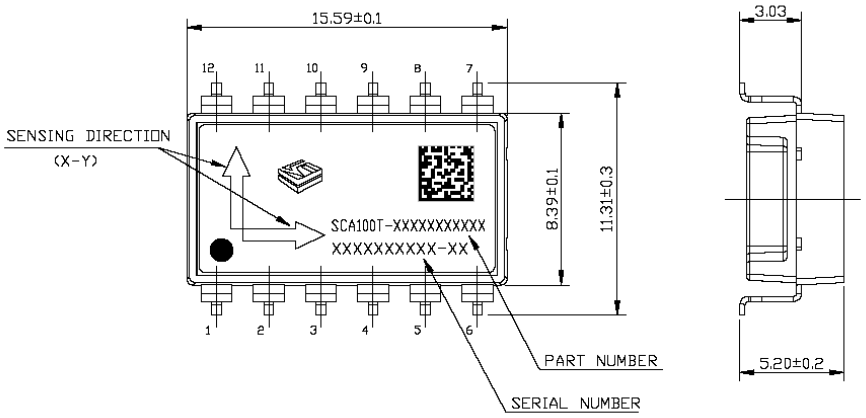

Figure 15. Mechanical dimensions of the SCA100T (Dimensions in mm)

4.2 Reflow Soldering

The SCA100T is suitable for Sn-Pb eutectic and Pb- free soldering process and mounting with normal SMD pick-and-place equipment.

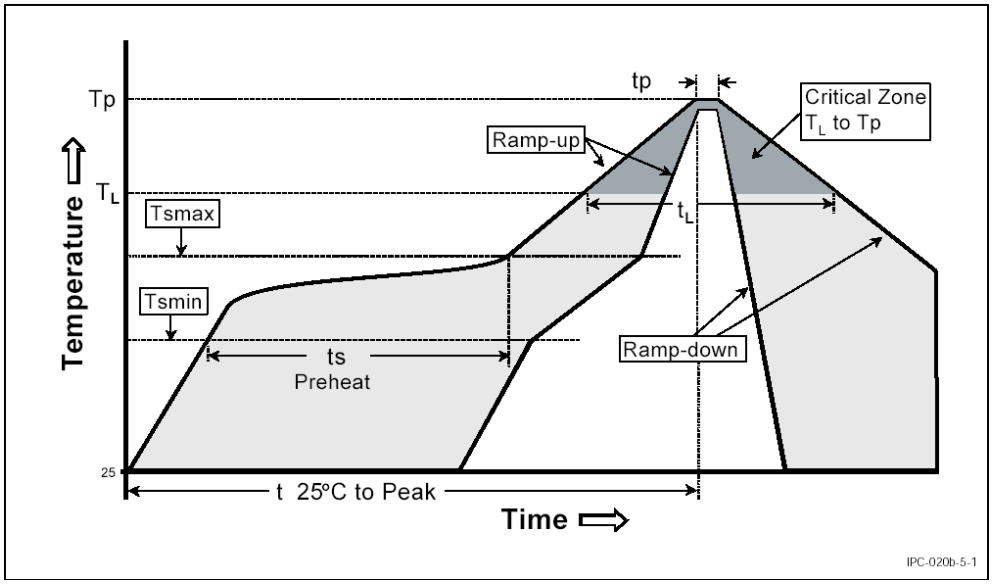

Figure 16. Recommended SCA100T body temperature profile during reflow soldering. Ref. IPC/JEDEC J-STD-020B.

Profile feature	Sn-Pb Eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat		
- Temperature min (T_{smin})	100°C	150°C
- Temperature max (T_{smax})	150°C	200°C
- Time (min to max) (ts)	60-120 seconds	60-180 seconds
Tsmax to T, Ramp up rate		3°C/second max
Time maintained above:		
- Temperature (T_L)	183°C	217°C
- Time (t_L)	60-150 seconds	60-150 seconds
Peak temperature (T_P)	240 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature (T_P)	10-30 seconds	20-40 seconds
Ramp-down rate	6°C/second max	6°C/second max
Time 25° to Peak temperature	6 minutes max	8 minutes max

The Moisture Sensitivity Level of the part is 3 according to the IPC/JEDEC J-STD-020B. The part should be delivered in a dry pack. The manufacturing floor time (out of bag) in the customer's end is 168 hours.

Notes:

- Preheating time and temperatures according to guidance from solder paste manufacturer.
- It is important that the part is parallel to the PCB plane and that there is no angular alignment error from intended measuring direction during assembly process.
- Wave soldering is not recommended.
- **Ultrasonic cleaning is not allowed**. The sensing element may be damaged by an ultrasonic cleaning process.