HAT2197R

Silicon N Channel Power MOS FET
Power Switching

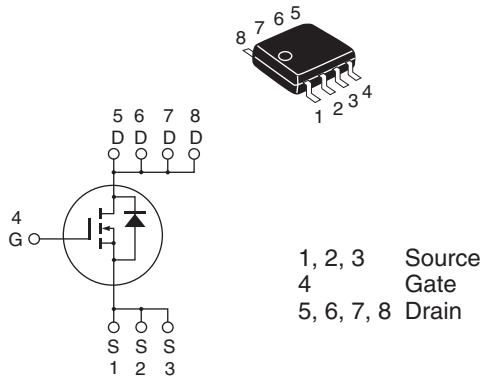
REJ03G0061-0201Z
Rev.2.01
Nov.30.2016

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
  $R_{DS(on)}$ = 5.3 mΩ typ. (at V_{GS} = 10 V)

Outline

SOP-8



1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	16	A
Drain peak current	$I_{D(pulse)}$ Note1	128	A
Body-drain diode reverse drain current	I_{DR}	16	A
Avalanche current	I_{AP} Note 2	16	A
Avalanche energy	E_{AR} Note 2	25.6	mJ
Channel dissipation	Pch Note3	2.5	W
Channel to ambient thermal impedance	θch-a Note3	50	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

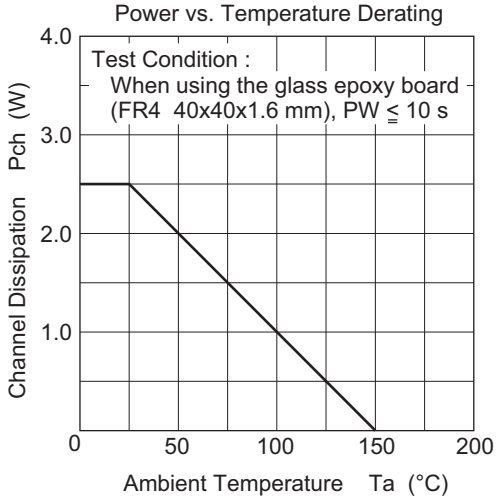
Electrical Characteristics

(Ta = 25°C)

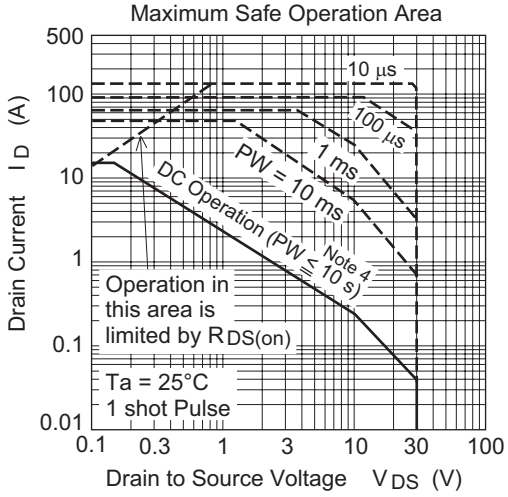
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	± 0.1	µA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	5.3	6.7	mΩ	I_D = 8 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	6.8	9.9	mΩ	I_D = 8 A, V_{GS} = 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	22	38	—	S	I_D = 8 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	2650	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	610	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	190	—	pF	f = 1 MHz
Gate Resistance	Rg	—	1.2	—	Ω	
Total gate charge	Qg	—	18	—	nC	V_{DD} = 10 V
Gate to source charge	Qgs	—	7.5	—	nC	V_{GS} = 4.5 V
Gate to drain charge	Qgd	—	4.2	—	nC	I_D = 16 A
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	V_{GS} = 10 V, I_D = 8 A
Rise time	t_r	—	25	—	ns	V_{DD} ≅ 10 V
Turn-off delay time	$t_{d(off)}$	—	45	—	ns	R_L = 1.25 Ω
Fall time	t_f	—	4.2	—	ns	Rg = 4.7 Ω
Body–drain diode forward voltage	V_{DF}	—	0.80	1.04	V	IF = 16 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	30	—	ns	IF = 16 A, V_{GS} = 0 diF/ dt = 100 A/ µs

Notes: 4. Pulse test

Power vs. Temperature Derating

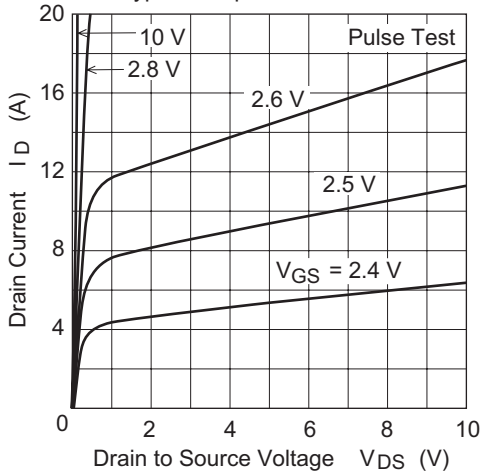


Maximum Safe Operation Area

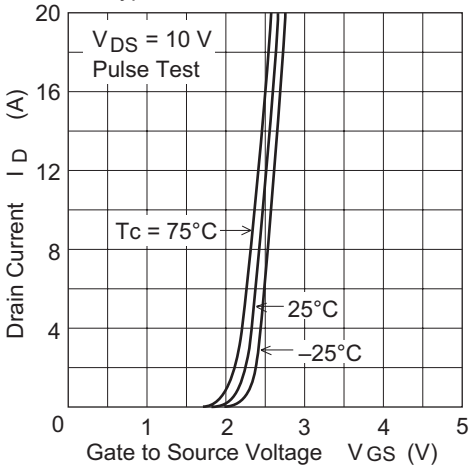


Note 4 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

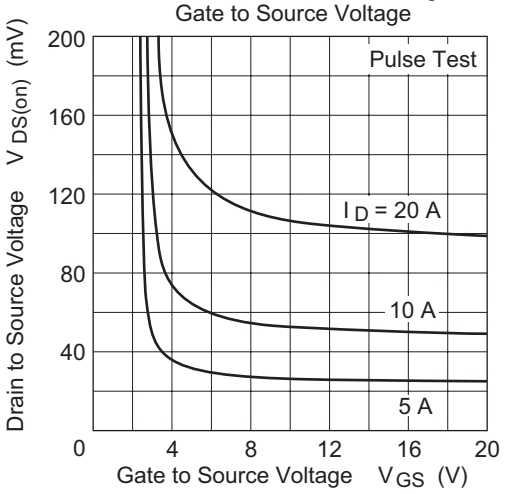
Typical Output Characteristics



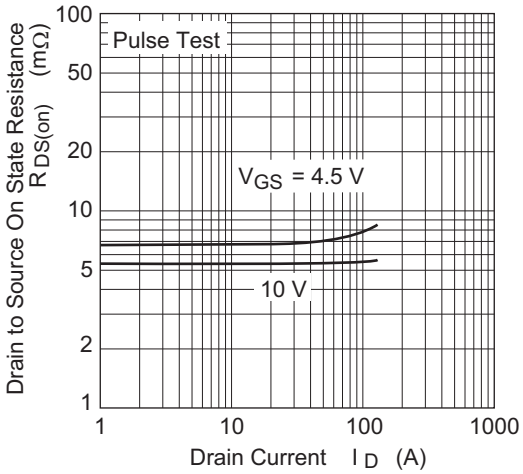
Typical Transfer Characteristics



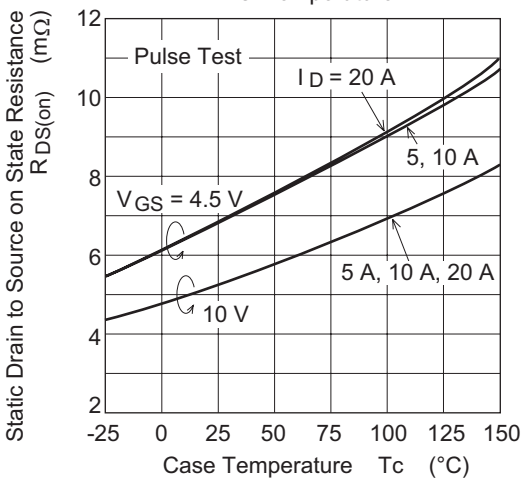
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



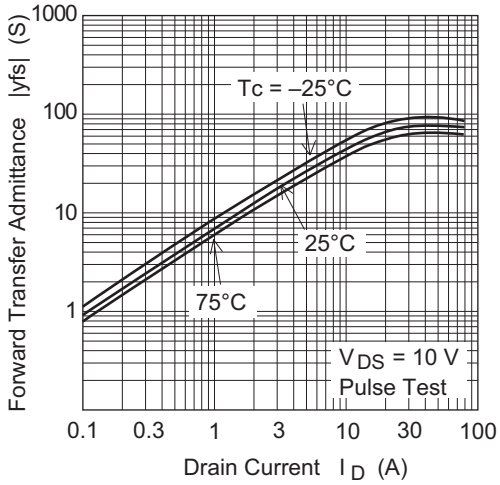
Static Drain to Source on State Resistance
vs. Drain Current



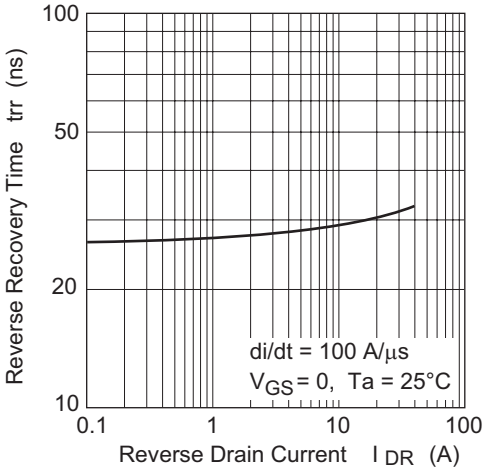
Static Drain to Source on State Resistance vs. Temperature



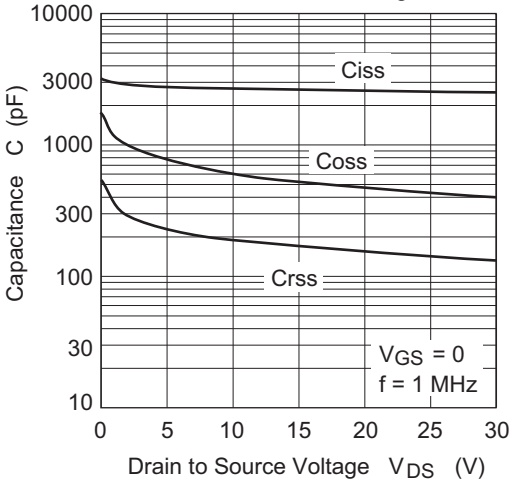
Forward Transfer Admittance vs. Drain Current



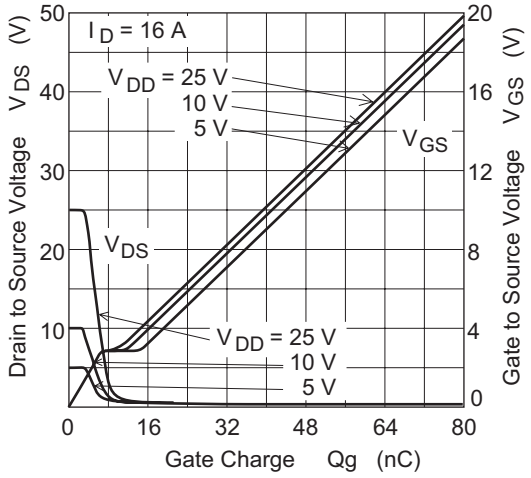
Body–Drain Diode Reverse Recovery Time



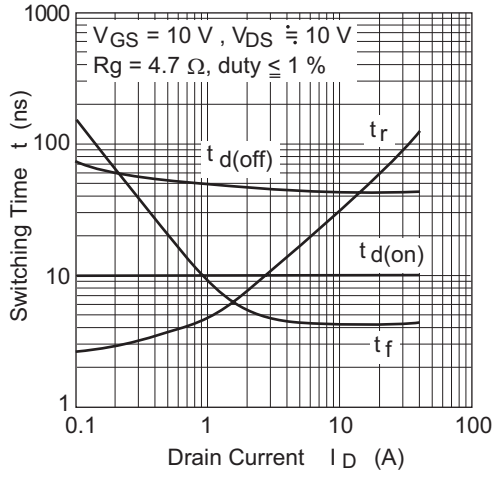
Typical Capacitance vs. Drain to Source Voltage



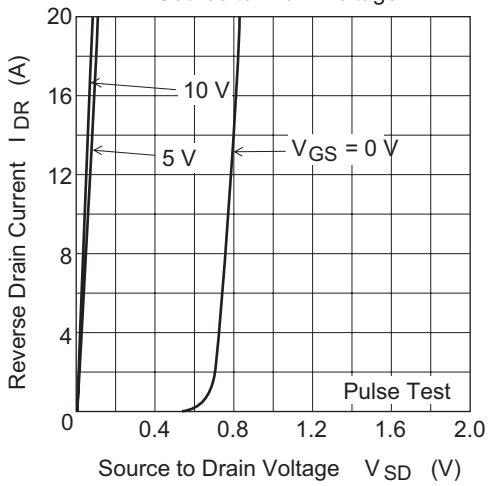
Dynamic Input Characteristics



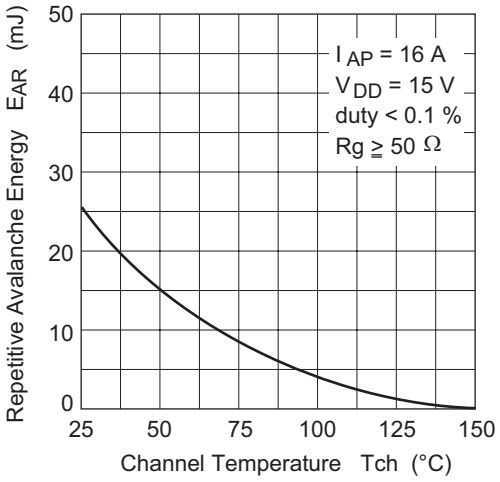
Switching Characteristics



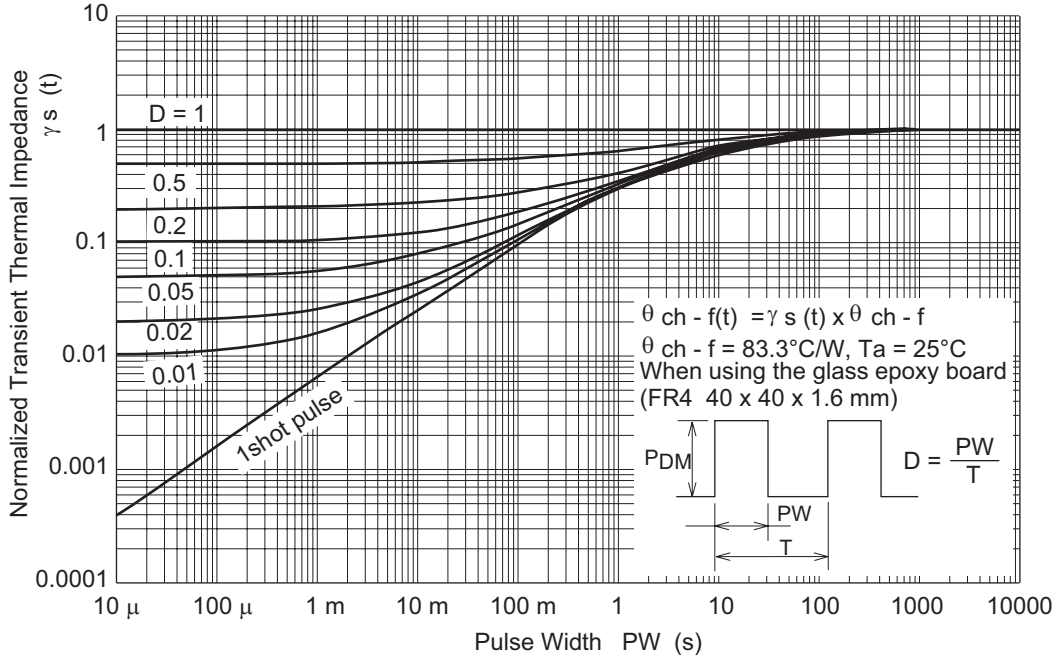
Reverse Drain Current vs.
Source to Drain Voltage



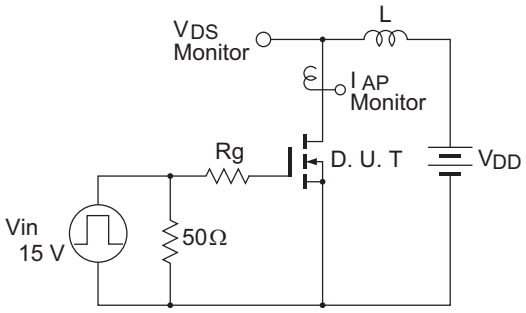
Maximum Avalanche Energy vs.
Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

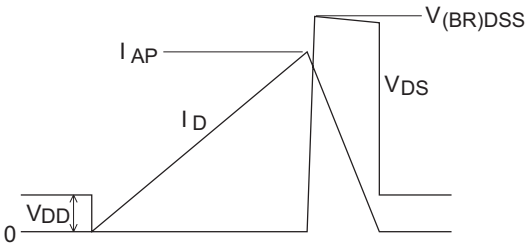


Avalanche Test Circuit

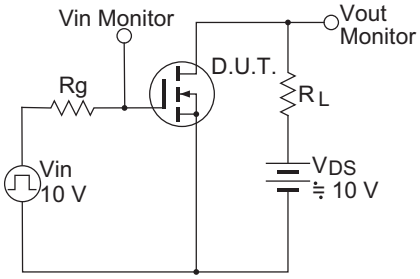


Avalanche Waveform

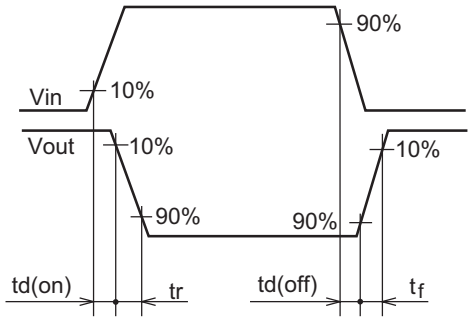
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

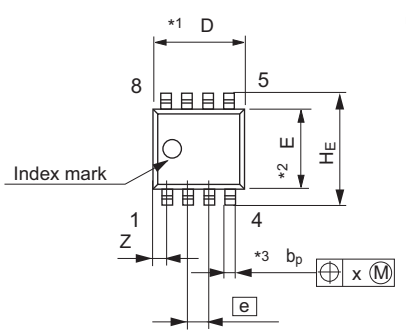


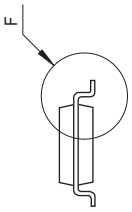
Switching Time Waveform

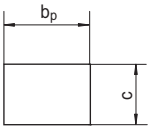


Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g

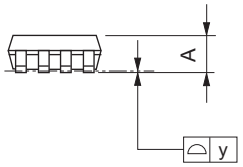


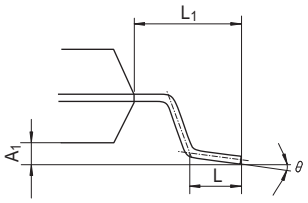




Terminal cross section
(Ni/Pd/Au plating)

NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.





Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L_1	—	1.08	—

Ordering Information

Orderable Part Number	Quantity	Shipping Container
HAT2197R-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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7. 虽然瑞萨电子一直致力于提高瑞萨电子产品的质量和可靠性，但是，半导体产品有其自身的具体特性，如一定的故障发生率以及在某些使用条件下会发生故障等。此外，瑞萨电子产品均未进行防辐射设计。所以请采取安全保护措施，以避免当瑞萨电子产品在发生故障而造成火灾时导致人身事故、伤害或损害的事故。例如进行软硬件安全设计（包括但不限于冗余设计、防火控制以及故障预防等）、适当的老化处理或其他适当的措施等。由于难于对微机软件单独进行评估，所以请用户自行对最终产品或系统进行安全评估。
8. 关于环境保护方面的详细内容，例如每种瑞萨电子产品的环境兼容性等，请与瑞萨电子的营业部门联系。使用瑞萨电子产品时，请遵守对管制物质的使用或含量进行管理的所有相应法律法规（包括但不限于《欧盟RoHS指令》）。对于因用户未遵守相应法律法规而导致的损害或损失，瑞萨电子不承担任何责任。
9. 不可将瑞萨电子产品和技术用于或者嵌入日本国内或海外相应的法律法规所禁止生产、使用及销售的任何产品或系统中。也不可将本文档中记载的瑞萨电子产品或技术用于与军事应用或者军事用途有关的任何目的（如大规模杀伤性武器的开发等）。在将本文档中记载的瑞萨电子产品或技术进行出口时，应当遵守相应的出口管制法律法规，并按照上述法律法规所规定的程序进行。
10. 向第三方分销或处分产品或者以其他方式将产品置于第三方控制之下的瑞萨电子产品买方或分销商，有责任事先向上述第三方通知本文档规定的内容和条件；对于用户或第三方因非法使用瑞萨电子产品而遭受的任何损失，瑞萨电子不承担任何责任。
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