Data Sheet

1.5MHz, 800mA, STEP DOWN DC-DC CONVERTER AUR9703

General Description

The AUR9703 is a high efficiency step-down DC-DC voltage converter. The chip operation is optimized using constant frequency, peak-current mode architecture with built-in synchronous power MOSFET switchers and internal compensators to reduce external part counts. It is automatically switching between the normal PWM mode and LDO mode to offer improved system power efficiency covering a wide range of loading conditions.

The oscillator and timing capacitors are all built-in providing an internal switching frequency of 1.5MHz that allows the use of small surface mount inductors and capacitors for portable product implementations. Additional features included Soft Start (SS), Under Voltage Lock Out (UVLO), and Thermal Shutdown Detection (TSD) to provide reliable product applications.

The device is available in adjustable output voltage versions ranging from 1V to 3.3V, and is able to deliver up to 800mA.

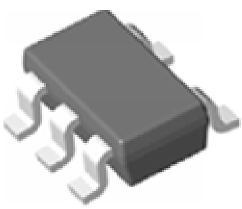
The AUR9703 is available in TSOT-23-5 package.

Features

- High Efficiency Buck Power Converter
- Low Quiescent Current
- Output Current: 800mA
- Adjustable Output Voltage from 1V to 3.3V
- Wide Operating Voltage Range: 2.5V to 5.5V
- Built-in Power Switches for Synchronous Rectification with High Efficiency
- Feedback Voltage: 600mV
- 1.5MHz Constant Frequency Operation
- Automatic PWM/LDO Mode Switching Control
- Thermal Shutdown Protection
- Low Drop-out Operation at 100% Duty Cycle
- No Schottky Diode Required

Applications

- Mobile Phone, Digital Camera and MP3 Player
- Headset, Radio and Other Hand-held Instrument
- Post DC-DC Voltage Regulation
- PDA and Notebook Computer



TSOT-23-5

Figure 1. Package Type of AUR9703

Pin Configuration

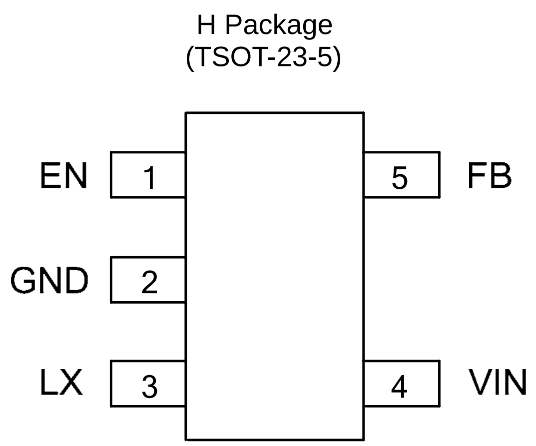


Figure 2. Pin Configuration of AUR9703 (Top View)

Pin Description

Pin Number	Pin Name	Function
1	EN	Enable signal input, active high
2	GND	This pin is the GND reference for the NMOS power stage. It must be connected to the system ground
3	LX	Connect to inductor
4	VIN	Power supply input
5	FB	Feedback voltage from the output

Functional Block Diagram

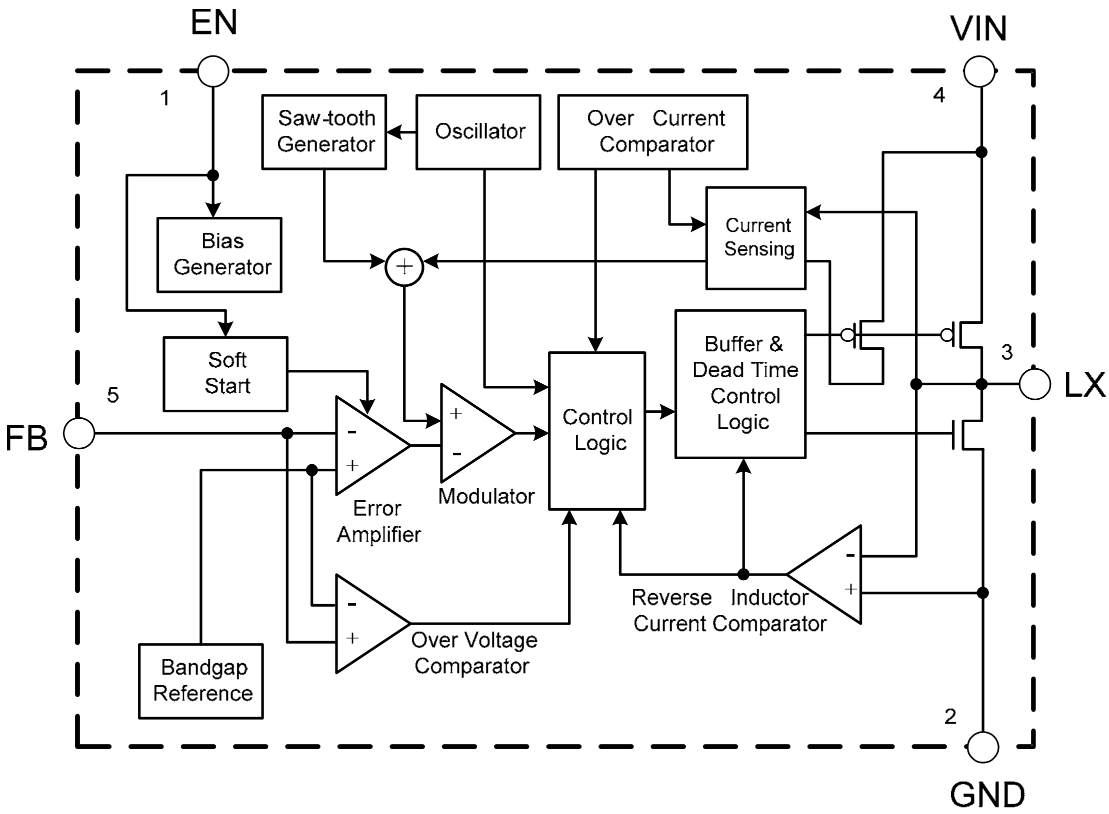
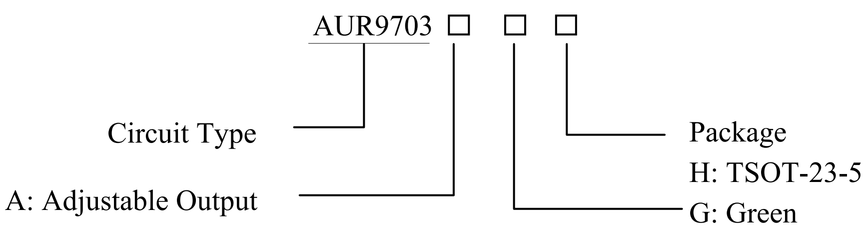


Figure 3. Functional Block Diagram of AUR9703

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
TSOT-23-5	-40 to 80°C	AUR9703AGH	9703AG	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G" in the part number, are RoHS compliant and green.

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value	Unit
Supply Input Voltage	V_{IN}	0 to 6.0	V
Enable Input Voltage	V_{EN}	-0.3 to V_{IN}+0.3	V
Output Voltage	V_{OUT}	-0.3 to V_{IN}+0.3	V
Power Dissipation (On PCB, T_A=25°C)	P_D	0.85	W
Thermal Resistance (Junction to Ambient, Simulation)	θ_{JA}	118.31	°C/W
Thermal Resistance (Junction to Case, Simulation)	θ_{JC}	113.67	°C/W
Operating Junction Temperature	T_J	160	°C
Operating Temperature	T_{OP}	-40 to 85	°C
Storage Temperature	T_{STG}	-55 to 150	°C
ESD (Human Body Model)	V_{HBM}	2000	V
ESD (Machine Model)	V_{MM}	200	V

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Input Voltage	V_{IN}	2.5	5.5	V
Junction Temperature Range	T_J	-20	125	°C
Ambient Temperature Range	T_A	-40	80	°C

Electrical Characteristics

V_{IN}=5V, V_{OUT}=3.3V, V_{FB}=0.6V, L=2.2μH, C_{IN}=4.7μF, C_{OUT}=10μF, T_A=25°C, I_{MAX}=800mA. Unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Shutdown Current	I_{OFF}	V_{EN}=0		0.1	1	μA
Regulated Feedback Voltage	V_{FB}	For Adjustable Output Voltage	0.585	0.6	0.615	V
Regulated Output Voltage Accuracy	$\Delta V_{OUT}/V_{OUT}$	V_{IN}=2.5V to 5.5V, I_{OUT}=0 to 800mA	-3		3	%
Peak Inductor Current	I_{PK}	V_{IN}=5V, V_{FB}=0.5V		1.2		A
Oscillator Frequency	f_{OSC}	V_{IN}=5V	1.2	1.5	1.8	MHz
PMOSFET R_{ON}	$R_{ON(P)}$	V_{IN}=5V, I_{OUT}=200mA		0.25		Ω
NMOSFET R_{ON}	$R_{ON(N)}$	V_{IN}=5V, I_{OUT}=200mA		0.27		Ω
Quiescent Current	I_Q	I_{OUT}=0A, V_{FB}= 0.7V		100		μA
LX Leakage Current	I_{LX}	V_{EN}=0V, V_{LX}=0V or 5V, V_{IN}=5V		0.1	1	μA
Feedback Current	I_{FB}				30	nA
Soft Start Time	t_{SS}			200		μs
EN Leakage Current	I_{EN}			0.01	0.1	μA
EN High-level Input Voltage	V_{EN_H}	V_{IN}=2.5V to 5.5V	1.5			V
EN Low-Level Input Voltage	V_{EN_L}	V_{IN}=2.5V to 5.5V			0.6	V
Under Voltage Lock Out	V_{UVLO}			1.8		V
Hysteresis				0.1		V
Thermal Shutdown	T_{SD}			160		°C

Typical Performance Characteristics

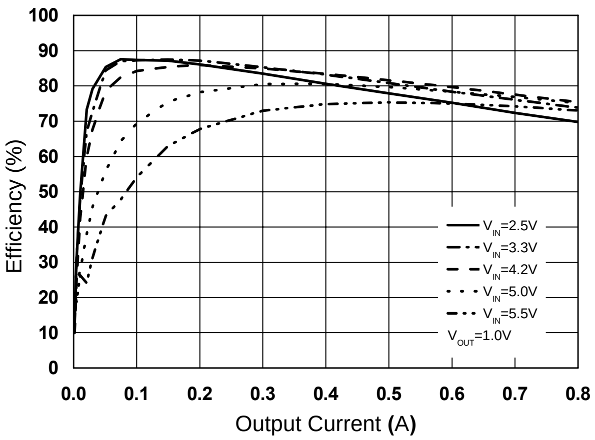


Figure 4. Efficiency vs. Output Current (V_{OUT}=1.0V)

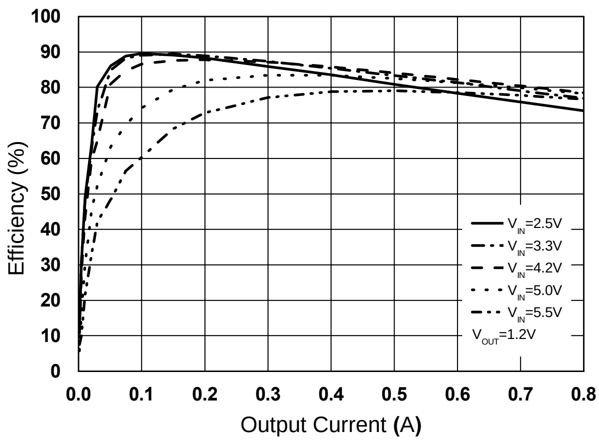


Figure 5. Efficiency vs. Output Current (V_{OUT}=1.2V)

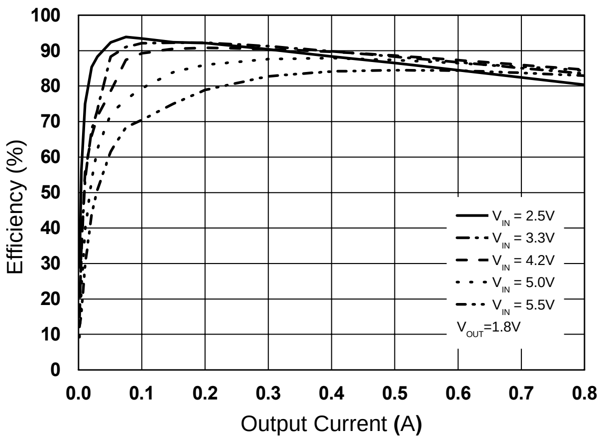


Figure 6. Efficiency vs. Output Current (V_{OUT}=1.8V)

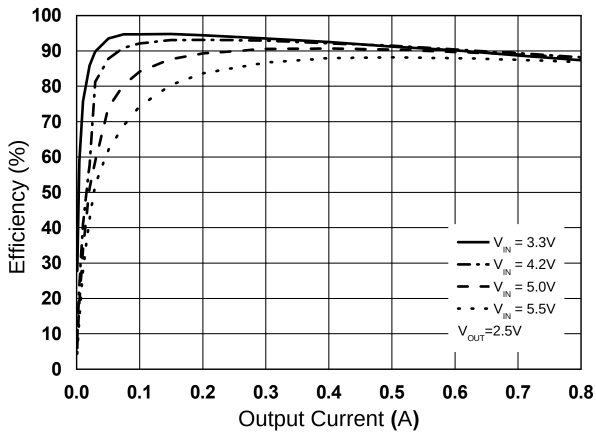


Figure 7. Efficiency vs. Output Current (V_{OUT}=2.5V)

Typical Performance Characteristics (Continued)

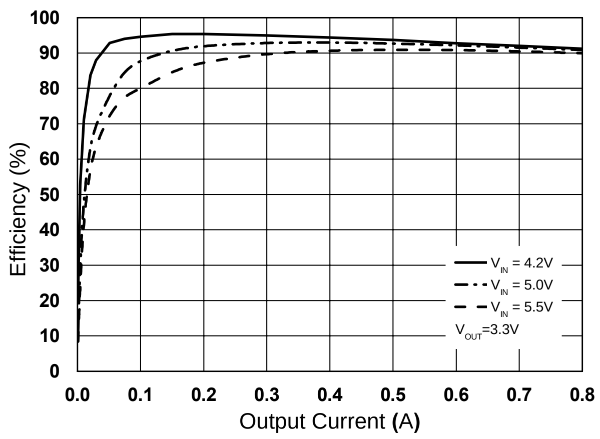


Figure 8. Efficiency vs. Output Current (V_{OUT}=3.3V)

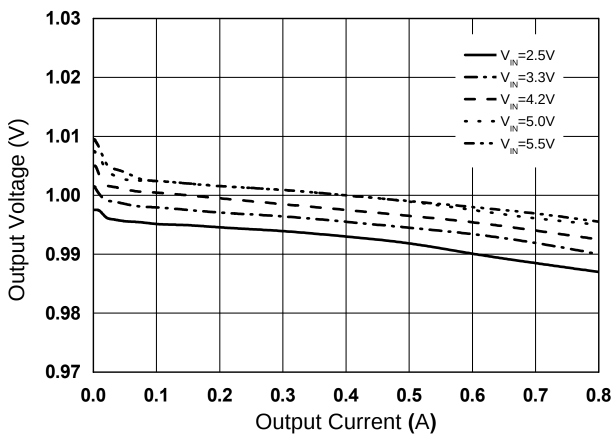


Figure 9. Load Regulation (V_{OUT}=1.0±0.03V)

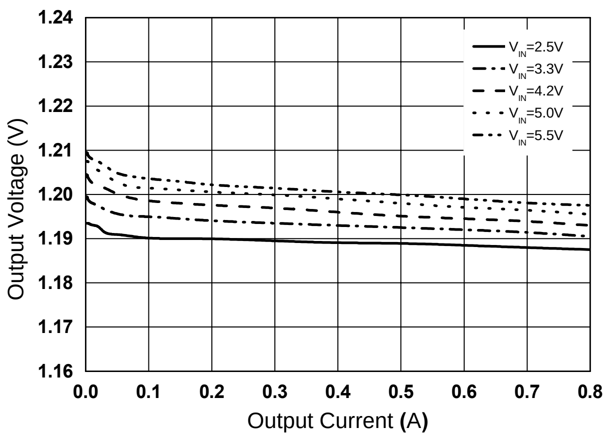


Figure 10. Load Regulation (V_{OUT}=1.2±0.03V)

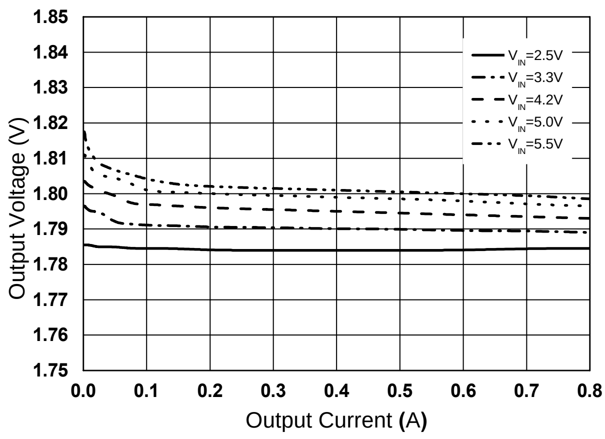


Figure 11. Load Regulation (V_{OUT}=1.8±0.03V)

Typical Performance Characteristics (Continued)

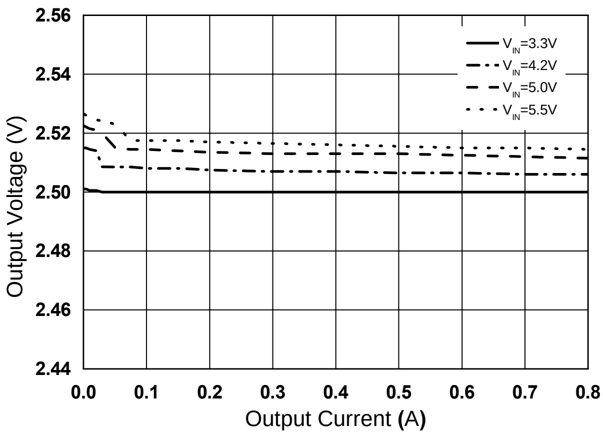


Figure 12. Load Regulation (V_{OUT}=2.5±0.03V)

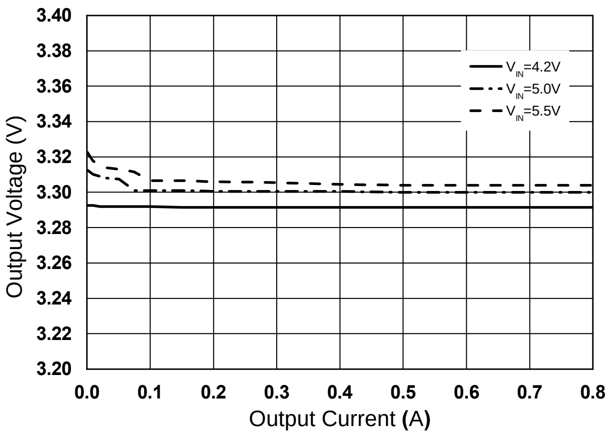


Figure 13. Load Regulation (V_{OUT}=3.3±0.03V)

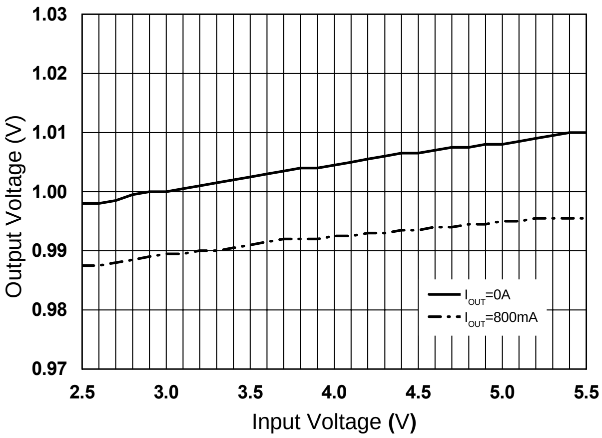


Figure 14. Line Regulation (V_{OUT}=1.0±0.03V)

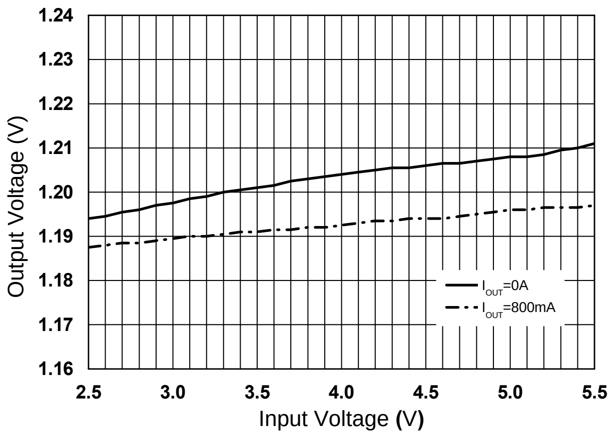


Figure 15. Line Regulation (V_{OUT}=1.2±0.03V)

Typical Performance Characteristics (Continued)

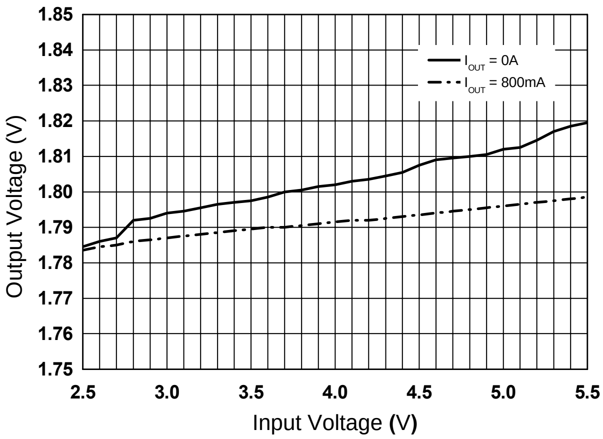


Figure 16. Line Regulation (V_{OUT}=1.8±0.03V)

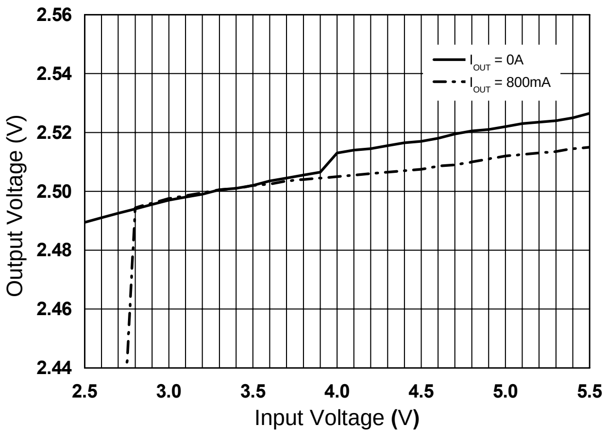


Figure 17. Line Regulation (V_{OUT}=2.5±0.03V)

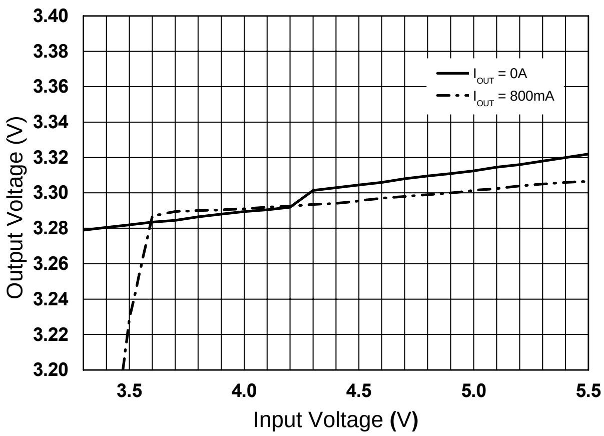


Figure 18. Line Regulation (V_{OUT}=3.3±0.03V)

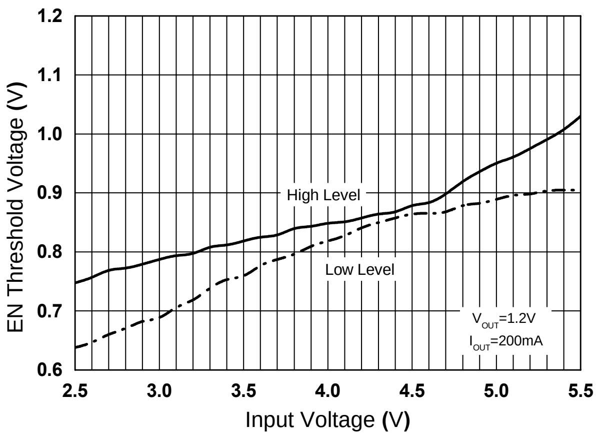


Figure 19.EN Threshold Voltage vs. Input Voltage

Typical Performance Characteristics (Continued)

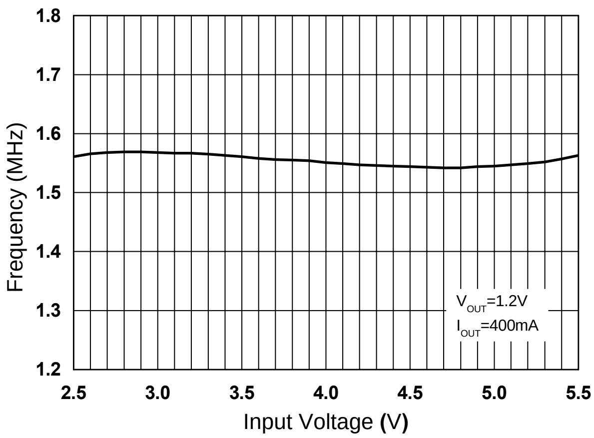


Figure 20.Frequency vs. Input Voltage

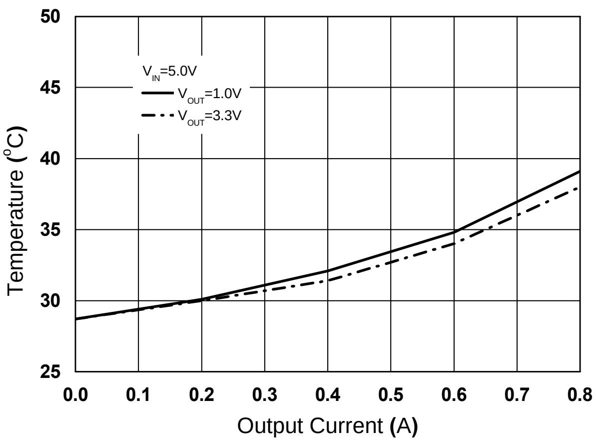


Figure 21.Temperature vs. Output Current

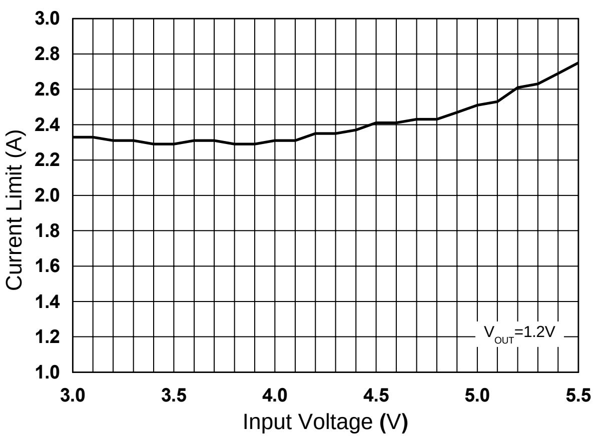


Figure 22. Current Limit vs. Input Voltage

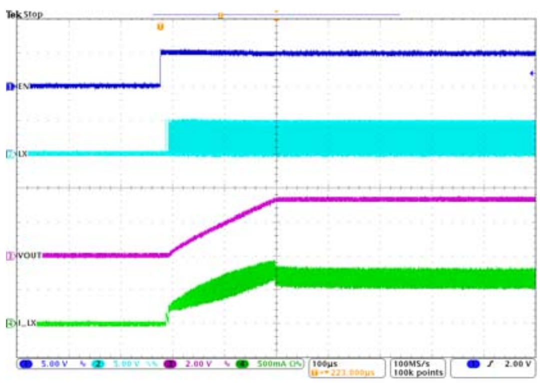


Figure 23. Start Up through EN
(V_{IN}=5V, V_{EN}= 0 to 5V, V_{OUT}=3.3V, I_{OUT}=800mA)

Typical Performance Characteristics (Continued)

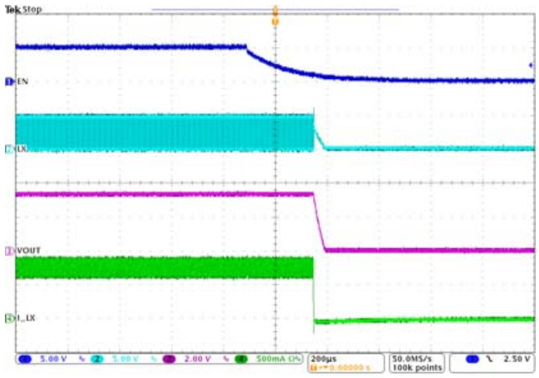


Figure 24. Shut Down through EN
(V_{IN}=5V, V_{EN}=5V to 0V, V_{OUT}=3.3V, I_{OUT}=800mA)

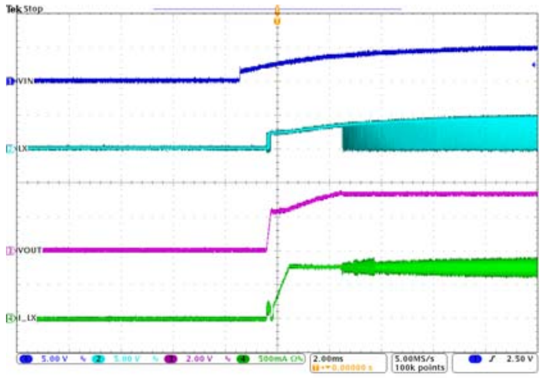


Figure 25. Start Up through VIN
(V_{IN}=0 to 5V, V_{OUT}=3.3V, I_{OUT}=800mA)

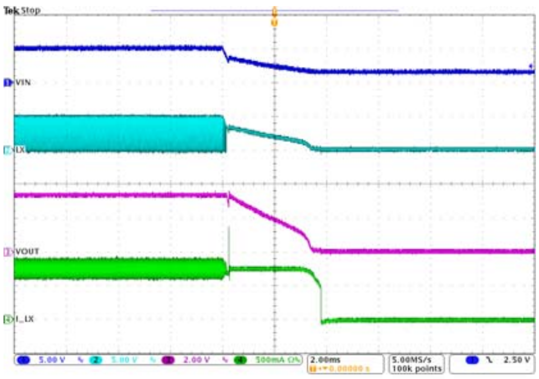


Figure 26. Shut Down through VIN
(V_{IN}=5.0 to 0V, V_{OUT}=3.3V, I_{OUT}=800mA)

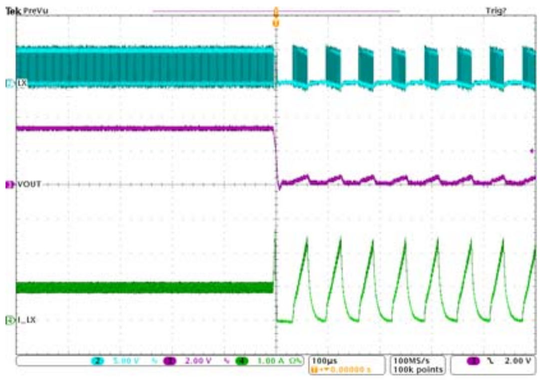


Figure 27. Short Circuit Protection
(V_{IN}=5.0V, V_{OUT} =3.3V, I_{OUT}=800mA)

Typical Performance Characteristics (Continued)

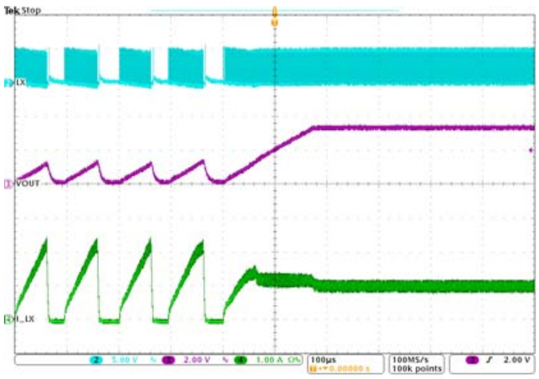


Figure 28. Short Circuit Recovery
(V_{IN}=5.0V, V_{OUT}=3.3V, I_{OUT}=800mA)

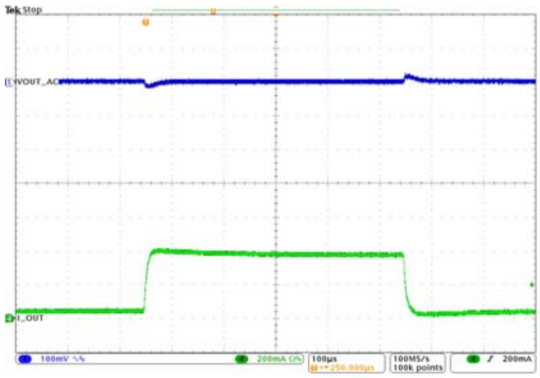


Figure 29. Load Transition
(V_{IN}=5.0V, V_{OUT}=1.0V, I_{OUT}=50mA to 400mA)

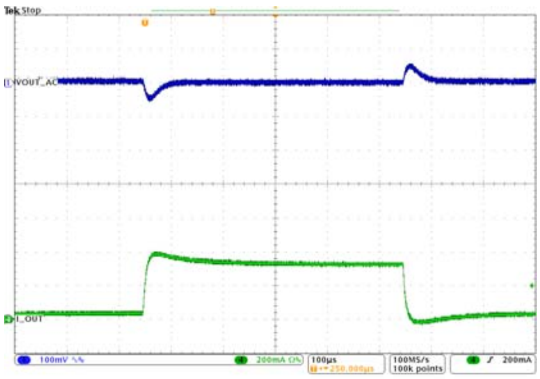


Figure 30. Load Transition
(V_{IN}=5.0V, V_{OUT}=3.3V, I_{OUT}=50mA to 400mA)

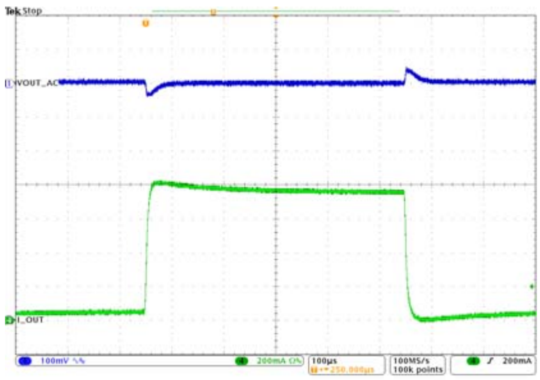


Figure 31. Load Transition
(V_{IN}=5.0V, V_{OUT}=1.0V, I_{OUT}=50mA to 800mA)

Typical Performance Characteristics (Continued)

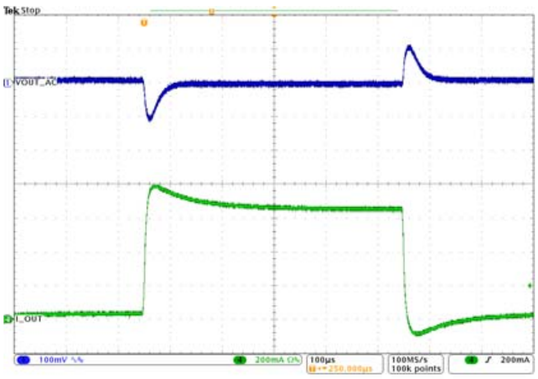


Figure 32. Load Transition
(V_{IN}=5.0V, V_{OUT}=3.3V, I_{OUT}=50mA to 800mA)

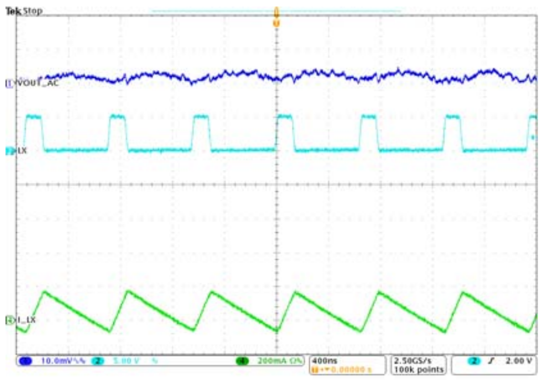


Figure 33. Output Ripple Voltage
(V_{IN}=5.0V, V_{OUT}=1.0V, I_{OUT}=10mA)

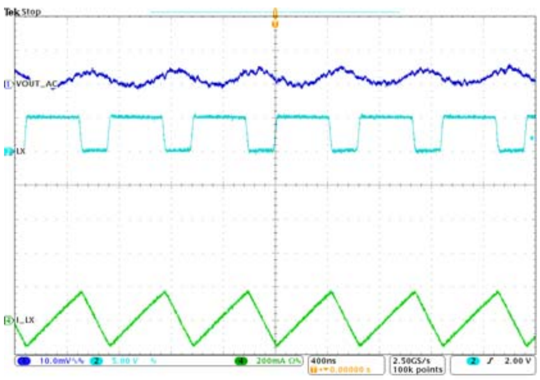


Figure 34. Output Ripple Voltage
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=10mA)

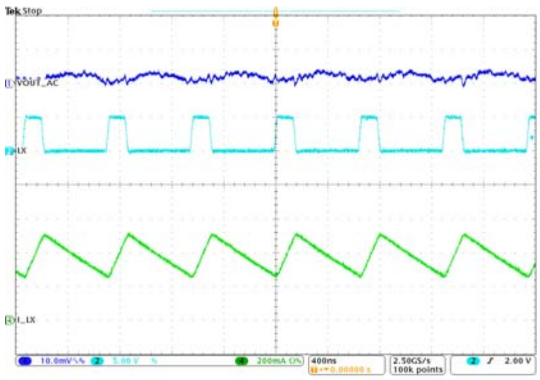


Figure 35. Output Ripple Voltage
(V_{IN}=5V, V_{OUT}=1.0V, I_{OUT}=400mA)

Typical Performance Characteristics (Continued)

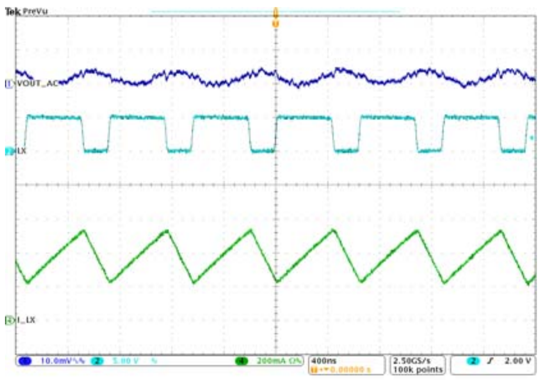


Figure 36. Output Ripple Voltage
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=400mA)

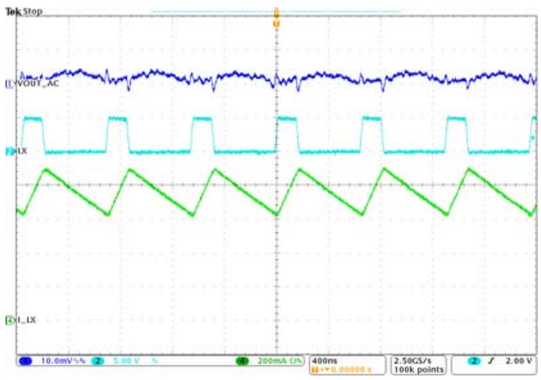


Figure 37. Output Ripple Voltage
(V_{IN}=5V, V_{OUT}=1.0V, I_{OUT}=800mA)

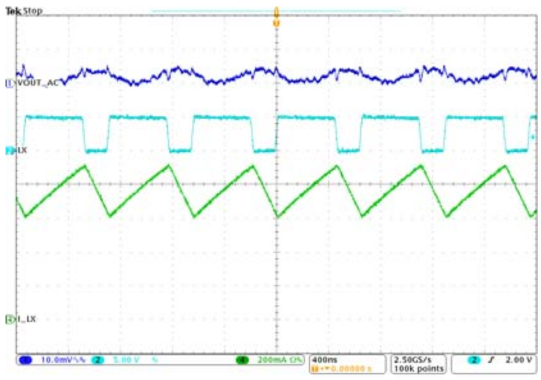


Figure 38. Output Ripple Voltage
(V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=800mA)

Application Information

The basic AUR9703 application circuit is shown in Figure 41, external components selection is determined by the load current and is critical with the selection of inductor and capacitor values.

1. Inductor Selection

For most applications, the value of inductor is chosen based on the required ripple current with the range of 2.2μH to 4.7μH.

$$\Delta I_L = \frac{1}{f \times L} V_{OUT}(1 - \frac{V_{OUT}}{V_{IN}})$$

The largest ripple current occurs at the highest input voltage. Having a small ripple current reduces the ESR loss in the output capacitor and improves the efficiency. The highest efficiency is realized at low operating frequency with small ripple current. However, larger value inductors will be required. A reasonable starting point for ripple current setting is $\triangle I_L = 40\% I_{MAX}$. For a maximum ripple current stays below a specified value, the inductor should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_L(MAX)}][1 - \frac{V_{OUT}}{V_{IN}(MAX)}]$$

The DC current rating of the inductor should be at least equal to the maximum output current plus half the highest ripple current to prevent inductor core saturation. For better efficiency, a lower DC-resistance inductor should be selected.

2. Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OMAX} \times \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{\frac{1}{2}}}{V_{IN}}$$

It indicates a maximum value at $V_{IN}=2V_{OUT}$, where $I_{RMS}=I_{OUT}/2$. This simple worse-case condition is commonly used for design because even significant deviations do not much relieve. The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize output voltage ripple and load step transients, as well as the amount of bulk capacitor that is necessary to ensure that the control loop is stable. Loop stability can be also checked by viewing the load step transient response as described in the following section. The output ripple, $\triangle V_{OUT}$, is determined by:

$$\Delta V_{OUT} \le \Delta I_L [ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple is the highest at the maximum input voltage since $\triangle I_L$ increases with input voltage.

3. Load Transient

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\triangle I_{LOAD} \times ESR$, where ESR is the effective series resistance of output capacitor. $\triangle I_{LOAD}$ also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During the recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

4. Output Voltage Setting

The output voltage of AUR9703 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} \times (1 + \frac{R_1}{R_2}) = 0.6V \times (1 + \frac{R_1}{R_2})$$

The resistive divider senses the fraction of the output voltage as shown in Figure 39.

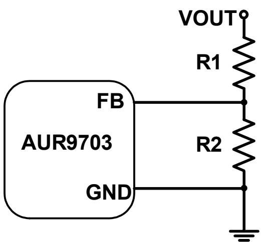


Figure 39. Setting the Output Voltage

Application Information (Continued)

5. Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

Efficiency=100%-L1-L2-…..

Where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very light load currents and the I^2R loss dominates the efficiency loss at medium to heavy load currents.

5.1 The V_{IN} quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low, then to high again, and the packet of charge, dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the internal DC bias current. In continuous mode,

$$I_{GATE} = f \times (Q_P + Q_N)$$

Where Q_P and Q_N are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the V_{IN} and this effect will be more serious at higher input voltages.

5.2 I^2R losses are calculated from internal switch resistance, R_{SW} and external inductor resistance R_L. In continuous mode, the average output current flowing through the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the LX pin is a function of both PMOSFET $R_{DS(ON)}$ and NMOSFET $R_{DS(ON)}$ resistance and the duty cycle (D):

$$R_{SW} = R_{DS(ON)P} \times D + R_{DS(ON)N} \times (1 - D)$$

Therefore, to obtain the I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2 % of total additional loss.

6. Thermal Characteristics

In most applications, the part does not dissipate much heat due to its high efficiency. However, in some conditions when the part is operating in high ambient temperature with high $R_{DS(ON)}$ resistance and high duty cycles, such as in LDO mode, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB, the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction and ambient.

7. PCB Layout Considerations

When laying out the printed circuit board, the following checklist should be used to optimize the performance of AUR9703.

1) The power traces, including the GND trace, the LX trace and the VIN trace should be kept direct, short and wide.
2) Place the input capacitor as close as possible to the VIN and GND pins.
3) The FB pin should be connected directly to the feedback resistor divider.
4) Keep the switching node, LX, away from the sensitive FB pin and the node should be kept small area.

Application Information (Continued)

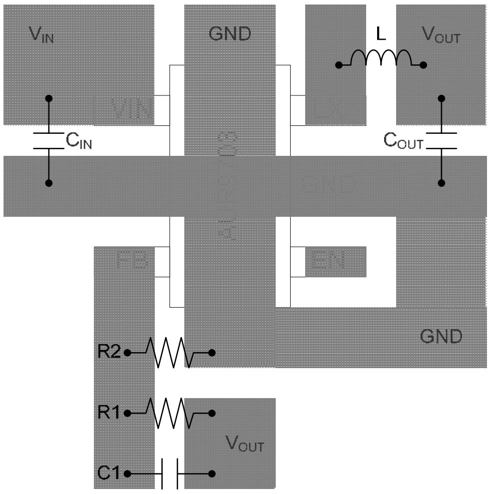
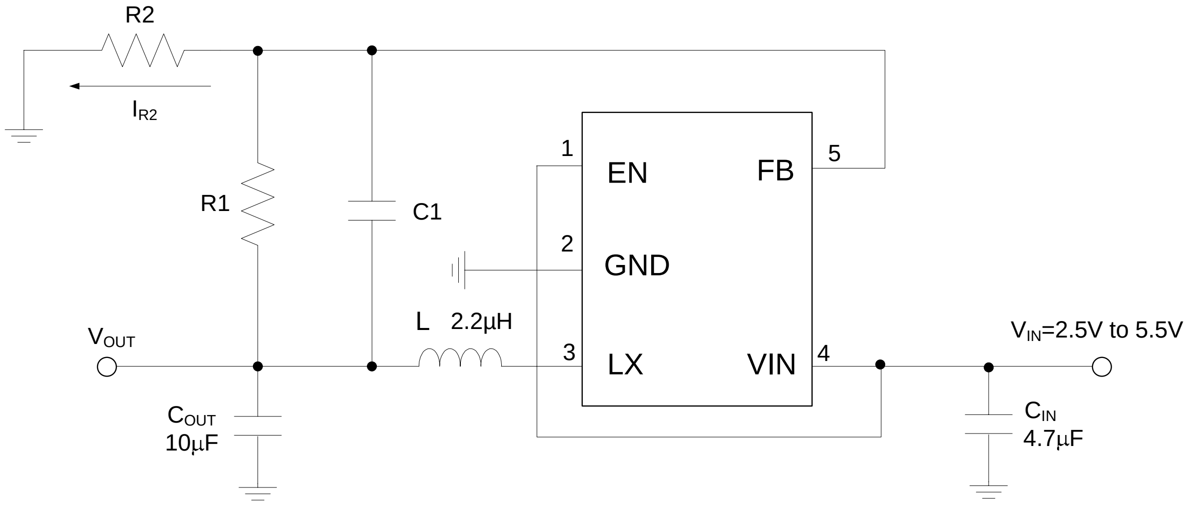


Figure 40. Layout Example of AUR9703

Typical Application



Note 2: $V_{OUT1} = V_{REF} \times (1 + \frac{R_1}{R_2})$.

When R2=300kΩ to 60kΩ, the I_{R2}=2μA to 10μA, and R1×C1 should be in the range between 3×10^{-6} and 6×10^{-6} for component selection.

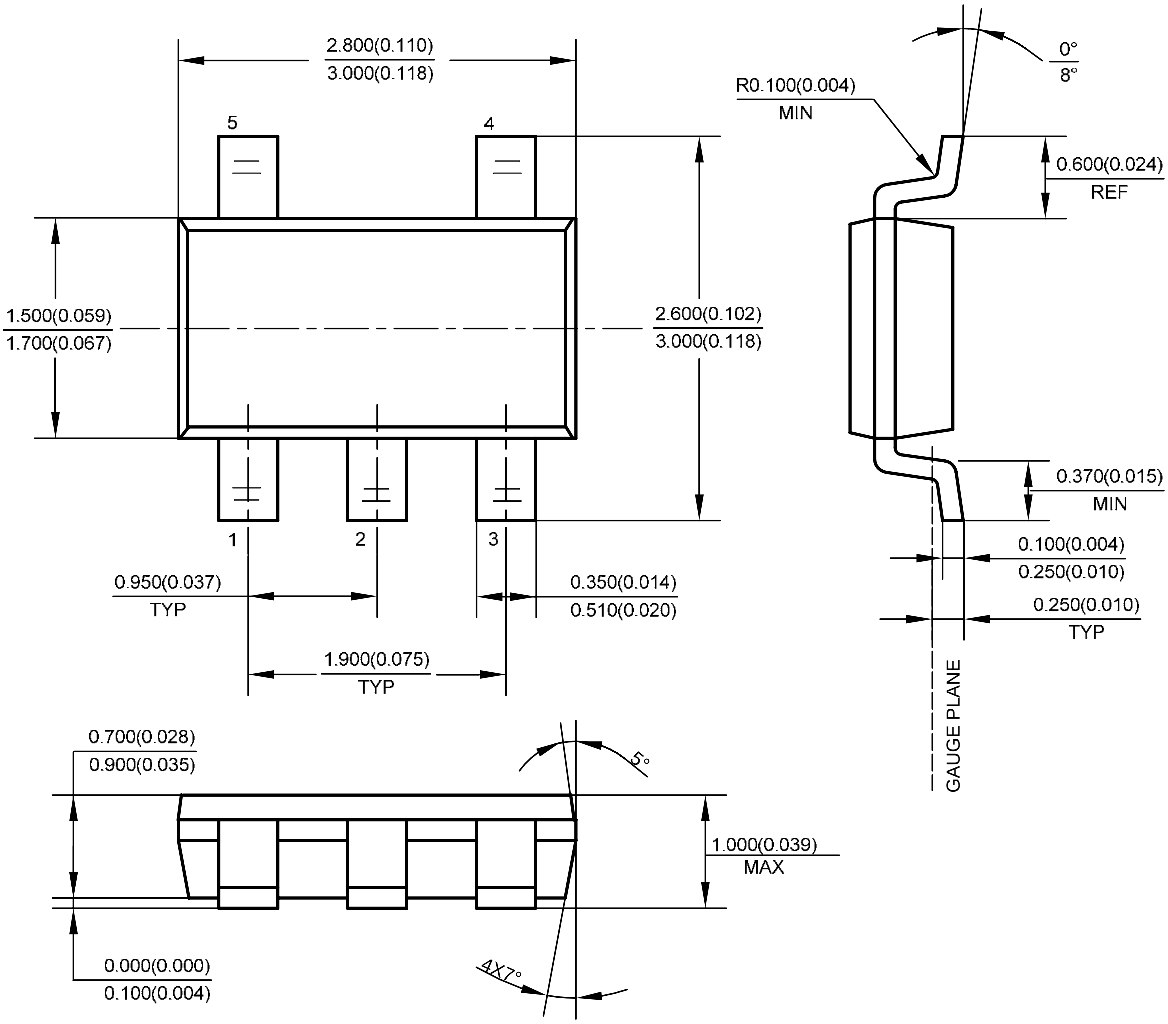
Figure 41. Typical Application Circuit of AUR9703

Table 1. Component Guide

V_{OUT}(V)	R1(kΩ)	R2(kΩ)	C1(pF)	L1(μH)
1.0	68	100	82	2.2
1.2	100	100	56	2.2
1.8	200	100	30	2.2
2.5	320	100	18	2.2
3.3	453	100	13	2.2

Mechanical Dimensions

TSOT-23-5 **Unit: mm(inch)**



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