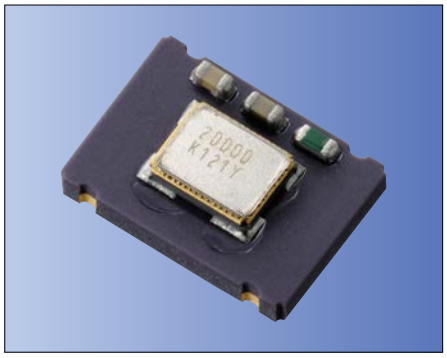
Temperature Compensated Crystal Oscillators (TCXO, VCTCXO)
Surface Mount Type TCXO (LSI Type) KT7050 Series for Femtocell/ Stratum3

7.0×5.0mm



RoHS Compliant

Features
- High stability and high reliability
- 2.7 to 5.5V drive available
- Clipped sine wave or CMOS level output
- Low phase noise
- Disable Function (KT7050A)

Applications
- Femtocell, Stratum3
- SONET/ SDH/ Ethernet

- Compliant to the GR1244-Core & GR253-Core
- Recommended in Microsemi's ZLAN-68 app. note for Stratum3 applications based on tests performed by Kyocera.

How to Order

For Femtocell (Standard Spec.)
Freq. Temp. Chrst. : ±0.1×10⁻⁶/ −10°C to 70°C

KT7050 A 20000 A G T 33 T xx
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

For Stratum3 (Standard Spec.)
Freq. Temp. Chrst. : ±0.28×10⁻⁶/ −40°C to 85°C

KT7050 A 20000 K A W 33 T xx
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

① Series

② Land Type

A	10Pads
B	4Pads

③ Output Frequency

④ Freq. Temp. Chrst.

A	+0.1×10⁻⁶
K	±0.28×10⁻⁶

⑤ Lower Operating Temp.

A	−40°C
G	−10°C
J	0°C

⑥ Upper Operating Temp.

T	+70°C
W	+85°C

⑦ Supply Voltage

33	3.3V

⑦ Voltage Control Function

T	TCXO
Other*	VCTCXO

* Customer Spec.

⑨ Option Code

Packaging (Tape & Reel 1000 pcs./ reel)

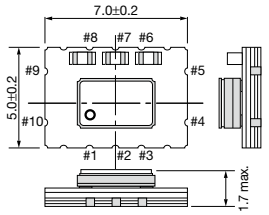
Specifications

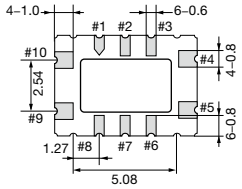
Item	Symbol	Conditions	Min.	Max.	Units
Output Frequency Range	fo	Standard Frequency: 10, 19.2, 20, 24.576, 26, 30.72, 38.88, 40	10	40	MHz
Frequency Tolerance	f_tol	vs Temperature (−10 to +70°C) [±(fmax-fmin)/ 2fo]	−0.1	+0.1	×10⁻⁶
		vs Temperature (−40 to +85°C) [±(fmax-fmin)/ 2fo]	−0.28	+0.28	
		vs Voltage	−0.1	+0.1	
Supply Voltage	Vcc		+2.7	+5.5	V
Current Consumption	Icc	CMOS output	—	6	mA
Frequency Aging	f_age	20years aging @40°C Including temp characteristics, initial tolerance, rated power supply voltage change and load change.	−4.6	+4.6	×10⁻⁶
Voltage Control Range	f_cont	Positive *100k ohm min	±5	±20	×10⁻⁶
Output Level	Vpp	Clipped Sine, Load: 10k ohm // 10pF	0.8	—	Vp-p
Low Level Output Voltage	VOL	CMOS, Load: 15pF IOL = 4mA	—	10% Vcc	V
High Level Output Voltage	VOH	CMOS, Load: 15pF IOH = −4mA	90% Vcc	—	V
Rise / Fall Time (10%Vcc to 90%Vcc)	tr/ tf	CMOS, Load: 15pF	—	8	ns
Symmetry	SYM	50% Vcc	45	55	%
Phase Noise @20MHz	—	− 90 (@10Hz offset) −120 (@100Hz offset) −140 (@1kHz offset) −150 (@10kHz offset) −150 (@100kHz offset)			dBc/ Hz

* Please contact us for other specifications.

Dimensions

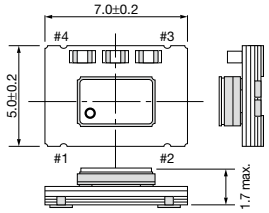
KT7050A

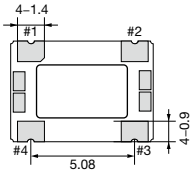




Pin Connection	
#1	Do not connect (Pin1)
#2/3	Do not connect
#4	GND
#5	Output
#6/7	Do not connect
#8	Tri-state Enable/ Disable connect
#9	Vcc
#10	Voltage Control (VCTCXO), GND (TCXO)

KT7050B





Pin Connection	
#1	Voltage Control (VCTCXO), GND (TCXO)
#2	GND
#3	Output
#4	Vcc

Recommended Land Pattern (Unit: mm)